X-Powers

AXP288

Datasheet

PMIC Optimized For Multi-Core High-Performance System

Revision 1.07

2014.6.24

Revision History

Revision	Date	Description
Rev 1.0	2013.12.10	Version1.0 for Intel
Rev 1.01	2013.12.16	1. Table9-3, T0 change to 1000μs 2. Update table 9-41 and related register 3. Update table 9-43, add 4.35V OCV~percentage
Rev 1.02	2013.12.18	1. Add Pb free description
Rev 1.03	2013.12.20	1. Change the SCK/SDA pull high voltage to 1.8V in typical application circuit
Rev 1.04	2014.1.24	1. Add power on interval description 2. Update table 10-92, change default value 3. Update table 10-77, remove bit[7] description 4. Change the capacitance of VCC_RTC to 10uF in typical application circuit 5. Update table 10-74, remove bit[1:0] description 6. Update table 10-36, remove bit[2] description 7. Update table 10-32, add bit[6] description 8. Swap IRQ description in REG 43H/44H/4BH/4CH 9. Update table 10-89, remove bit[1:0] description 10. Add VBAT condition in power on source 11. Correct table 10-50 description 12. Update table 10-32, add bit[6] description 13. Update the hysteresis of temperature protection threshold 14. Update table 10-9, change bit[3] description 15. Update table 10-4, describe how to clear the indication
Rev 1.05	2014.2.13	1. Update QFN76 package description 2. Add QFN76 board layout example 3. Update table 10-106, correct bit[2:0] description 4. Correct OCV Percentage Table description
Rev 1.06	2014.5.23	1. Version change: Reg03H: 0x41 to 0x51 2. Reg14[3] default value change to 1 3. Use Reg14[7] as an enable bit for cold reset within global reset input 4. When BC module isn't work, disable RID detection by default 5. Update section 9.1 / 9.1.1 / 9.4 / 9.4.2 / 9.4.5 6. Update RTC_LDO output capacitor's value 7. Update Reg80 bit[7], bit[3],bit[1] description

		8. Correct Reg3BH Bit[4],bit[3-0] description 9. Update the max charge current to 2.8A 10. Update electrical characteristics description 11. Correct Reg25H Reg26H default value to A8 12. Add table-1 for part number description 13. Add Package materials information Figure 11-3 14. Add RegA0H RegA1H real time value of battery voltage description 15. Update Reg80H bit[7] description 16. Update RegB8H bit[3] description 17. Add order information and table 11 18. Correct table 9-29 description 19. Correct Reg01H bit[4] description 20. Correct Reg59H, 5BH, 79H, 7BH, 7DH description
Rev 1.07	2014.6.24	1. Add AXP288D description

Declaration

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Catalog

1 Overview

AXP288 is customized PMIC for Intel Bay trail (BYT-CR) and Cherry trail (CHT-CR) platforms.

AXP288 is a highly integrated PMIC targeting at Li-battery (Li-ion or Li-polymer) applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for processors to meet the increasingly complex and accurate requirements on power control.

AXP288 comes with an adaptive USB3.0-compatible Flash Charger that supports up to 2.8A charge current. It also supports 20 channels power outputs (including 6-CH Bucks). To ensure the security and stability of the power system, AXP288 provides multiple channels 12-bit ADC for voltage/current/temperature monitor and integrates protection circuits such as OVP, UVP, OTP, and OCP. Moreover, AXP288 features a unique E-Gauge™(Fuel Gauge) system, making power gauge easy and exact.

In addition, AXP288 embraces a fast interface for the system to dynamically adjust output voltage and enable power outputs so that the battery life can be extended to the largest extent.

Besides, AXP288 features an IPS™ (Intelligent Power Select) circuit to transparently select power path among USB and Li-battery to system load.

AXP288 is available in 9mm x 9mm 76-pin QFN package, and the package is Pb free.

Applications :

• Tablet, Smart phone, DVR, Desktop, Dongle

• UMPC-like, Student Computer

Supported processers and corresponding part numbers:

Table 1

Compatible Processor	Application	Part Number
Bay Trail CR	Tablet	AXP288
Bay Trail CR	Desktop, Dongle	AXP288D
Cherry Trail CR	Tablet	AXP288C

2 Feature

--6 Frequency spread Bucks

- BUCK1: PFM/PWM, 0.5-1.20V, 10mV/step, 1.22-1.30V, 20mV/step, IMAX=3A, DVM
- BUCK2: PFM/PWM, 0.6-1.10V, 10mV/step, 1.12-1.52V, 20mV/step, IMAX=1.8A, DVM
- BUCK3: PFM/PWM, 0.6-1.10V, 10mV/step, 1.12-1.52V, 20mV/step, IMAX=2.5A, DVM
- BUCK4: PFM/PWM, 0.8-1.12V, 10mV/step, 1.14-1.84V, 20mV/step, IMAX=2.5A, DVM, default set by BUCK4SET
- BUCK5: PFM/PWM, 0.5-1.20V, 10mV/step, 1.22-1.30V, 20mV/step, IMAX=6A, DVM, Dual-Phase
- BUCK6: PFM/PWM, 1.6-3.4V, 0.1V/step, 19 steps, IMAX=1.5A
- BUCK1/5:71+5 steps；BUCK2/3:51+21steps；BUCK4:33+37 steps
- DVM(Dynamic Voltage scaling Management) ramp rate: 2.5mV/us at buck frequency 3MHz

--15 LDOs & Switch

- RTCLDO: VCC_RTC=3V, IMAX=60mA, always enable
- ALDO1: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=500mA, input is ALDOIN
- ALDO2: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=300mA, input is ALDOIN
- ALDO3: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=200mA, input is ALDOIN
- DLDO1: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps; IMAX=500mA, input is DLDOIN
- DLDO2: Analog LDO, 0.7-3.4V, 100mV/step; 28 steps; 3.4-4.2V, 200mV/step, 4 steps. IMAX=400mA, input is DLDOIN
- DLDO3: Analog LDO, 0.7-3.3V, 100mV/step; 27 steps, IMAX=300mA, input is DLDOIN
- DLDO4: Analog LDO, 0.7-3.3V, 100mV/step; 27 steps, IMAX=500mA, input is DLDOIN
- ELDO1: Digital LDO, 0.7-1.9V, 50mV/step; 25 steps, IMAX=400mA, input is ELDOIN
- ELDO2: Digital LDO, 0.7-1.9V, 50mV/step; 25 steps, IMAX=200mA, input is ELDOIN
- ELDO3: Digital LDO, 0.7-1.9V, 50mV/step; 25 steps, IMAX=200mA, input is ELDOIN
- FLDO1: Digital LDO, 0.7-1.45V, 50mV/step, 16 steps, IMAX=300mA, input is FLDOIN
- FLDO2: Digital LDO, 0.7-1.45V, 50mV/step, 16 steps, IMAX=100mA, input is FLDOIN
- FLDO3: Sink and Source LDO, FLDOIN/2, BUCK4/2, IMAX=30mA, input is FLDOIN, for VREFDQ， default on
- GPIO0LDO: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=100mA, input is ALDOIN
- GPIO1LDO: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=150mA, input is ALDOIN
- CHGLED: GND switch for motor or LED, IMAX=100mA

--Two wire serial interface (SCK/SDA) supporting standard and quick slave mode

--Intelligent Power Select (IPS), VBUS-IPSOUT is 80mΩ typically

--Adaptive Li battery PWM charger with current total up to 2.8A

--Battery Fuel Gauge and coulomb counter

--Power output on/off touch key

--Internal Temperature sensor and protection

--Safe and Soft start up

3 Typical Application

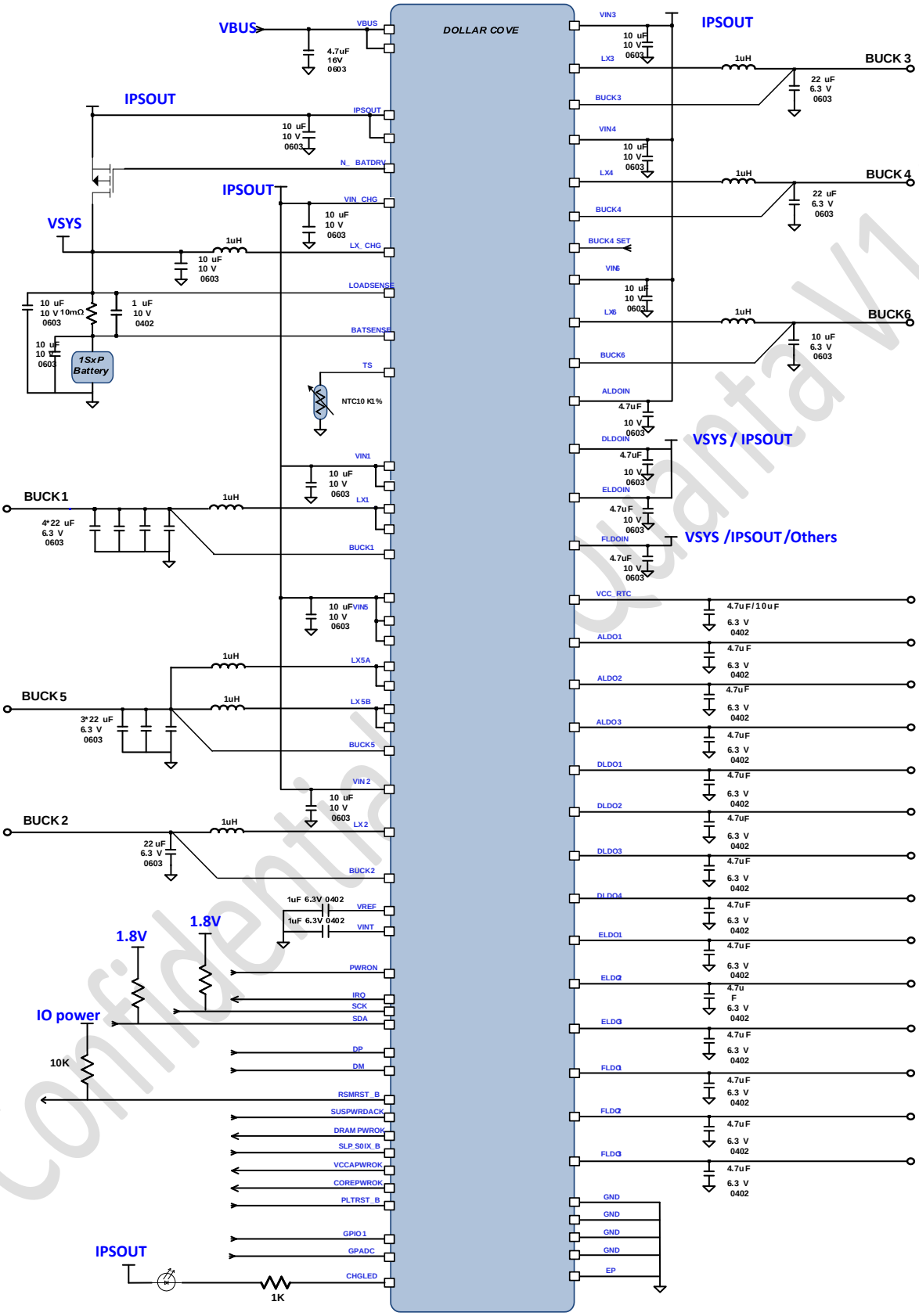

Figure 3-1

4 Pin Map

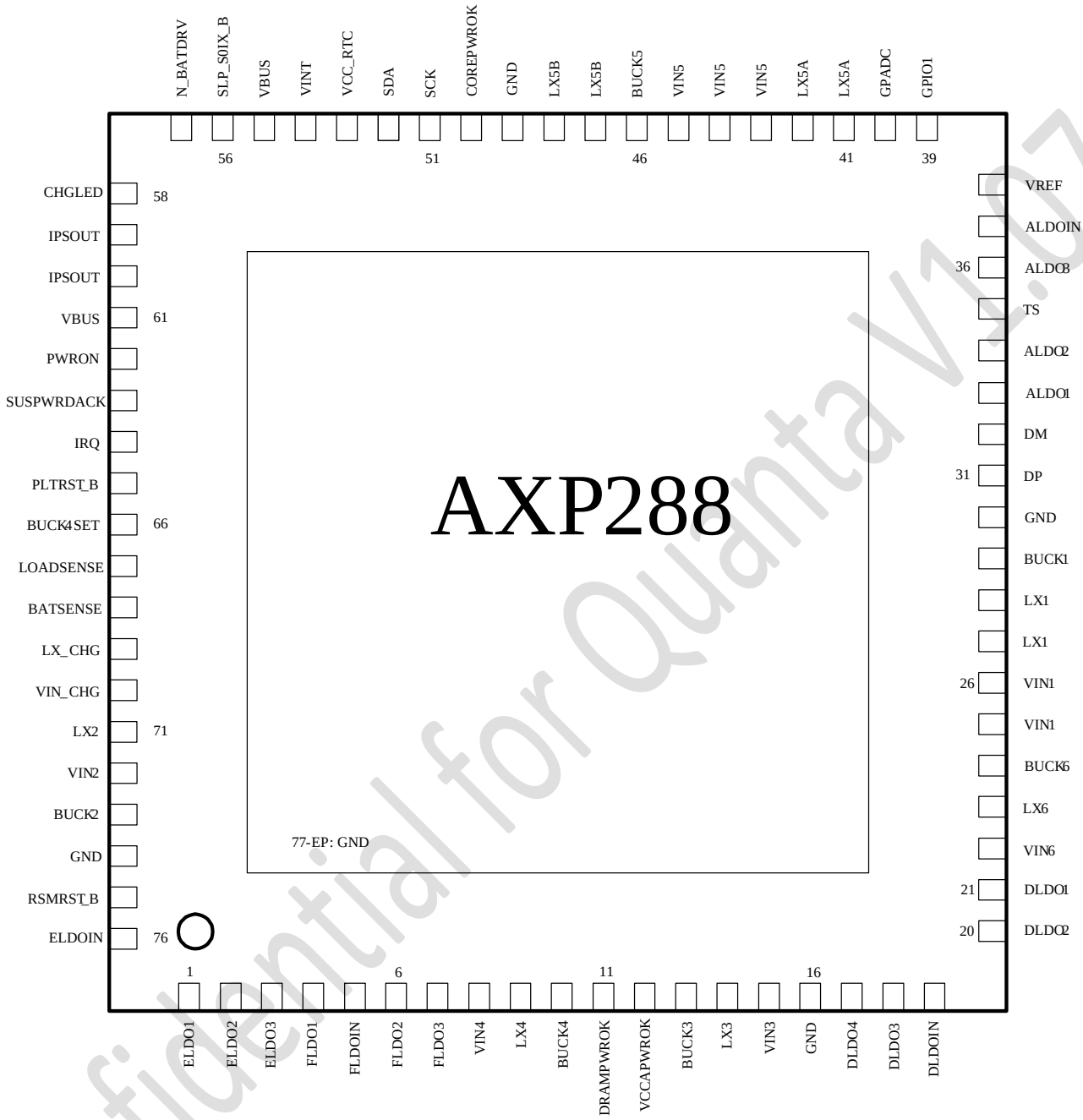

Figure 4-1

5 Pin Description

Table 5-1

N um	Name	Type	Condition	Description
1	ELDO1	O		Output pin of ELDO1
2	ELDO2	O		Output pin of ELDO2
3	ELDO3	O		Output pin of ELDO3
4	FLDO1	O		Output Pin of FLDO1
5	FLDOIN	PI		FLDO input source
6	FLDO2	O		Output Pin of FLDO2
7	FLDO3	O		Output Pin of FLDO3
8	VIN4	PI		BUCK4 input source
9	LX4	IO		Inductor Pin for BUCK4
10	BUCK4	I		BUCK4 feedback pin
11	DRAMPWROK	O		Power good pin, push-pull output, and pull to V_{BUCK4} internal. DRAMPWROK is an active high dedicated output signal. DRAMPWROK asserts when voltage rails V_{BUCK4} is within 15% of its nominal voltage
12	VCCAPWROK	O		Power Good pin, push-pull output, and pull to V_{BUCK4} internal. VCCAPWROK asserts when all voltage rails to the SOC that are supposed to be on in S0 and S0IX states are within 15% of its nominal voltage
13	BUCK3	I		BUCK3 feedback pin
14	LX3	IO		Inductor Pin for BUCK3
15	VIN3	PI		BUCK3 input source
16	GND	G		GND for internal analog circuit
17	DLDO4	O		Output Pin of DLDO4
18	DLDO3	O		Output Pin of DLDO3
19	DLDOIN	PI		DLDOIN input source
20	DLDO2	O		Output Pin of DLDO2
21	DLDO1	O		Output Pin of DLDO1
22	VIN6	PI		BUCK6 input source
23	LX6	IO		Inductor Pin for BUCK6
24	BUCK6	I		BUCK6 feedback pin
25	VIN1	PI		BUCK1 input source
26	VIN1	PI		BUCK1 input source
27	LX1	IO		Inductor Pin for BUCK1

N um	Name	Type	Condition	Description
28	LX1	IO		Inductor Pin for BUCK1
29	BUCK1	I		BUCK1 feedback pin
30	GND	G		GND for internal analog circuit
31	DP	I		Charger detection, USB D+
32	DM	I		Charger detection, USB D-
33	ALDO1	O		Output pin of ALDO1
34	ALDO2	O		Output pin of ALDO2
35	TS	I		Battery Temperature Sensor Input or an External ADC Input
36	ALDO3	O		Output pin of ALDO3
37	ALDOIN	PI		ALDO input source
38	VREF	O		Internal reference voltage
39	GPIO1	IO		General purpose I/O or LDO by REG92H. When it's digital input, the logic high level is 1.5V, and the logic low level is 0.5V typically. When it's digital output, the logic high level is decided by REG93H.
40	GPADC	I		General purpose I/O/ADC input or LDO by REG90H. When it's digital input, the logic high level is 1.5V, and the logic low level is 0.5V typically. When it's digital output, the logic high level is decided by REG91H.
41	LX5A	IO		Inductor Pin for BUCK5 phase A
42	LX5A	IO		Inductor Pin for BUCK5 phase A
43	VIN5	PI		BUCK5 input source
44	VIN5	PI		BUCK5 input source
45	VIN5	PI		BUCK5 input source
46	BUCK5	I		BUCK5 feedback pin
47	LX5B	IO		Inductor Pin for BUCK5 phase B
48	LX5B	IO		Inductor Pin for BUCK5 phase B
49	GND	G		GND for internal analog circuit
50	COREPWROK	O		Power Good pin, push-pull output , and pull to VCC_RTC internal. COREPWROK is an active high dedicated output signal. COREPWROK asserts when all voltage rails to the SOC that are supposed to be on in S0 and S0IX states are within 15% of its nominal voltage
51	SCK	I	2.2KΩ Pull High	Clock pin for serial interface, need a 2.2KΩ Pull High.
52	SDA	IO	2.2KΩ Pull High	Data pin for serial interface, need a 2.2KΩ Pull High.

N um	Name	Type	Condition	Description
53	VCC_RTC	O		Output pin of VCC_RTC
54	VINT	PO		Internal logic power, 1.8V
55	VBUS	PI		VBUS input, must tied to pin 61
56	SLP_S0IX_B	I		SOC sleep signal, SLP_S0IX_B is an active low dedicated input signal from the SOC that indicates S0IX state entry upon assertion (SLP_S0IX=LOW) and exit upon de-assertion (SLP_S0IX_B=HIGH). Typically, the logic high level is 1.5V, and the logic low level is 0.5V.
57	N_BATDRV	O		BAT to PS extern PMOS driver
58	CHGLED	O		Charger status indication
59	IPSOUT	PO		System power source
60	IPSOUT	PO		System power source
61	VBUS	PI		VBUS input, must tied to pin 55
62	PWRON	I		Power On-Off key input，Internal 100k pull high to VINT pin
63	SUSPWRDACK	I		Power down signal, SUSPWRDACK is an active high dedicated input signal from the SOC that tells the PMIC to turn off all rails but RTC. Typically, the logic high level is 1.5V, and the logic low level is 0.5V.
64	IRQ	O	10KΩ Pull High	Interrupt output, open drain output, need a 10KΩ Pull High
65	PLTRST_B	I		Reset signal from SOC to PMIC. Typically, the logic high level is 1.5V, and the logic low level is 0.5V.
66	BUCK4SET	I		Setting BUCK4 default Output Voltage, this pin must tied to GND/VINT or floating.
67	LOADSENSE	I		PWM Charger Current Sense Resistance Positive Input
68	BATSENSE	I		PWM Charger Current Sense Resistance Negative Input
69	LX_CHG	IO		Inductor Pin for PWM Charger
70	VIN_CHG	I		Charger input source
71	LX2	IO		Inductor Pin for BUCK2
72	VIN2	PI		BUCK2 input source
73	BUCK2	I		Feedback to BUCK2
74	GND	G		GND for internal analog circuit
75	RSMRST_B	O	10KΩ Pull High	Power good pin, open drain output, need a 10KΩ Pull High. Resume reset output to SOC, de-asserted (=1) after ALDO3 is within 15% nominal voltage
76	ELDOIN	PI		ELDO input source
77	EP	G		Exposed pad, connected to system ground

6 Block Diagram

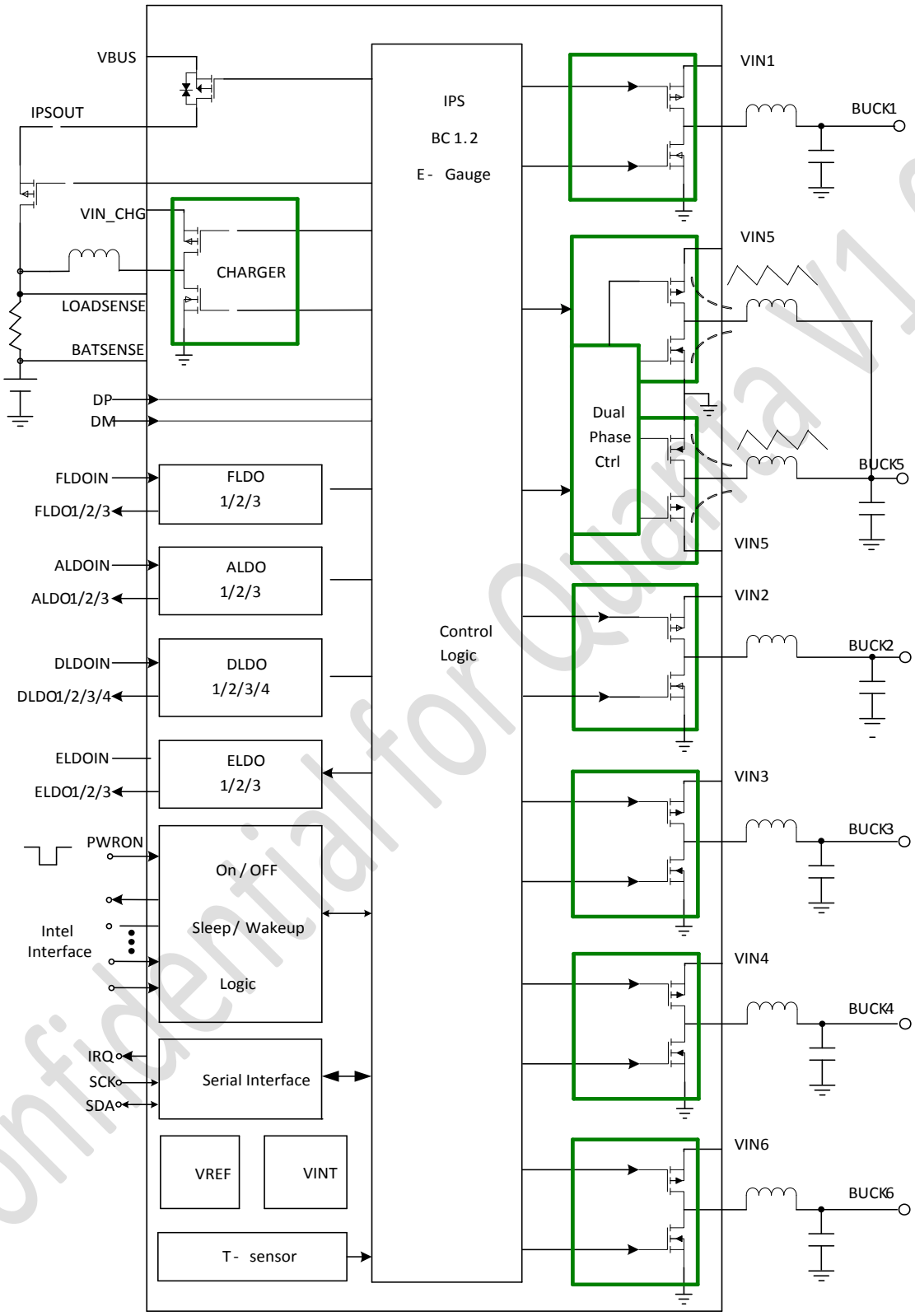

Figure 6-1

7 Absolute Maximum Ratings

Table 7-1

SYMBOL	DESCRIPTION	VALUE	UNITS
VBUS	Input Voltage Range	-0.3 to 11	V
V_{RIO1}	Voltage Range on pins RSMRST_B, SUSPWRDACK, IRQ, PLTRST_B, COREPWROK	-0.3 to 5.5	V
V_{RIO2}	Voltage Range on pins SCK, SDA, GPADC, GPIO1, SLP_S0IX_B	-0.3 to IPSOUT+0.3	V
V_{RIO3}	Voltage Range on pins DRAMPWROK, VCCAPWROK	-0.3 to V_{BUCK4}+0.3	
V_{RIO3}	Voltage Range on pin PWRON	-0.3 to 2.1	V
T_j	Operating Junction Temperature Range	125	℃
T_A	Operating Temperature Range	-20 to 85	℃
Ts	Storage Temperature Range	-40 to 150	℃
T_{LEAD}	Maximum Soldering Temperature (at leads，10sec)	260	℃
V_{ESD}	Maximum ESD stress voltage，Human Body Model	>2000	V
P_D	Internal Power Dissipation	2700	mW

8 Electrical Characteristics

Table 8-1

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS						
V_{IN}	VBUS Input Voltage		3.5		7	V
I_{OUT}	V_{OUT} Current Available Before Loading BAT		100	500	4000	mA
V_{UVLO}	VBUS Under Voltage Lockout			3.5		V
V_{OUT}	IPSOUT Output Voltage		2.9		5.0	V
R_{VBUS}	Internal Ideal Diode On Resistance	VBUS to IPSOUT		80		mΩ
Battery Charger						
V_{TRGT}	BAT Charge Target Voltage		4.1	4.2	4.35	V
I_{CHRG}	Charge Current		200	1200	2800	mA
I_{TRKL}	Trickle Charge Current Ratio to I_{CHRG}			10%		mA
V_{TRKL}	Trickle Charge Threshold Voltage			3.0		V
ΔV_{RECHG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{TARGET}		-100		mV
T_{TIMER1}	Charger Safety Timer Termination Time	Trickle Mode	40	50	70	min
T_{TIMER2}	Charger Safety Timer Termination Time	CC Mode	360	480	720	min
I_{END}	End of Charge Indication Current Ratio to I_{CHRG}	CV Mode	10%	10%	20%	mA
I_{TOLER}	The tolerance of charge current	I_{CHRG} = 0.2A - 2.8A	±3%	±5%	±10%	mA
V_{TOLER}	The tolerance of charge target voltage				±0.5%	V
NTC						
$V_{LTF\text{-}work}$	Cold Temperature Fault Threshold Voltage For Battery Work		0	3.226	3.264	V
$V_{HTF\text{-}work}$	Hot Temperature Fault Threshold Voltage For Battery Work		0	0.282	3.264	V
$V_{LTF\text{-}charge}$	Cold Temperature Fault Threshold Voltage For Battery Charge		0	2.112	3.264	V
$V_{HTF\text{-}charge}$	Hot Temperature Fault Threshold Voltage For Battery Charge		0	0.397	3.264	V
Off Mode Current						

I_{BATOFF}	OFF Mode Current	BAT=3.7V		40		μA
BUCK						
f_{OSC}	Oscillator Frequency	Default		3		MHz
L	Inductor value			1.0		μH
BUCK1						
I_{VIN1}	Input Current	PFM Mode I_{BUCK1} =0		40		μA
	Switch Current Limit of PMOS	PWM Mode		3900		mA
I_{BUCK1}	Available Output Current	PWM Mode		3000		mA
V_{BUCK1}	Output Voltage		0.5	1	1.3	V
C_{OUT1}	Output capacitor value		22	4*22	110	μF
BUCK2						
I_{VIN2}	Input Current	PFM Mode I_{BUCK2} =0		40		μA
	Switch Current Limit of PMOS	PWM Mode		2300		mA
I_{BUCK2}	Available Output Current	PWM Mode		1800		mA
V_{BUCK2}	Output Voltage		0.6	1	1.52	V
C_{OUT2}	Output capacitor value		22	22	66	μF
BUCK3						
I_{VIN3}	Input Current	PFM Mode I_{BUCK3} =0		40		μA
	Switch Current Limit of PMOS	PWM Mode		3000		mA
I_{BUCK3}	Available Output Current	PWM Mode		2500		mA
V_{BUCK3}	Output Voltage		0.6	1	1.52	V
C_{OUT3}	Output capacitor value		22	22	66	μF
BUCK4						
I_{VIN4}	Input Current	PFM Mode I_{BUCK4} =0		40		μA
	Switch Current Limit of PMOS	PWM Mode		3000		mA
I_{BUCK4}	Available Output Current	PWM Mode		2500		mA
V_{BUCK4}	Output Voltage		0.8	1.5	1.84	V
C_{OUT4}	Output capacitor value		22	22	66	μF
BUCK5 (Dual Phase)						
I_{VIN5}	Input Current	PFM Mode I_{BUCK5} =0		50		μA
	Switch Current Limit Per PMOS	PWM Mode		3900		mA

I_{BUCK5}	Available Output Current	PWM Mode		6000		mA
V_{BUCK5}	Output Voltage		0.5	1	1.3	V
C_{OUT5}	Output capacitor value		44	3*22	132	µF
BUCK6						
I_{VIN6}	Input Current	PFM Mode I_{BUCK6} =0		40		µA
	Switch Current Limit of PMOS	PWM Mode		2000		mA
I_{BUCK6}	Available Output Current	PWM Mode		1500		mA
V_{BUCK6}	Output Voltage (3.3V for AXP288D)		1.6	1.8	3.4	V
C_{OUT6}	Output capacitor value		22	22	66	µF
RTCLDO (always on)						
V_{RTCLDO}	Output Voltage	I_{RTCLDO}=1mA		3		V
I_{RTCLDO}	Output Current			60		mA
ALDO1						
V_{ALDO1}	Output Voltage	I_{ALDO1}=1mA	0.7	1.2	3.3	V
I_{ALDO1}	Output Current			500		mA
I_Q	Quiescent Current			60		µA
PSRR	Power Supply Rejection Ratio	V_{ALDO1}=3V,f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{ALDO1}=1.8V,I_{ALDO1}=10mA		40		µVRMS
ALDO2						
V_{ALDO2}	Output Voltage	I_{ALDO2}=1mA	0.7		3.3	V
I_{ALDO2}	Output Current			300		mA
I_Q	Quiescent Current			60		µA
PSRR	Power Supply Rejection Ratio	V_{ALDO2}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{ALDO2}=1.8V,I_{ALDO2}=10mA		40		µVRMS
ALDO3						
V_{ALDO3}	Output Voltage	I_{ALDO1}=1mA	0.7	3.3	3.3	V
I_{ALDO3}	Output Current			200		mA
I_Q	Quiescent Current			60		µA
PSRR	Power Supply Rejection Ratio	V_{ALDO3}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{ALDO3}=1.8V,I_{ALDO3}=10mA		40		µVRMS
DLDO1						
V_{DLDO1}	Output Voltage	I_{DLDO1}=1mA	0.7		3.3	V
I_{DLDO1}	Output Current			500		mA

I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{DLDO1}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{DLDO1}=1.8V,I_{DLDO1}=10mA		40		μVRMS
DLDO2						
V_{DLDO2}	Output Voltage	I_{DLDO2}=1mA	0.7		4.2	V
I_{DLDO2}	Output Current			400		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{DLDO2}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{DLDO2}=1.8V,I_{DLDO2}=10mA		40		μVRMS
DLDO3						
V_{DLDO3}	Output Voltage	I_{DLDO3}=1mA	0.7		3.3	V
I_{DLDO3}	Output Current			300		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{DLDO3}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{DLDO3}=1.8V,I_{DLDO3}=10mA		40		μVRMS
DLDO4						
V_{DLDO4}	Output Voltage	I_{DLDO4}=1mA	0.7		3.3	V
I_{DLDO4}	Output Current			500		mA
I_Q	Quiescent Current			60		μA
PSRR	Power Supply Rejection Ratio	V_{DLDO4}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{DLDO4}=1.8V,I_{DLDO4}=10mA		40		μVRMS
ELDO1						
V_{ELDO1}	Output Voltage (1.8V for AXP288D)	I_{ELDO1}=1mA	0.7		1.9	V
I_{ELDO1}	Output Current			400		mA
I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{ELDO1}=1.2V, f=1kHz		65		dB
ELDO2						
V_{ELDO2}	Output Voltage	I_{ELDO2}=1mA	0.7		1.9	V
I_{ELDO2}	Output Current			200		mA
I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{ELDO2}=1.2V, f=1kHz		65		dB
ELDO3						
V_{ELDO3}	Output Voltage	I_{ELDO3}=1mA	0.7		1.9	V
I_{ELDO3}	Output Current			200		mA

I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{ELDO3}=1.2V, f=1kHz		65		dB
FLDO1						
V_{FLDO1}	Output Voltage	I_{FLDO1}=1mA	0.7	1.2	1.45	V
I_{FLDO1}	Output Current			300		mA
I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{FLDO1}=1.2V, f=1kHz		65		dB
FLDO2						
V_{FLDO2}	Output Voltage	I_{FLDO2}=1mA	0.7	1.2	1.45	V
I_{FLDO2}	Output Current			100		mA
I_Q	Quiescent Current			35		μA
PSRR	Power Supply Rejection Ratio	V_{FLDO2}=1.2V, f=1kHz		65		dB
FLDO3						
V_{FLDO3}	Output Voltage	I_{FLDO3}=1mA	0.5*V_{BUCK4}(default) Or 0.5*V_{FLDOIN}			V
I_{FLDO3}	Output Current			30		mA
I_Q	Quiescent Current			35		μA
GPADC						
$V_{GPIO0LDO}$	Output Voltage	REG90H[2:0]=011, $I_{GPIO0LDO}$=1mA	0.7		3.3	V
$I_{GPIO0LDO}$	Output Current	REG90H[2:0]=011		100		mA
I_Q	Quiescent Current	REG90H[2:0]=011		35		μA
PSRR	Power Supply Rejection Ratio	REG90H[2:0]=011 V_{GPADC}=3V, f=1kHz		65		dB
GPIO1						
$V_{GPIO1LDO}$	Output Voltage	REG92H[2:0]=011, $I_{GPIO1LDO}$=1mA	0.7		3.3	V
$I_{GPIO1LDO}$	Output Current	REG92H[2:0]=011		150		mA
I_Q	Quiescent Current	REG92H[2:0]=011		35		μA
PSRR	Power Supply Rejection Ratio	REG92H[2:0]=011 V_{GPIO1}=3V, f=1kHz		65		dB
CHGLED						
R_{CHGLED}	Internal Ideal Resistance	Supply Voltage is 0.3V		2		Ω
TWSI						
V_{CC}	Input Supply Voltage		1.8	3.3		V

Addr	TWSI Slave Address (7 bits)			0x34		
f_{SCK}	Clock Operating Frequency			400		kHz
V_{IL}	SCK/SDA Logic Low Voltage	SDA is Open drain pin			0.3*V_{CC}	V
V_{IH}	SCK/SDA Logic Low Voltage		0.7*V_{CC}			V
t_f	Clock Data Fall Time	2.2Kohm Pull High		60		ns
t_r	Clock Data Rise Time	2.2Kohm Pull High		100		ns
VINT						
V_{INT}	Internal power supply for logic circuit			1.8		V
Related IO: PWRON						
$R_{pull-up}$	Internal resister to VINT		50	100		KΩ
V_{IL}	Logic Low Voltage			0.5		V
V_{IH}	Logic High Voltage			1.3	2.1	V
Related IO: IRQ						
V_{IL}	Logic Low Voltage	IRQ is open drain output pin, pull up to IO power (V_{IO}) by 10KΩ			0.3	V
V_{IH}	Logic High Voltage		0.7*V_{IO}		V_{IO}	V
Related IO: RSMRST_B						
V_{IL}	Logic Low Voltage	RSMRST_B is open drain output pin, pull up to IO power (V_{IO}) by 10KΩ			0.3	V
V_{IH}	Logic High Voltage		0.7*V_{IO}		V_{IO}	V
Related IO: SUSPWRDACK						
V_{IL}	Logic Low Voltage	Input pin		0.5		V
V_{IH}	Logic High Voltage			1.3		V
$I_{pull-down}$	Pull down current			15		µA
Related IO: DRAMPWROK						
V_{IL}	Logic Low Voltage	DRAMPWROK is push-pull output pin, pull up to BUCK4 internal			0.3	V
V_{IH}	Logic High Voltage		0.7* V_{BUCK4}		V_{BUCK4}	V
Related IO: SLP_S0IX_B						
V_{IL}	Logic Low Voltage	Input pin		0.5		V
V_{IH}	Logic High Voltage			1.3		V
$I_{pull-down}$	Pull down current			15		µA
Related IO: VCCAPWROK						
V_{IL}	Logic Low Voltage	VCCAPWROK is push-pull output pin, pull up to BUCK4 internal			0.3	V
V_{IH}	Logic High Voltage		0.7* V_{BUCK4}		V_{BUCK4}	V
Related IO: COREPWROK						

V_{IL}	Logic Low Voltage	COREPWROK is push-pull output pin, pull up to V_{RTCLDO} internal			0.3	V
V_{IH}	Logic High Voltage		0.7* V_{RTCLDO}		V_{RTCLDO}	V
Related IO: PLTRST_B						
V_{IL}	Logic Low Voltage	Input pin		0.5		V
V_{IH}	Logic High Voltage			1.3		V
$I_{pull-down}$	Pull down current			15		μA
Related IO: GPADC						
V_{IL}	Logic Low Voltage	REG90H[2:0]=010, digital input		0.5		V
V_{IH}	Logic High Voltage			1.3		V
V_{IL}	Logic Low Voltage	REG90H[2:0]=000, drive low			0.3	V
V_{IH}	Logic High Voltage	REG90H[2:0]=001, drive high (high level set by REG91H)	0.7	3.3	3.3	V
Related IO: GPIO1						
V_{IL}	Logic Low Voltage	REG92H[2:0]=010, digital input		0.5		V
V_{IH}	Logic High Voltage			1.3		V
V_{IL}	Logic Low Voltage	REG92H[2:0]=000, drive low			0.3	V
V_{IH}	Logic High Voltage	REG92H[2:0]=001, drive high (high level set by REG93H)	0.7	3.3	3.3	V

9 Control and operation

When AXP288 works, the TWSI (two wire serial interface) SCK/SDA pin is pulled up to system IO power, and this interface can be used by HOST to access and adjust AXP288's working status.

Note that the external power hereinafter is VBUS input.

9.1 Power on/off and Power sequences

PMIC has power off and power on status. When at off state, all voltage outputs are turned off except VCC_RTC, VINT and charger. At this time if powered by battery, the total power consumption is typically 40uA.

9.1.1 Power on/off sources

Power on source

Below are the 3 power up sources supported by AXP288 in mechanical off state:

1. Charger insertion (VBAT > VBPTH)
2. Battery insertion (VBAT > VBPTH)
3. Power on key pressed (VBAT > VBPTH)

Note：VBPTH (boot threshold), 3.0-3.45V, 150mV/step, 4 steps, default is 3.15V.

Power off source

Below are the few sources that can trigger power down of PMIC:

1. ALDOIN < V_{OFF} (indicating IPSOUT too low)
2. Faulty condition
3. Power on key pressed
4. BYT/CHT cold off

Power on from charger insertion

The PMIC should be able to start the boot sequence from a charger insertion. A charger insertion is detected from a rising voltage on the VBUS node. If 4.1V< VBUS < 7.0V, the charger will start charging immediately and autonomously. If the battery level is above the battery boot threshold, the PMIC will continue the boot process, otherwise the charger will continue charging until the battery boot threshold is reached at which point the PMIC will continue the boot process.

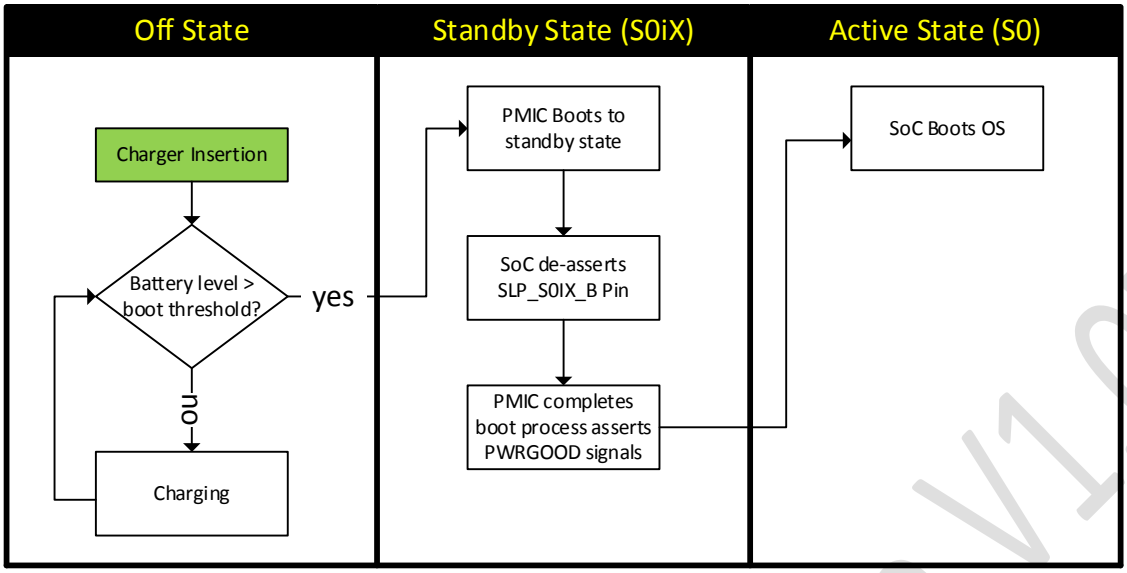

Figure 9-1

Power on from battery insertion

The PMIC should be able to start the boot sequence from a battery insertion. A battery insertion is detected from a rising voltage on the battery node. If the battery level is above the battery boot threshold, the PMIC will continue the boot process.

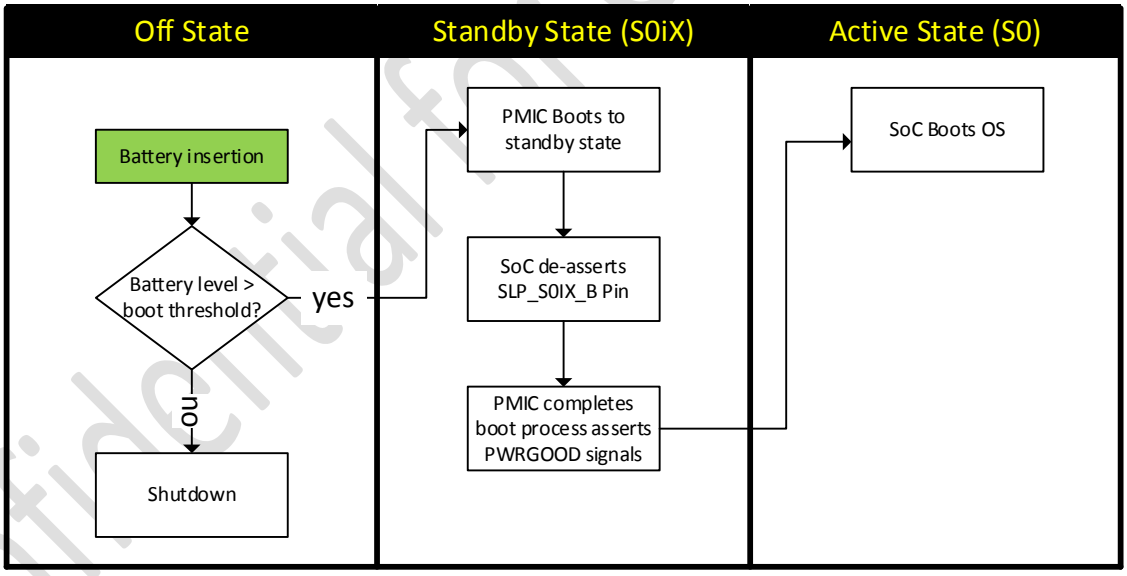

Figure 9-2

Power on from power key pressed

POK----Power On Key

The Power On Key(POK) can be connected between PWRON pin and GND of AXP288. AXP288 can automatically identify the status and then correspond respectively.

The PMIC should be able to start the boot sequence from a power on key pressed. The PMIC has a configurable timer to detect the power on key hold time. Power on key signal in AXP288 is referred as POK. Once falling edge is detected on

POK, PMIC timer will start counting the hold time. POK signal has to be low for at least 32ms for it to be considered a valid signal. If the power on key hold time exceeds the timer threshold (ONLEVEL determined by REG36H [7:6]), the PMIC will continue to boot as long as the battery voltage is above the battery boot threshold. Otherwise the PMIC will remain off.

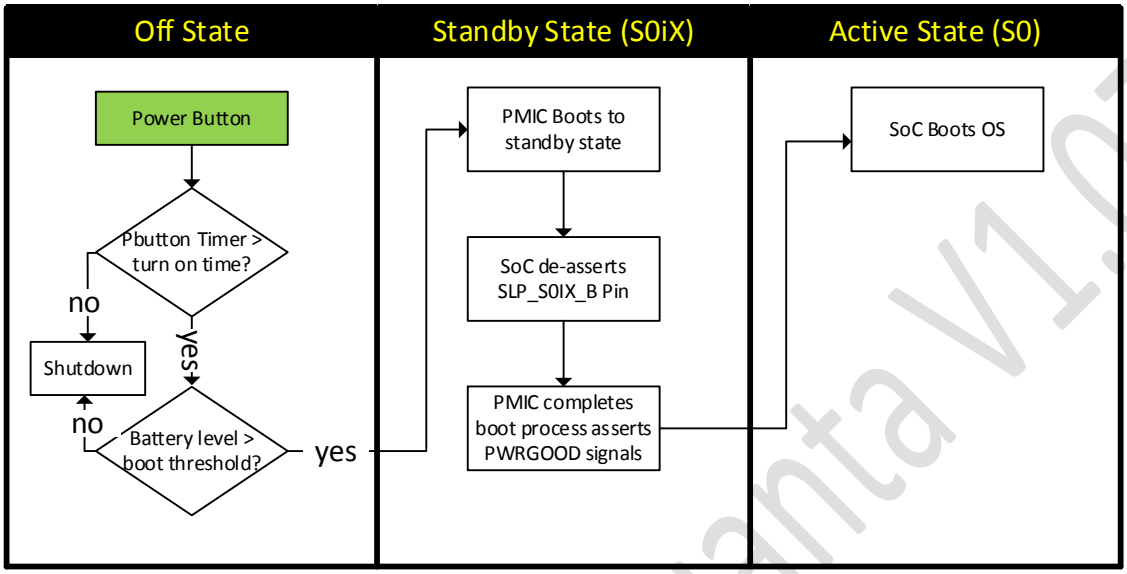

Figure 9-3

Power off from ALDOIN< V_{OFF}

PMIC will constantly monitor voltage level of ALDOIN which is connected to IPSOUT. When VALDOIN < V_{OFF} (default is 2.9V, set in REG 31H[2:0]), PMIC will force shutdown. There will be 500us de-bounce circuit for ALDOIN detection and adjusted hysteresis voltage to prevent false trigger. After force shutdown occurred, PMIC will remain off and wait for power on event to boot up.

V_{OFF} and the compensated hysteresis voltage as below:

Table 9-1

V_{OFF} **condition**	**VX condition (Hysteresis)**
V_{OFF}<=3.0V	0.3V
V_{OFF} = 3.1V	0.2V
V_{OFF} = 3.2V or 3.3V	0.1V

Power off due to faulty condition

PMIC will force shutdown once faulty event happened. Faulty event includes VBUS>7V, PMIC internal temperature exceeds warning level3 (set in REG 8FH [2]) and buck output drop more than 15% than the targeted output voltage (set in Reg 81H).

Power off by power on key pressed

Once power on key pressed, POK signal assert low and need to remain low for 32ms to be considered valid. PMIC has configurable timer to detect power on key hold time. If POK remain low for less than IRQLEVEL (set in REG 36H [5:4]), POKSIRQ will be set. For POK hold time > IRQLEVEL, POKLIRQ will be set. Typically, the system uses POKLIRQ to allow user to express

their demands for Host shutdown.

If POK remain low for more than OFFLEVEL (set in REG 36H [1:0]), POKOIRQ will be issued. After IRQ issued, PMIC will wait for a period of time before it force shutdown (set in REG36H[3]). The PMIC can be turned on automatically (set in REG36[2]). The waiting period is programmable from 0s to 70s(set in REG37H[2:0]).

If POK width is more than 16s, then PMIC will force shutdown immediately. This feature can be set in REG 8FH [3]. When PMIC force shutdown, VCC_RTC will be shut off for 2 seconds, with 1K resistor to pull VCC_RTC to ground and then it will turn back on.

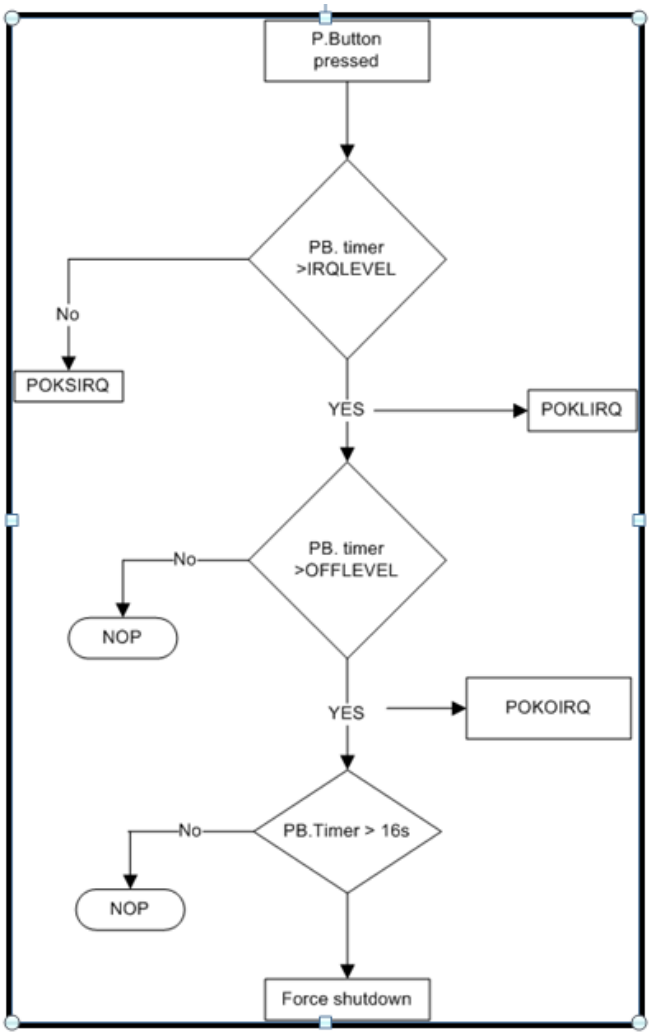

Figure 9-4

9.1.2 Power up sequence

Specially for Intel mode:

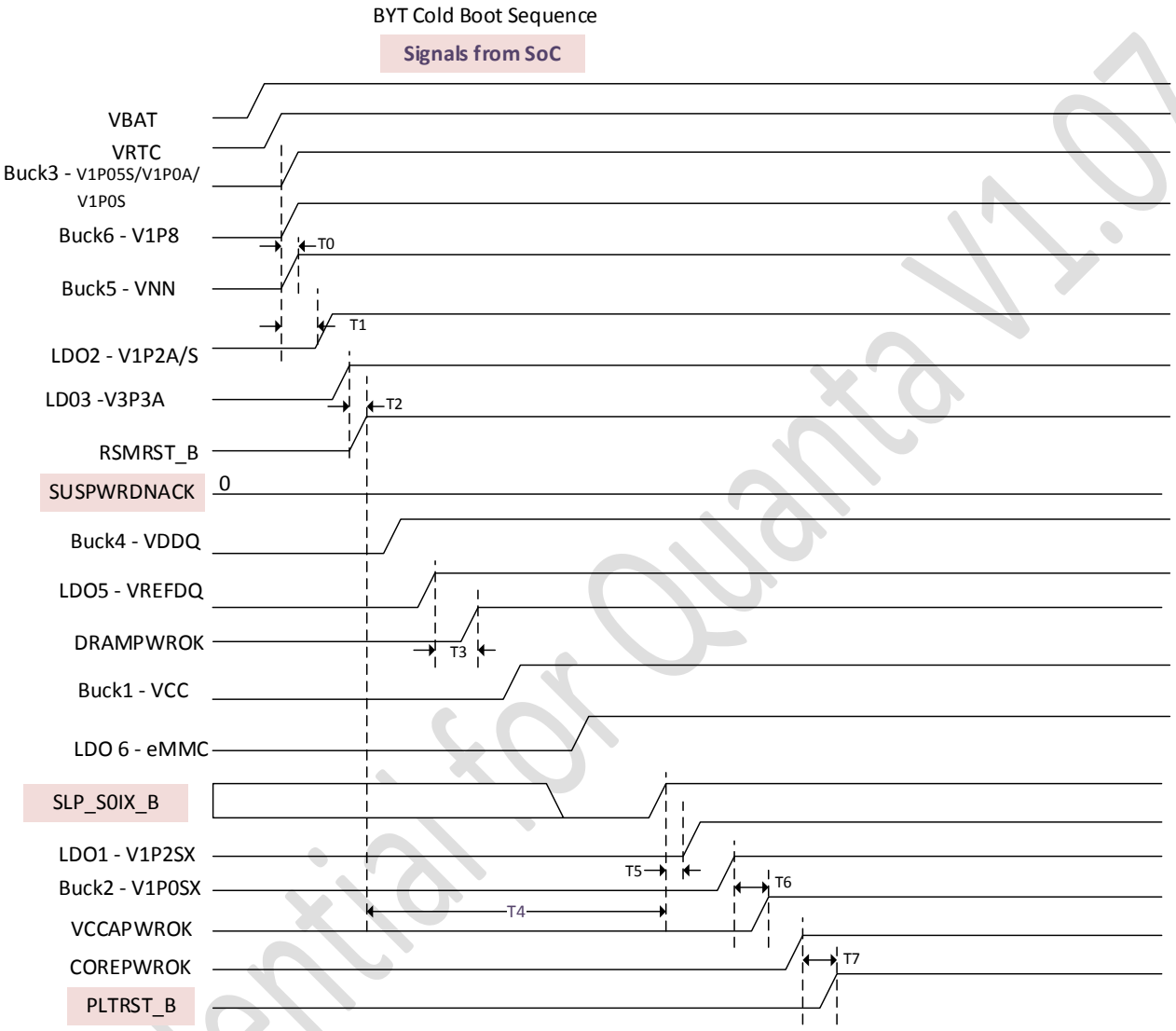

Figure 9-5

Note:

- Buck 3, 5 and 6 power up at the same time
- PMIC Power up sequence has no dependency on SUSPWRDNAK signal
- SLP_S0IX_B signal gates pmic performing the remainder power up sequence

Table 9-2

Parameter	Description	Min	Typical	Max	Units
T0	Rail Ramp-Up Time from 10% to 90% voltage level	0.08	1	2	ms
T1	Rail to Subsequent Rail Turn-On Delay	0.5	1	2.05	ms

Parameter	Description	Min	Typical	Max	Units
T2	V3P3A valid to RSMRST_B de-assertion	0		150	µs
T3	VREFDQ valid (within +/-10% of its final normal value) to DRAMPWROK assertion	0		150	µs
T4	RSMRST_B de-assertion toSLP_S0IX_B de-assertion	80			µs
T5	SLP_S0IX_B de-assertion to first SX rail turn-on delay	0	8	16	ms
T6	Core rails valid to VCCAPWEROK and COREPWROK assertion		1		ms
T7	COREPWROK assertion to PLTRST_B de-assertion	60			µs

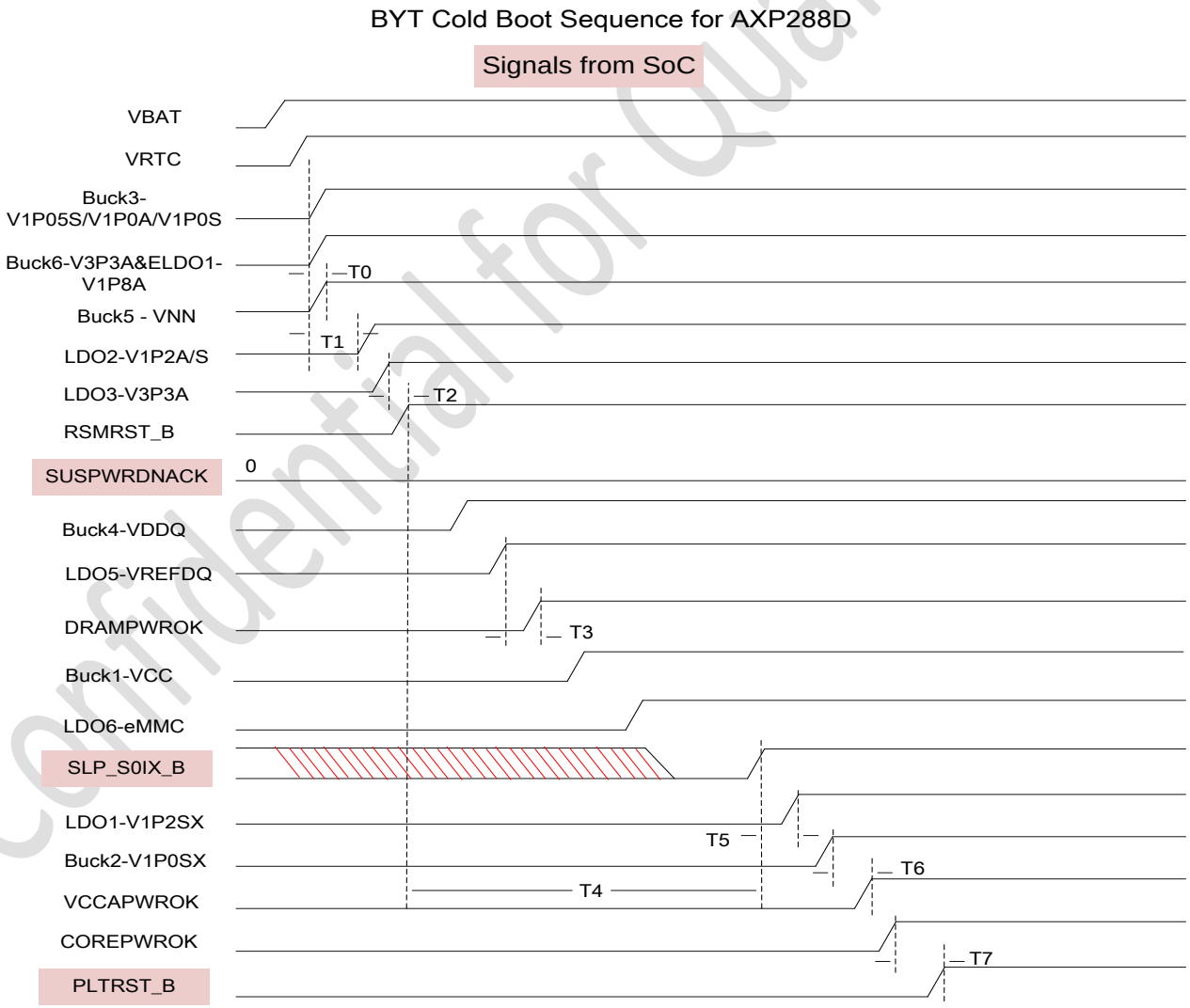

Figure 9-6

Note:

- Buck 3, 5, 6 and ELDO1 power up at the same time
- PMIC Power up sequence has no dependency on SUSPWRDNAK signal
- SLP_S0IX_B signal gates pmic performing the remainder power up sequence

Table 9-3

Parameter	Description	Min	Typical	Max	Units
T0	Rail Ramp-Up Time from 10% to 90% voltage level	0.08	1	2	ms
T1	Rail to Subsequent Rail Turn-On Delay	0.5	1	2.05	ms
T2	V3P3A valid to RSMRST_B de-assertion	0		150	µs
T3	VREFDQ valid (within +/-10% of its final normal value) to DRAMPWROK assertion	0		150	µs
T4	RSMRST_B de-assertion toSLP_S0IX_B de-assertion	80			µs
T5	SLP_S0IX_B de-assertion to first SX rail turn-on delay	0	8	16	ms
T6	Core rails valid to VCCAPWEROK and COREPWROK assertion		1		ms
T7	COREPWROK assertion to PLTRST_B de-assertion	60			µs

CHT Cold Boot Sequence

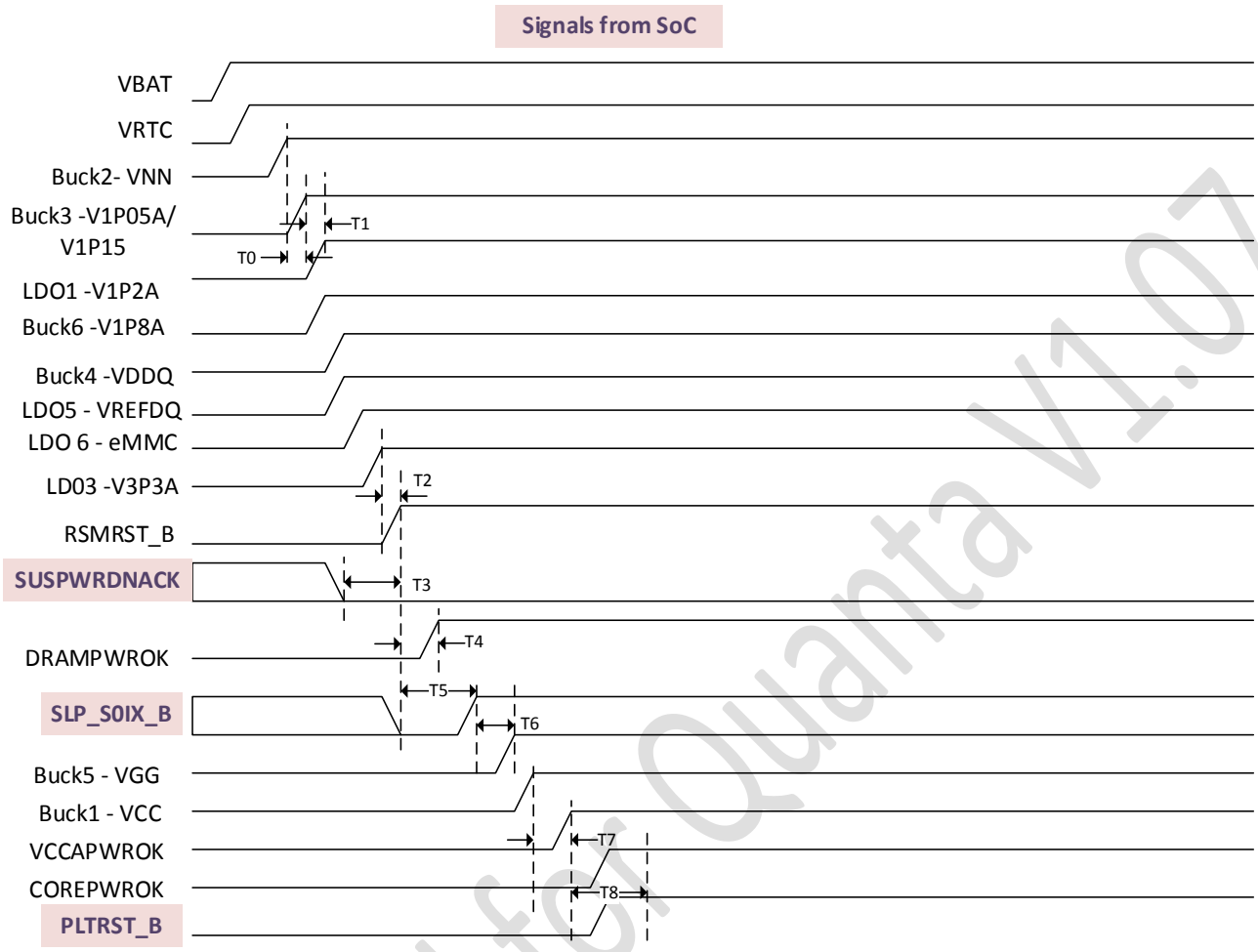

Figure 9-7

Note:

- Buck6 and LDO1 power up at the same time
- LDO6 and LDO3 can power up at the same time
- PMIC Power up sequence has no dependency on SUSPWRDNAK signal
- SLP_S0IX_B signal gates pmic performing the remainder power up sequence

Table 9-4

Parameter	Description	Min	Typical	Max	Units
T0	BUCK2 to BUCK3 turn on delay	Buck2 to Buck3 turn on delay should follow the standard delay (T1), but have an option to support no delay (to be compliant with CHV A0)			µs
T1	Rail to Subsequent Rail Turn-On Delay for all rails unless specified otherwise	0.01	1	2.0	ms

Parameter	Description	Min	Typical	Max	Units
T2	V3P3A valid (90% level) to RSMRST_B de-assertion if SUSPWRDNACK is low	0	24	500	µs
T3	SUSPWRDNACK de-assertion (LOW) to RSMRST_B de-assertion	0			µs
T4	RSMRST_B de-assertion to DRAMPWROK assertion	0		150	µs
T5	RSMRST_B de-assertion to SLP_S0IX_B de-assertion	20			µs
T6	SLP_S0IX_B de-assertion to first subsequent voltage rail start to turn-on delay	0	24	150	ms
T7	Core rails valid to VCCAPWROK and COREPWROK assertion		1		ms
T8	COREPWROK assertion to PLTRST_B de-assertion	60			µs

Timing information

Table 9-5

N	Description	Min	Typical	Max	Units
1	Rail Ramp-Up Time from 10% to 90% voltage level	0.08	1	2	ms
2	Rail to Subsequent Rail Turn-On Delay	0.5	1	2.05	ms
3	V3P3A valid to RSMRST_B de-assertion	0		150	µs
4	VREFDQ valid (within +/-10% of its final normal value) to DRAMPWROK assertion	0		150	µs
5	RSMRST_B de-assertion to SLP_S0IX_B de-assertion	20			µs
6	SLP_S0IX_B de-assertion to first SX rail turn-on delay	0	8	16	ms
7	Core rails valid to VCCAPWEROK and COREPWROK assertion		1		ms
8	COREPWROK assertion to PLTRST_B de-assertion	60			µs

Note:

- VREFDQ power up the same time with VDDQ
- The power down sequence is the opposite sequence of power up

9.1.3 Power down Sequencing

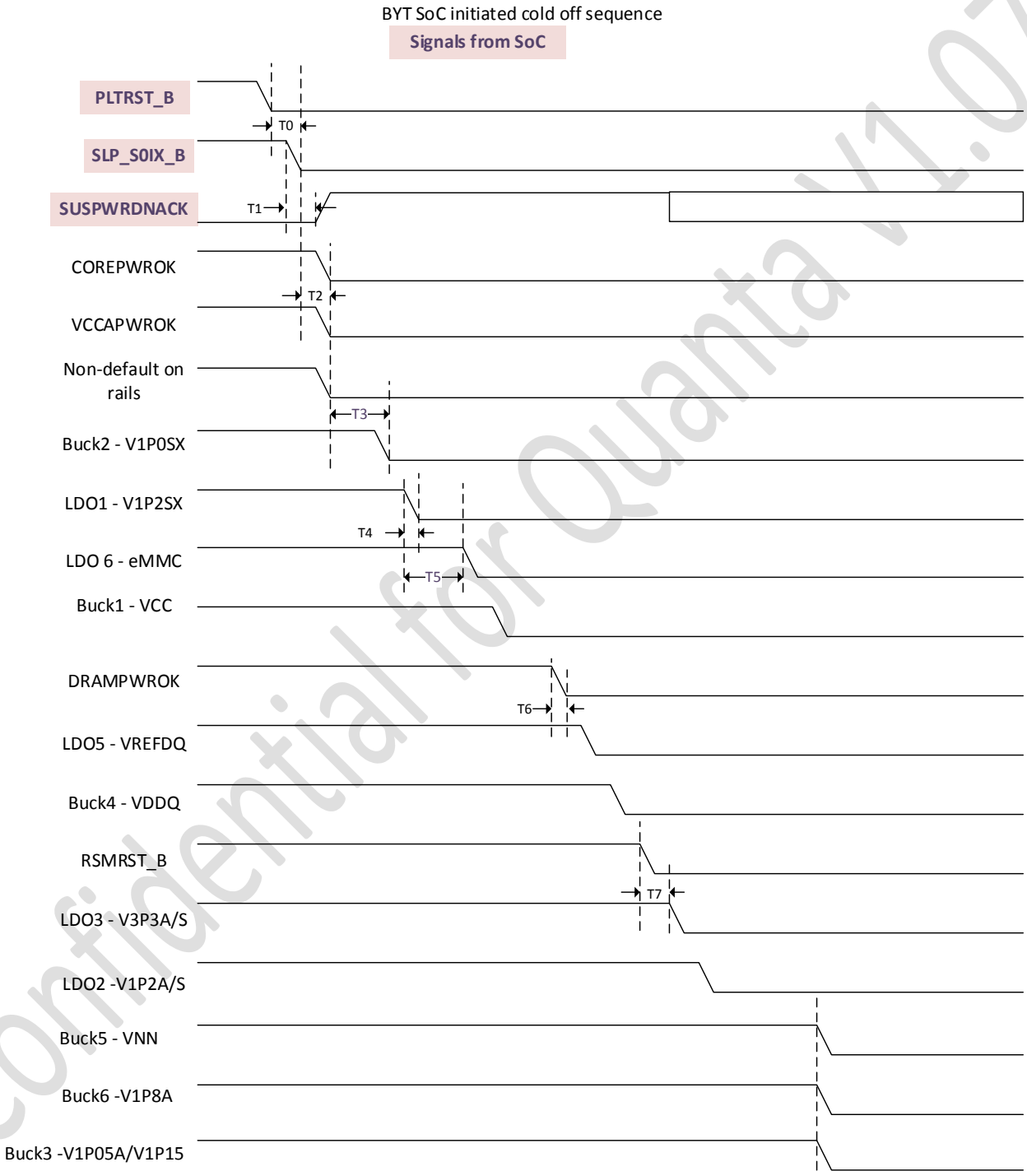

Figure 9-8

Note:

- Power down sequencing is the opposite of power up sequencing
- Buck3, Buck5 and Buck6 power down together

Table 9-6

Parameter	Description	Min	Typical	Max	Units
T0	PLTRST_B assertion to SLP_S0IX_B assertion	31		100	µs
T1	SLP_S0IX_B de-assertion to SUSPWRDNACK assertion	0		50	µs
T2	SLP_S0IX_B assertion to VCCAPWROK and COREPWROK de-assertion	0		150	µs
T3	VCCAPWROK and COREPWROK de-assertion to first VR starts to turn off	0		150	µs
T4	Rail Ramp-down Time from 90% to 10% voltage level	0.5	1	2	ms
T5	Rail to Subsequent Rail Turn-Off Delay	0.5	1	3	ms
T6	DRAMPWROK de-assertion to VREFDQ starts to turn off	0		150	µs
T7	RSMRST_B assertion to V3P3A starts to turn off	0		150	µs

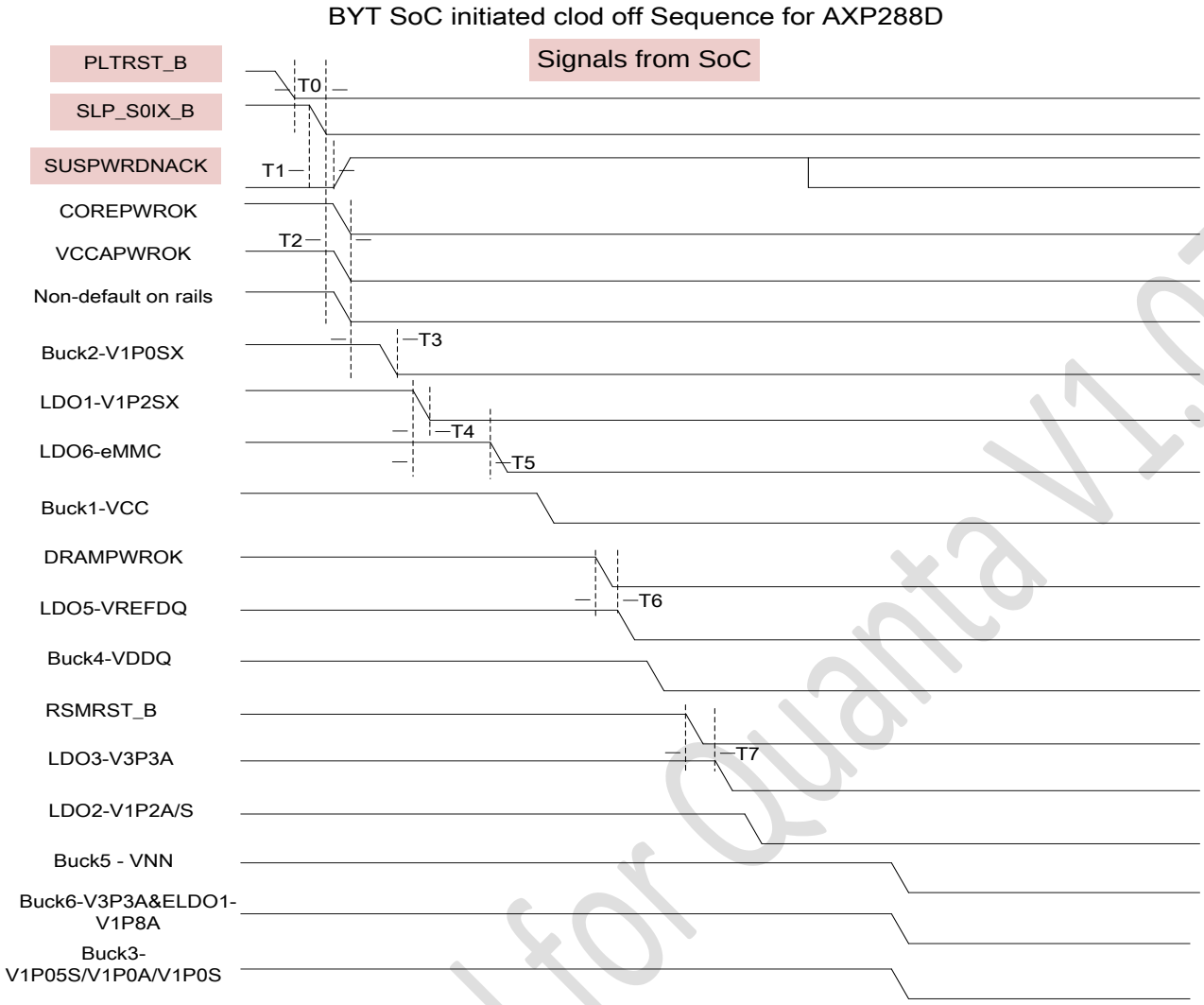

Figure 9-9

Note:

- Power down sequencing is the opposite of power up sequencing
- Buck3, Buck5 and Buck6 power down together

Table 9-7

Parameter	Description	Min	Typical	Max	Units
T0	PLTRST_B assertion to SLP_S0IX_B assertion	31		100	µs
T1	SLP_S0IX_B de-assertion to SUSPWRDNACK assertion	0		50	µs
T2	SLP_S0IX_B assertion to VCCAPWROK and COREPWROK de-assertion	0		150	µs

Parameter	Description	Min	Typical	Max	Units
T3	VCCAPWROK and COREPWROK de-assertion to first VR starts to turn off	0		150	µs
T4	Rail Ramp-down Time from 90% to 10% voltage level	0.5	1	2	ms
T5	Rail to Subsequent Rail Turn-Off Delay	0.5	1	3	ms
T6	DRAMPWROK de-assertion to VREFDQ starts to turn off	0		150	µs
T7	RSMRST_B assertion to V3P3A starts to turn off	0		150	µs

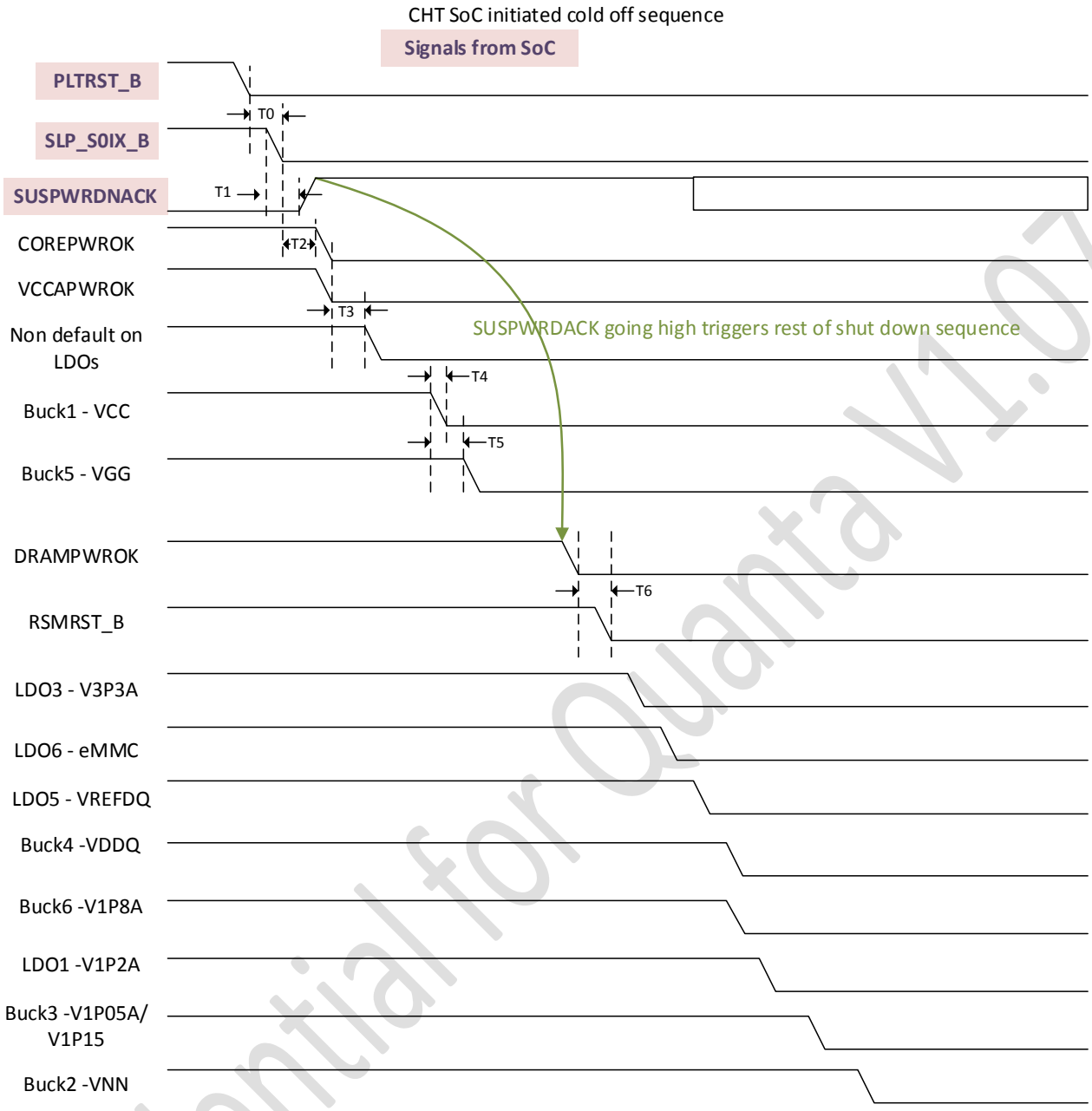

Figure 9-10

Note: Implementation note: SUSPWRDNACK should be sampled after the 50uS

Table 9-8

Parameter	Description	Min	Typical	Max	Units
T0	PLTRST_B de-assertion to SLP_S0IX_B de-assertion	31		100	µs
T1	SLP_S0IX_B de-assertion to SUSPWRDNACK assertion	0		50	µs
T2	SLP_S0IX_B assertion to VCCAPWROK and COREPWROK de-assertion	0		150	µs

Parameter	Description	Min	Typical	Max	Units
T3	VCCAPWROK and COREPWROK de-assertion to first VR starts to turn off	0		150	µs
T4	Rail Ramp-down Time from 90% to 10% voltage level	0.5	1	2	ms
T5	Rail to Subsequent Rail Turn-Off Delay	0.5	1	3	ms
T6	DRAMPWROK de-assertion to RSMRST_B assertion			150	µs

9.1.4 Cold Reset and Global reset

Reset types:

- Global reset: partial power down followed by power up
- Cold reset: full power down followed by power up

There are two special scenarios where a cold reset can be enabled by having the SoC either initiate a cold off or a cold reset in conjunction with a bit in the PMIC being set. These two bits are the COLDRSTEN1 and COLDRSTEN bits as defined below.

Table 9-9

BIT	NAME	FUNCTION	DEFAULT
D[7:2]	RSVD	Reserved	0
D[1]	COLDRSTEN1	Sets whether a global reset or cold reset is done when a global reset is initiated by the SoC 0 – COLD RESET not enabled 1 – COLD RESET enabled	0
D[0]	COLDRSTEN	Sets whether a cold off or cold reset is done when a cold off is initiated by the SoC 0 – COLD RESET not enabled 1 – COLD RESET enabled	0

Cold Reset scenario 1:

The diagram below shows the first special case of a cold reset being enabled based on a cold off and the PMIC register bit being set.

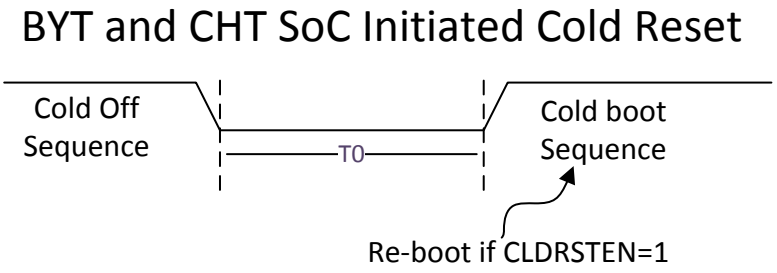

Figure 9-11

Table 9-10

Parameter	Description	Min	Typical	Max	Units
T0	Time delay between power down complete and power up start		50		ms

Cold Reset scenario 2:

The diagram below shows the second special case of a cold reset being enabled based on a global reset and the PMIC register bit being set.

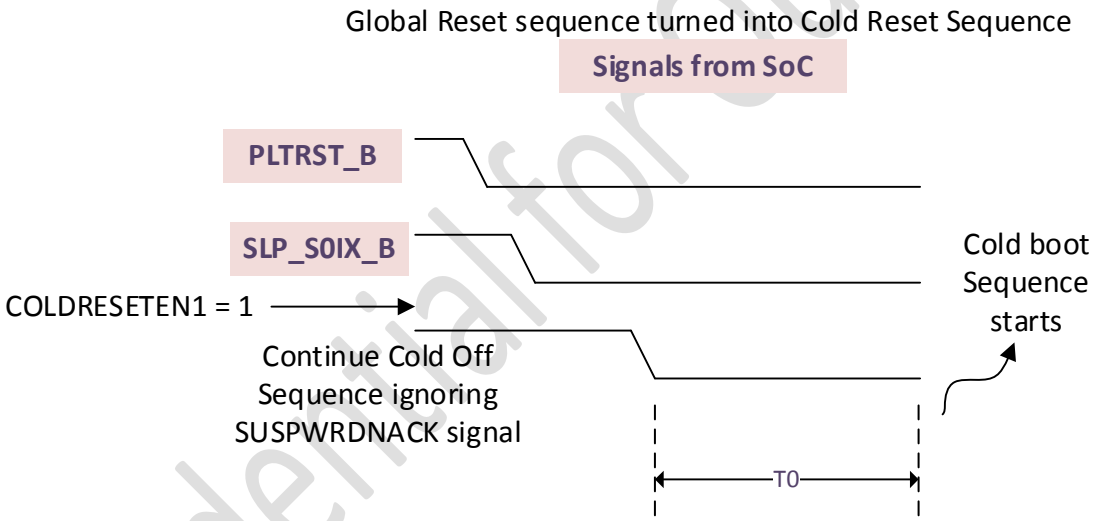

Figure 9-12

Table 9-11

Parameter	Description	Min	Typical	Max	Units
T0	Time delay between power down complete and power up start		50		ms

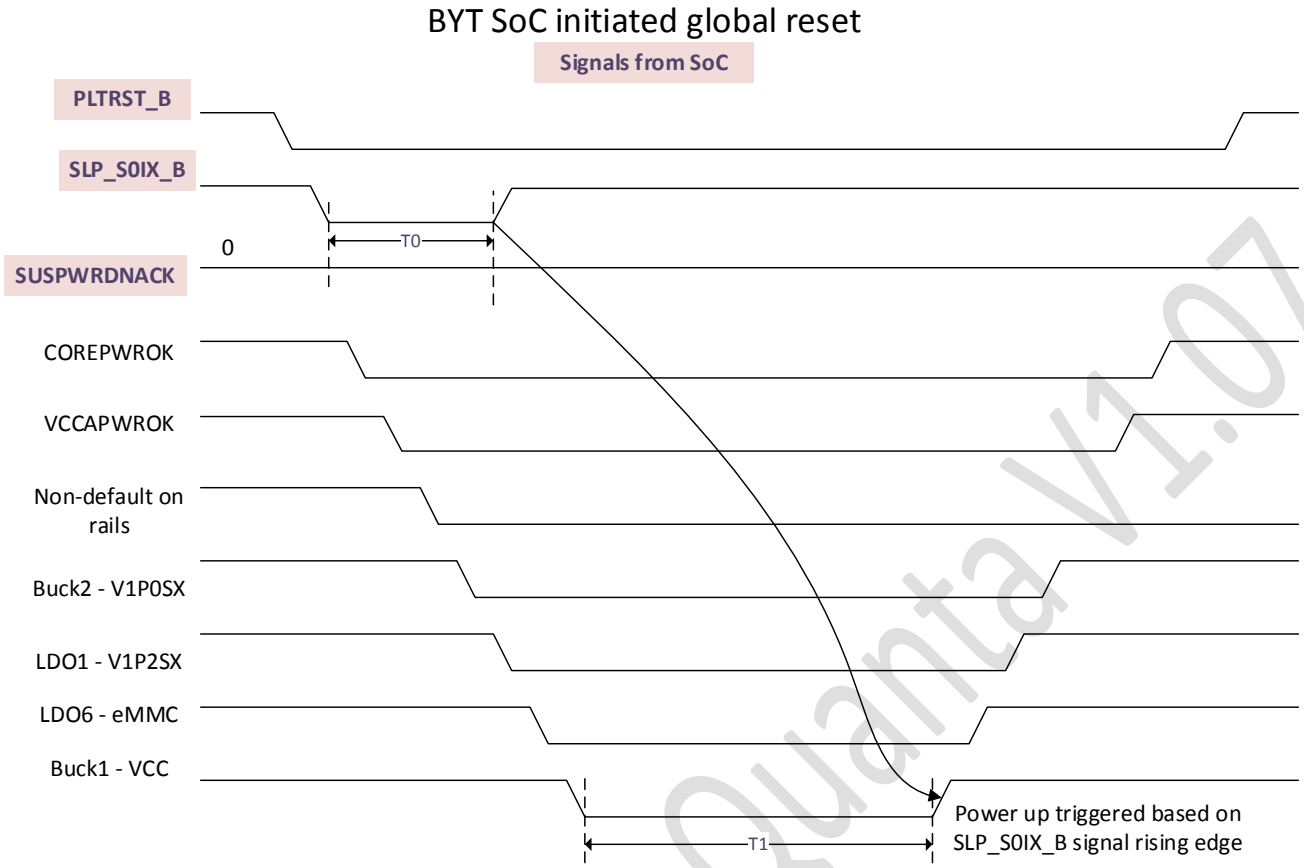

Figure 9-13

Note:

- Power down and power up timing follow cold off and cold boot timing
- Rail power up sequencing will wait until SLP_S0IX_B signal goes high to begin the sequence
- If SLP_S0IX_B signal goes high before power down sequence completes, power down sequence should complete before power up begins
- PLTRST_B to SLP_S0IX_B delay could be zero

Table 9-12

Parameter	Description	Min	Typical	Max	Units
T0	Time that the SLP_S0IX_B signal stays low	0.1		No max	ms
T1	Time for which rails stay down before power up sequence begins		50		ms

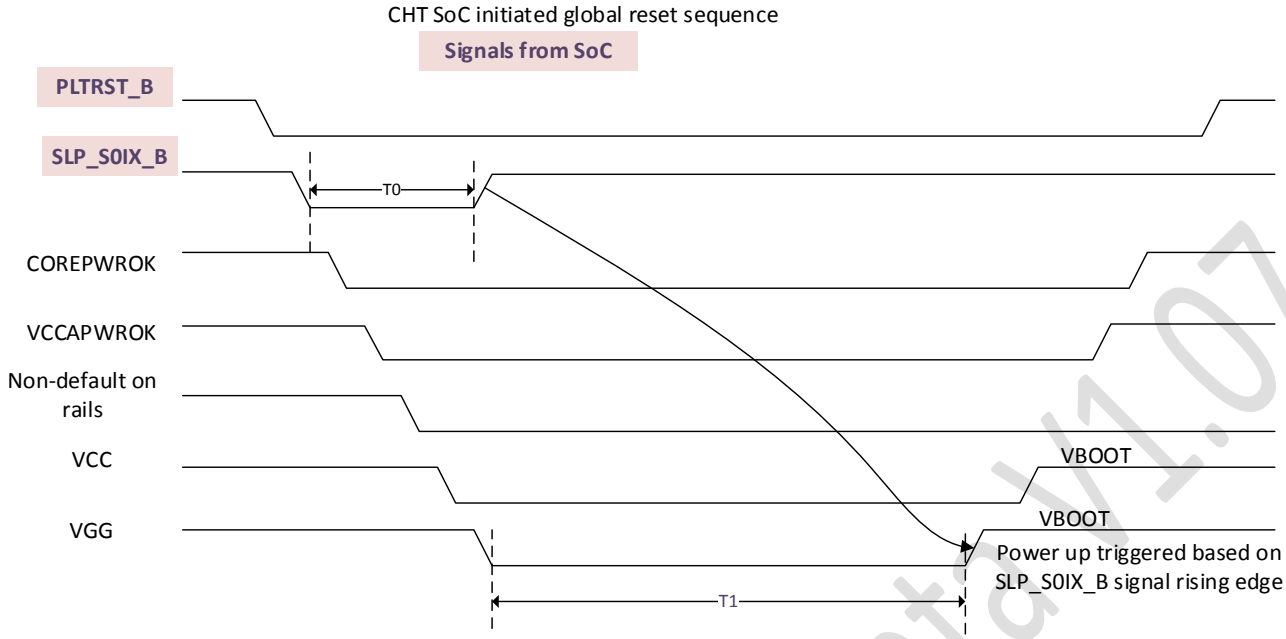

Figure 9-14

Note:

- Power down and power up timing follow cold off and cold boot timing
- Rail power up sequencing will wait until SLP_S0IX_B signal goes high to begin the sequence
- If SLP_S0IX_B signal goes high before power down sequence completes, power down sequence should complete before power up begins
- PLTRST_B to SLP_S0IX_B delay could be zero

Table 9-13

Parameter	Description	Min	Typical	Max	Units
T0	Time that the SLP_S0IX_B signal stays low	25		No max	ms
T1	Time for which rails stay down before power up sequence begins		50		ms

9.1.5 Sleep state control

Description:

1. Set the REG 9AH - REG 9EH

2. SOC set SLP_S0IX_B low, the power rails power down

3. SOC set SLP_S0IX_B high, the power rails power up

Default rail status

The following table is a list of the default on rails. The table also shows what the rail status is during sleep.

Table 9-14

Voltage Regulator	**Rail Function**	**Sleep State based on SLP_S0IX_B pin**	**Off State**
BUCK1	VCC	Off (based on register setting)	Off
BUCK2	V1P0SX (BYT) VNN (CHT)	BYT(Off), CHT(On) – based on register setting Reduced voltage based on register setting	Off
BUCK3	V1P0/V1P05/V1P15	Regulator is On Reduced voltage based on register setting	Off
BUCK4	VDDQ	On	Off
BUCK5	VNN (BYT) VGG (CHT)	BYT(On), CHT (Off) – based on register setting Reduced voltage based on register setting	Off
BUCK6	V1P8	On	Off
LDO1	V1P2SX (BYT) V1P2A (CHT)	Off	Off
LDO2	V1P2A (BYT)	On	Off
LDO3	V3P3A	On	Off
LDO4	VRTC	On	On
LDO5	VREFDQ	On	Off
LDO6	eMMC	On	Off
All other rails are controlled by the driver		Based on register control from the driver	Off

BYT Standby entry and exit sequence

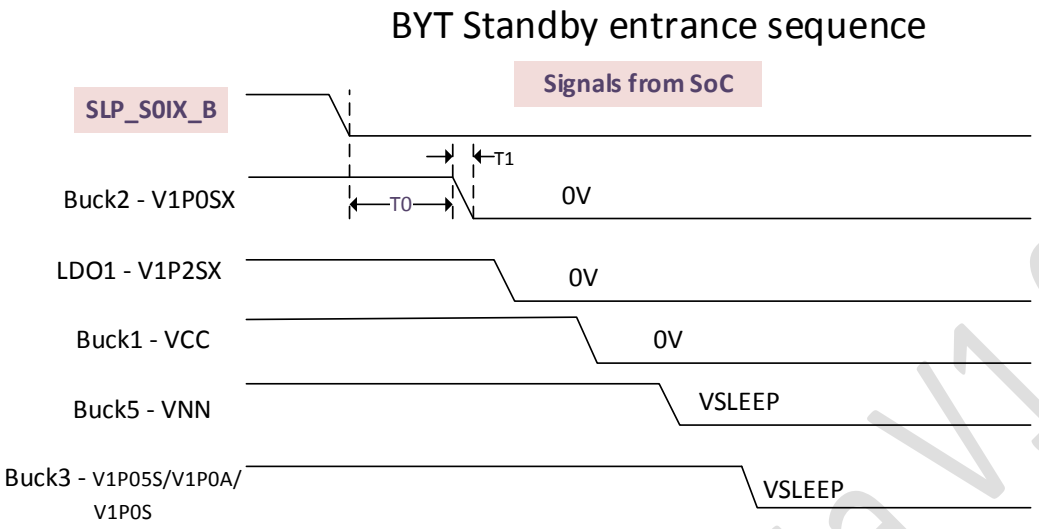

Figure 9-15

Table 9-15

Parameter	Description	Min	Typical	Max	Units
T0	SLP_S0IX_B assertion to first SX rail starts to turn off	0		100	µs
T1	Rail Ramp-down Time from 90% to 10% voltage level	0.5	1	2.0	ms
T2	Rail to Subsequent Rail Turn-Off Delay	0.5	1	3.0	ms

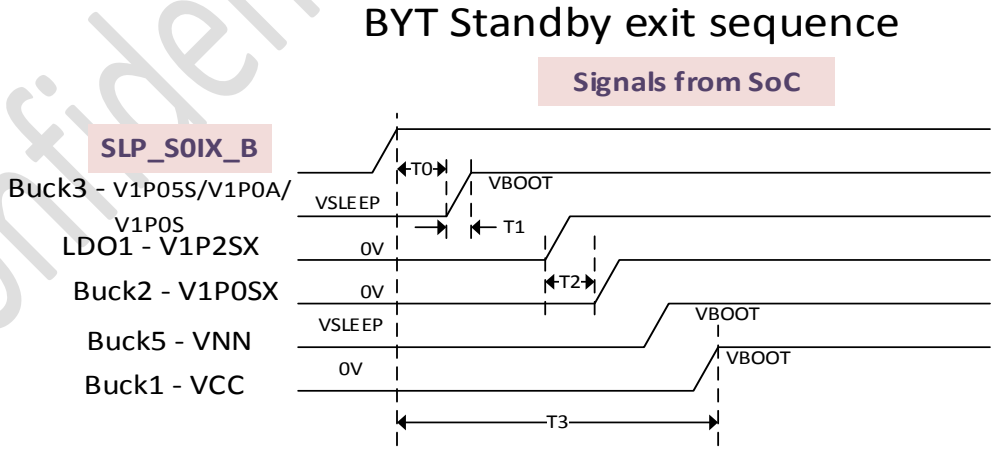

Figure 9-16

Table 9-16

Parameter	Description	Min	Typical	Max	Units
T0	SLP_S0IX_B de-assertion to first SX rail starts to turn on	0		100	µs
T1	Rail Ramp-Up Time from 10% to 90% voltage level		0.08	1	ms
T2	Rail to Subsequent Rail Turn-On Delay			1	ms
T3	Total S0IX exit latency: from SLP_S0IX_B de-assertion to all VRs are within its specified tolerance		0.2	4.1	ms

CHT Standby entry and exit sequence

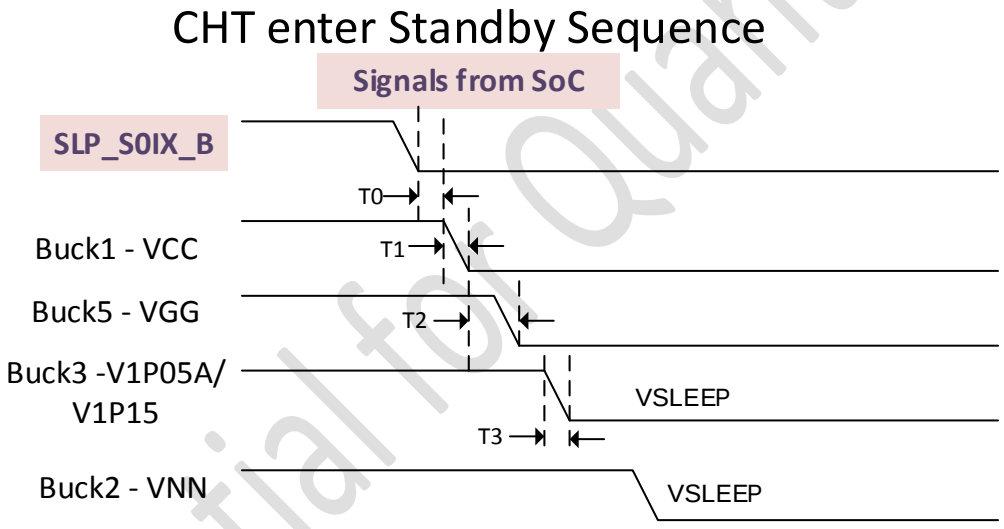

Figure 9-17

Table 9-17

Parameter	Description	Min	Typical	Max	Units
T0	SLP_S0IX_B assertion to voltage rail starts to ramp down	0		100	µs
T1	VR rail ramp-down time from 90% to 10% voltage level for all VRs unless specified otherwise	0.01	1	3.0	ms
T2	VR to subsequent VR turn-off delay for all VRs unless specified otherwise	0.1	1	3.0	ms
T3	Ramp down slew rate for BUCK3 to VSLEEP voltage	2.5		10	mv/µs

CHT exit Standby Sequence

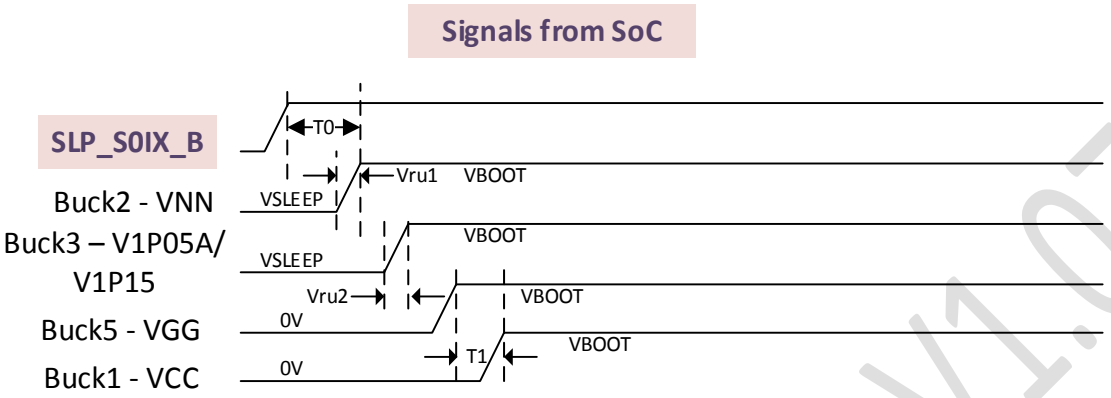

Figure 9-18

Table 9-18

Parameter	Description	Min	Typical	Max	Units
T0	SLP_S0IX_B assertion to voltage rail starts to ramp up	0	8	100	µs
T1	VR to subsequent VR Turn-On Delay for all VRs unless specified otherwise	0	0.08	1	ms
Vru1	Buck2 voltage ramp-up slew rate to VBOOT	2.5		10	mv/µs
Vru2	Buck3 voltage ramp-up slew rate to VBOOT	2.5		10	mv/µs

9.2 IPS (Intelligent Power Select)

AXP288 has Intelligent Power Select (IPS) to select the appropriate source to power the system. The output of IPS, IPSOUT will then be used as power source for downstream regulators and battery charger. For single input power source system, the power source needs to be connected to both VBUS power pins as shown in Figure 9-17.

9.2.1 IPS overview

Input Power Sources Block Diagram

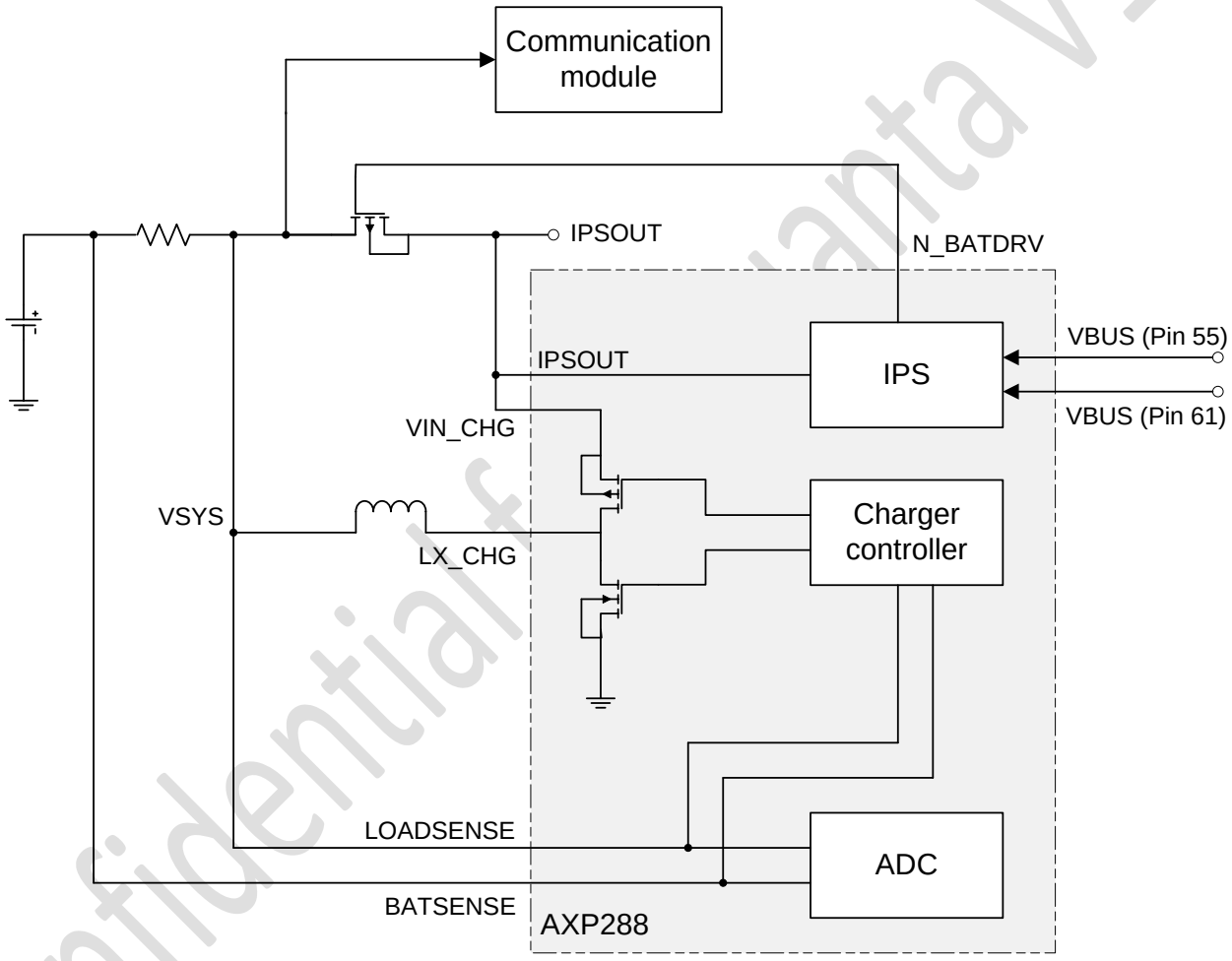

Figure 9-19

Single Input Power Source Connection Diagram

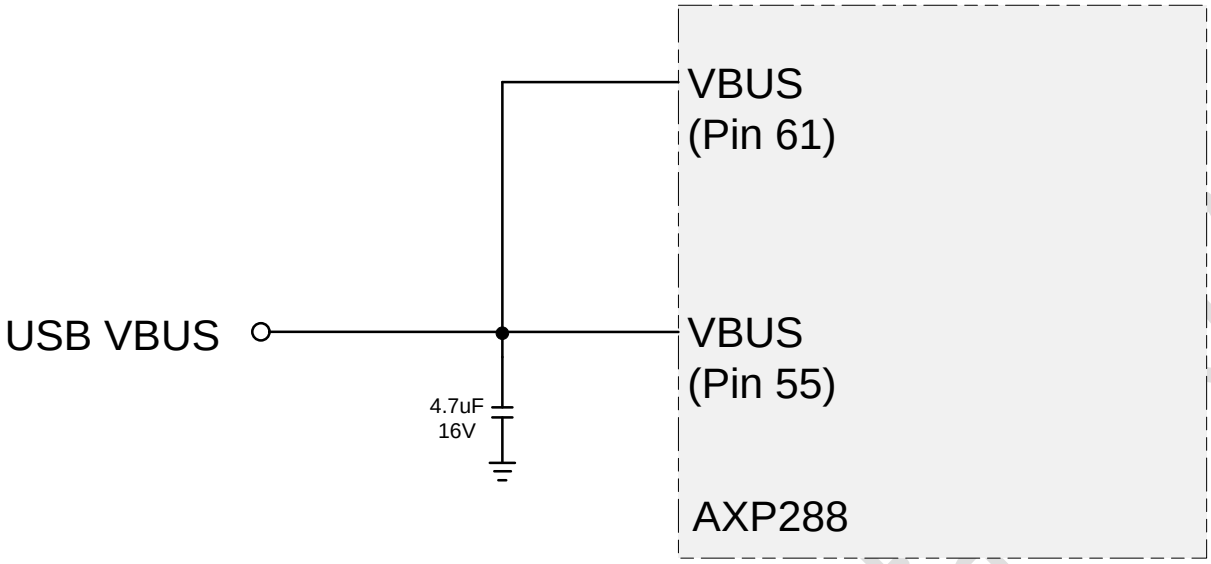

Figure 9-20

- If only Li- Battery is available, and no external power input, Li- Battery is used for power input;
- If external power is available (VBUS), it is preferred in power supply
- If Li- Battery is available, it will “Seamlessly” switch to Li- Battery once external power is removed
- If the current is still insufficient, charge current will be reduced to zero, and Battery is used for one of power sources

9.2.2 IPSOUT source selection

For single input power source, VBUS source is channeled to IPSOUT when REG 30H[7] is set to 0 (default). For whatever reason, if VBUS source need to be disconnected from IPSOUT, set REG 30H[7] to 1. Note that when BC Detection module is detecting, REG 2CH[2] = 1, VBUS to IPSOUT channel is OFF.

VBUS Select Setting

Table 9-19

REG 30H[7]	REG 2CH[2]	VBUS_SEL
0	0	1
1	X	0
X	1	0

Table 9-20

REG 30H	Description	R/W	Default
Bit 7	VBUS path select control (VBUS_SEL) when VBUS valid 0: VBUS path selected 1: VBUS path not selected	RW	0

Table 9-21

REG 2CH	Description	R/W	Default
Bit 2	**BC_status (BC Detection status)** 1: Detecting, this bit is set when BC Detection start 0: Detection complete	RW	0

Input Source Select Setting

Table 9-22

VBUS_SEL	REG 00H[4]	IPSOUT from
1	1	VBUS
0	1	VSYS
×	0	VSYS

Table 9-23

REG 00H	Description	R/W	Default
Bit4	Indication VBUS can be used or not	R	0

9.2.3 VBUS current/voltage limitation

VBUS input power source has minimum hold voltage (VHOLD) setting and current limit setting. When the input source voltage drops below its VHOLD setting, it is considered as not having sufficient power. IPS will limit the current draw automatically so that the input source voltage is hold to this minimum level.

VBUS VHOLD is set as max of VBAT+0.15V or 30H[5:3] whereas VBUS current limit can be set through REG 35H[7:4].

VHOLD minimum voltage value can be set through the REG30H:

Table 9-24

5	V_{HOLD} setting bit 2	000: 4.0V; 001: 4.1V; 010: 4.2V 011: 4.3V; 100: 4.4V; 101: 4.5V 110: 4.6V; 111: 4.7V	RW	1
4	V_{HOLD} setting bit 1		RW	0
3	V_{HOLD} setting bit 0		RW	0

VBUS current limit is set by REG35H[7:4]:

Table 9-25

7:4	VBUS current limit select when VBUS Current limited mode is enable 0000-100mA 0001-500mA 0010-900mA 0011-1500mA 0100-2000mA 0101-2500mA 0110-3000mA 0111-3500mA 1xxx-4000mA	RW	0001

For the case of battery charger detection enabled, once the USB charger detection is completed, VBUS current limit will be guided by the result of the detection. Subject to the type of USB charger detected, the current limit set in REG 35H[7:4] will be auto updated by the value set in REG 30H[1:0]. For example, if the BC detection result indicates SDP, the current limit in REG 35H[7:4] will be set to 500mA (900mA if it is USB 3). If the detected USB charger is CDP or DCP, the current limit in REG 35H[7:4] will then be updated according to the setting in REG 30H[1:0].

Table 9-26

REG 2FH[7:5]	Current limit	Description
SDP	500mA	USB connected. After communication, CPU can identify USB3.0,then change the current limit to 900mA
Other	REG30H[1:0]	

VBUS with the BC detection:

AXP288 has battery charger detection module that capable of detecting type of USB charger plug onto the port. Below is the battery charger detection flow.

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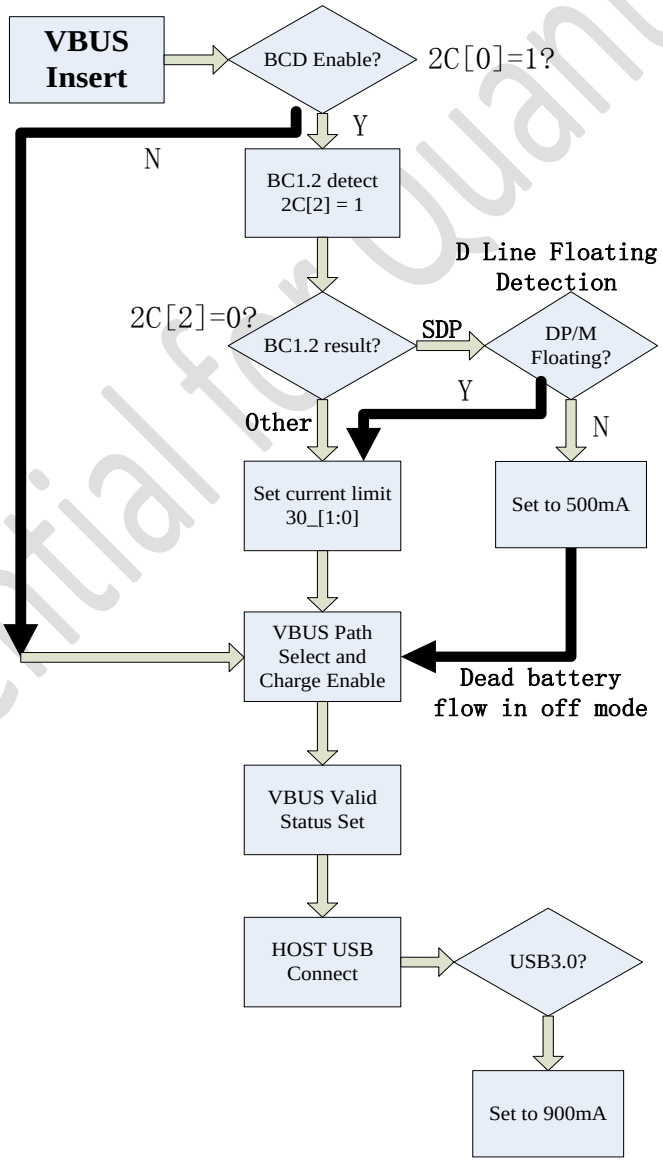


Figure 9-21

When REG 2CH[0] is set to 1, battery charger detection module will start to operate. Upon completion of the BC detection (REG 2CH[2] = 0), AXP288 will automatically update the detection result onto REG 2FH[7:5]. If the BC detection result indicate SDP, the current limit will be set to 500mA (900mA if it is USB 3) or else the current limit will follow the setting in REG 30H[1:0].

9.2.4 VBUS input overvoltage protection

VBUS to IPSOUT path have a regulator, target of 5.0V:

Table 9-27

Input power	**IPSOUT**	**CHGLED**	**Contents**
>7V	5V	Floating	PMIC shutdown
>6.3V	5V	2Hz toggle	Work normally
>5.06V	5V	Charge LED	
<5.06	Vin-0.06V	Charge LED	
<3.5V	Vin-0.06V	Charge LED	Invalid

9.2.5 VBUS insertion power up condition

The PMIC will start the boot sequence at the point of VBUS insertion. A VBUS insertion is detected from a rising voltage on the VBUS node as long as it is larger than 4.1V. The existence of VBUS is stored in REG 00H[5]. The charger will start charging immediately and automatically. If the battery level is above the battery boot threshold, the PMIC will continue the boot process, otherwise the charger will continue charging until the battery boot threshold is reached, at this point the PMIC will continue the boot process. Please refer to Section 9.1 for detail flow chart.

9.3 BC Detection Module

This section is primarily based on battery charging specification, for more information please refer to BC rev1.2 specifications. AXP288 is compatible with BC rev1.2 and can identify SDP/CDP/DCP except ACA The PMIC can detect the device type without software activity.

Table 9-28

Device	Description	Compatible
SDP	Standard Downstream Port	PMIC can identify
CDP	Charging Downstream Port	PMIC can identify
DCP	Dedicated Charging Port	PMIC can identify
ACA	Accessory Charger Adapter	PMIC can’t identify

Please refer to REG36H for detailed information.

9.4 Adaptive PWM Charger

The AXP288 battery charger solution has two charging modes that it can be in. It is specifically designed to charge Li Ion or Li Polymer type batteries. The two modes are 1) Pre Charge Mode and 2) Fast Charge Mode. The delineation between these two modes is based on the battery voltage level of V_{TRKL} which is set at 3.0V.

When battery voltage, $V_{BATSENSE}$ is between 0V to 3.0V (V_{TRKL}), the charger is in Pre Charge Mode where charging current is limited to a value of I_{TRKL} (10% of I_{CHRG}, default value is 120mA). This mode of operation is intended to prevent damage to the battery. Once $V_{BATSENSE} \geq V_{TRKL}$, the charger will enter Fast Charge Mode. The Fast Charge Mode can be subdivided into two phases, namely the constant current phase (CC) and the constant voltage phase (CV). The CC phase takes place when $V_{BATSENSE}$ is in between V_{TRKL} and V_{TRGT}. It will charge with constant I_{CHRG}. When $V_{BATSENSE}$ reach V_{TRGT}, charger will operate at CV phase. At this phase, charger will charge with constant voltage of V_{TRGT}.

9.4.1 Charger Overview

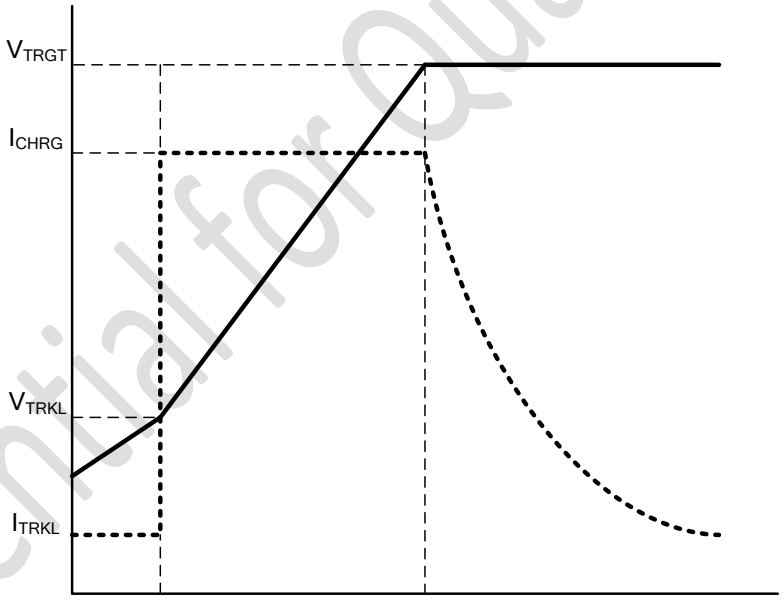


Figure 9-22

V_{TRGT} is programmed in REG 33H[6:5] and I_{CHRG} is in REG 33H[3:0] whereas V_{TRKL} is fixed at 3V and I_{TRKL} is set as 10% of I_{CHRG}.

9.4.2 Charging start and stop

When $V_{BATSENSE}$ is between 0V to 3.0V (V_{TRKL}), the charge operation will start when VBUS insert and REG 33H[7] is set to 1. The charging operation will cease when $V_{BATSENSE}$ is > $V_{TRGT-0.1V}$ and charging current < 10% of I_{CHRG}.

9.4.3 Timeout activity

Refer to REG 34H, there are 2 timers that can be programmed as charging expire time, REG 34H[7:6] for Pre Charge and REG 34H[1:0] for Fast Charge Mode. When the actual charge current is less than 20% of the ICHRG, the timer will automatically hold. When the timer expired, charger will no longer charge with programmed charging current. Instead, it will turn into safe mode. Under safe mode, charger will always charge the battery with 5mA until VBATSENSE > VTRGT – 0.1V. When the charger exits from safe mode, it will assert the IRQ. The safe mode status is reflected in REG 01H[3] and SOC can get the mode status through this bit.

Table 9-29

REG 34H Bit	Description		R/W	Default
7	Pre-charge Timer length setting 1	00: 40 minutes; 01: 50 minutes; 10: 60 minutes; 11: 70 minutes.	RW	0
6	Pre-charge Timer length setting 0		RW	1
1	Fast charge maximum time setting 1	00: 6 hours; 01: 8 hours; 10: 10 hours; 11: 12 hours.	RW	0
0	Fast charge maximum time setting 0		RW	1

Table 9-30

REG 01H	Description	R/W	Default
Bit3	Indicate battery active mode 0-charger is not in battery active mode 1-charger is in battery active mode	R	

There are two ways to reset or exit from safe mode. One is plug out and re-insert the input power source or toggle charger enable bit.

9.4.4 CHGLED activity

AXP288 provides CHGLED pin. The LED connected to this pin can be used to indicate charger status and input power sources over voltage alarm. There are two Charge LED modes that can be configured through REG 34H[4] if REG 32H[3] is set to 1.

Table 9-31

REG 34H	Description	R/W	Default
Bit 4	CHGLED Mode select when REG 32H[3] is 1 0: Type A; 1: Type B	RW	0

Table 9-30

REG 32H	Description		R/W	Default
Bit 5-4	CHGLED pin control	00: Hi-Z 01: 25% 0.5Hz toggle	RW	00

		10: 25% 2Hz toggle 11: drive low		
Bit 3	CHGLED pin control	0: controlled by REG 32H[5:4] 1: controlled by Charger	RW	0

Charge LED indicator

Table 9-32

CHGLED pin	Mode A	Mode B
Z (tri-state)	Not charging	Not charging due to 1. no external power source or 2. external power source is insufficient and battery is discharging
25% duty 1Hz (Z/Low)	Abnormality alarm due to 1. charger timeout or 2. IC temperature > warning level 2)	Charging
25% duty 4Hz (Z/Low)	Overvoltage alarm (VBUS > 6.3V)	Alarm due to 1. VBUS > 6.3V or 2. charger timeout or 3. IC temperature > warning level 2)
Low	Charging	Not charging due to battery is fully charged

9.4.5 Battery detection

When the VBATSENSE<2.2V, AXP288 judge it as battery is not present. When VBATSENSE goes higher than 2.2V, it indicates battery present or is inserted. For the case of battery insertion or removal, IRQ will be asserted. Battery presence status is indicated in REG01H[5]and the battery detection function can be set by REG 32H[6]. When charger insert, AXP288 will send a pulse to detect battery is present or not per 16 seconds.

9.4.6 Temperature protection

AXP288 has built in thermal protection for the IC itself with 3 levels of warning. Each warning level has 6.3℃ different in threshold compare to the next level and each warning level has hysteresis gap of 13.6˚C. Below are the charger responses with respect to each thermal warning level.

Table 9-33

Warning	AXP288 Response
Level 1	Once the IC temperature exceeds this level, charger will charge at minimum charging current. When IC temperature drops below hysteresis limit, charger will automatically go back to its original charging state.
Level 2	If IC temperature continue to rise and exceeds this level, charger will continue to charge at minimum charging current. Charge LED will provide indication according to **Table 9-31**. If IRQ is enabled in REG43H[7], IRQ will be asserted and its status can be read from REG 01H[7].
Level 3	If IC temperature exceeds this level, all the behavior is the same as level 2 but if REG8FH[2] is set to 1, IC will automatically shut down.

Table 9-34

REG 43H Bit	**Description**	**R/W**	**Default**
7	The PMIC temperature over the warning level 2 IRQ (OTIRQ) enable	RW	0

Table 9-35

REG 01H Bit	**Description**	**R/W**	**Default**
7	Indication PMIC die over temperature or not 0: not over temperature; 1: over temperature	R	0

Table 9-36

REG 8FH	**Description**	**R/W**	**Default**
Bit 2	The PMIC shut down or not when Die temperature is over the warning level 3 0-not shut down 1-shut down	RW	0

Beside built in IC thermal protection, AXP288 has the capability to sense one external thermal sensor (for battery temperature) through TS pin.

Block Diagram for Battery Temperature Measurement

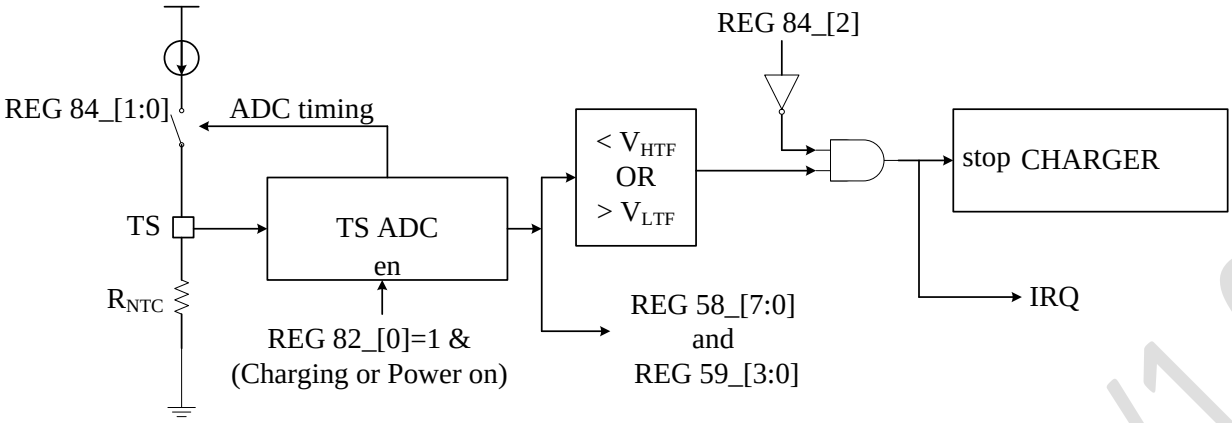


Figure 9-23

AXP288 has built in current source that can be used to inject to external thermal sensor thru TS pin for temperature reading. This current source has 4 level of current which can be programmed through REG 84H[5:4]. By default, the current source will only be injected when ADC is going to read the temperature data. The ADC to read TS pin input is enabled by setting REG 82H[0] to 1. However the current source switch can be programmed to always OFF or ON or only ON when charger is charging through REG 84H[1:0].

Table 9-38

REG 84H Bit	Description		R/W	Default
5-4	Current source from TS pin control: 00: 20uA; 01: 40uA; 10: 60uA; 11: 80uA		RW	11
1-0	Current source from TS pin on/off enable bit [1:0]	00: off 01: on when charging battery, off when not charging 10: on in ADC phase and off when out of the ADC phase, for power saving 11: always on	RW	10

Table 9-39

REG 82H Bit	Description		R/W	Default
0	TS pin input to ADC enable	0: off, 1: on	RW	0

When the current source is injected to thermal sensor (NTC), it will create a voltage drop across NTC and this voltage will be read by 12 bits ADC thru TS pin. The 12 bits code output of the ADC will then be stored in REG 58H (HSB 8) & REG 59H (LSB 4). The relation of TS pin voltage to 12 bits ADC output code is as below:

12 bits ADC output code = R_NTC(Ω) * REG 84[5:4](μA) / (0.8 * 10^3).

Table below is the example by using 10K NTC from Murata (NCP15XH103F03R).

Table 9-40

Temperature (˚C)	R_NTC (Ω)	TS Pin Voltage (V)	12 bits ADC output code	
			REG 58H[7:0]	REG 59H[3:0]
-10	40260	3.221	FBH	AH
0	26490	2.119	A5H	8H
25	10000	0.800	3EH	8H
40	5840	0.467	24H	7H
45	4924	0.394	1EH	CH
55	3550	0.284	16H	3H

There are 2 battery over temperature (OTP) and 2 under temperature (UTP) thresholds can be set to protect the battery by either controlling the charger or shutdown the system. The first level OTP & UTP thresholds are programmed by REG 38H & REG 39H. The second level OTP & UTP threshold are programmed by REG 3CH & REG 3DH. When battery temperature is higher or lower than the first level OTP or UTP threshold, IRQ is asserted, charger will stop charging and REG 01H[6] change to 0 to reflect the status. When battery temperature is higher or lower than the second level OTP or UTP threshold, IRQ is asserted. System may or may not shutdown subject to SW decision. There is a hysteresis of 460.8 mV(refer to TS pin voltage) for UTP threshold, and there is a hysteresis of 57.6 mV for OTP threshold. Every time when the battery temperature comes out from first level over or under temperature, IRQ is asserted. Charger restores the original charging state and REG 01H[6] change to 1. In normal case, first level of OTP & UTP thresholds should be set within the second level OTP & UTP thresholds.

Using TS pin current source and obtain TS pin data of the following table:

Table 9-41

Usage condition	setting	Key point
Don't need temperature protection	TS = GND，REG 84H[1:0] = 00，（default 00），REG84H[2] = 1	TS work as GPADC
Temperature protection when in charger	REG 84H[1:0] = 01	Current source on when charging
Temperature protection when in charging and discharging	REG 84H[1:0] = 10	
TS for GPADC or GPIO	REG 84H[1:0] = 11 when need current source REG 84H[1:0] = 00 when not need current source	

Logic Table：

Table 9-42

REG84H[2] Function	REG82H[0] ADC Enable	REG84H[1:0] Current	Work mode	IRQ	Note
0	0	xx	TS	NO	
0	1	00	TS	NO	
0	1	01	TS	IRQ when in Charging	all IRQ work
0	1	10/11	TS	IRQ all times	
1	0	xx	GPADC	NO	TS function disable

9.5 Multi-Power Outputs

BUCK1-6 are dual mode (PFM / PWM), by default is auto switch mode. All Buck and PWM charger are synchronized with frequency of 3MHz (with spread spectrum option), hence small value external inductors and capacitors components can be used.

All Buck and LDO have current limiting protection function. When the load current exceeds the current limit, the output voltage will drop. Meanwhile, all of the Buck output voltage will be monitored. If the Buck output voltage is 15% lower than the set value and BUCK 85% low voltage turn off PMIC function (REG 81H) is enabled, PMIC will automatically force a shutdown and PWROK pin becomes low. Buck output voltage monitor de-bounce time setting is available at REG 8EH[7:6].

BUCK1-5 has DVM enable option. In DVM mode, when there is a change in the output voltage, BUCK will change to the new targeted value step by step. If the application does not require use of any Buck, the LX pin can be left floating while VIN and PGND need to be connected. PMIC will automatically detect this state to turn off the Buck.

Table 9-43

X-Powers	Intel	Input	Default Voltage	Max Current	Default State	Application
BUCK1	BUCK1	IPSOUT	1.0V	3A	on	VCC
BUCK2	BUCK2	IPSOUT	1.0V	1.8A	on	V1P0SX (BYT), VNN (CHT)
BUCK3	BUCK3	IPSOUT	1.0V	2.5A	on	V1P0/1P05/A/S
BUCK4	BUCK4	IPSOUT	1.5/1.36/1.24V	2.5A	on	VDDQ
BUCK5 (Dual Phase)	BUCK5	IPSOUT	1.0V	6A	on	VNN (BYT), VGG CHT)
BUCK6	BUCK6	IPSOUT	1.8V 3.3V(only for	1.5	on	V1P8A/S V3P3A(only for

			AXP288D)			AXP288D)
ELDO1		IPSOUT	1.8V	0.4A	on	V1P8A(only for AXP288D)
ALDO3	LDO3	IPSOUT	3.3V	0.2A	on	V3P3A/S
FLDO1	LDO1	>1.2V	1.25V	0.3A	on	V1P2SX
FLDO2	LDO2	>1.2V	1.25V	0.1A	on	V1P2A/S
FLDO3	LDO5	>1.2V	V_{BUCK4}/2	0.03A	on	VREFDQ
RTCLDO	LDO4	IPSOUT	3.0V	60mA	Always on	RTC

Both VINT and VCC_RTC input from IPSOUT. As long as any of the VBUS or BAT power exists, they will not power down. VINT output is fixed at 1.8V, while VCC_RTC is fixed at 3.0V.

9.6 ADC

PMIC has a 12Bit SAR ADC. The ADC input range is 0V to 2.0475V, with is 0.5mV/step. Voltage and current ADC has sampling frequency option of 800/400/200/100Hz. The relationship between input signal and data is listed below:

Table 9-44

Channel function	**000H**	**STEP**	**FFFH**	**Condition**
BAT voltage (BATSENSE)	0mV	1.1mV	4.5045V	Power On
Current offset	0mA	1mA	4.095A	Charging or power on
BAT discharge current	0mA	1mA	4.095A	Power on
Internal temperature				Charging or Power on
BAT charge current	0mA	1mA	4.095A	Charging or Power on
TS pin input	0mV	0.8mV	3.276V	Charging or Power on
GPIO0 pin input	0mV	0.8mV	3.276V	Power On

Current ADC measured the current through the 10mohm resistor between BATSENSE and LOADSENSE. For internal temperature, internal logic will do the ADC data comparison with register set warning level for sending over-temperature alarm or shutdown. To identify the battery current direction, the charge current and discharge current value will be compare base on status of charger enable, battery present and VBUS present indication.

9.7 Fuel Gauge

The Fuel Gauge comprises 3 modules – Rdc calculation module; OCV (Open Circuit Voltage) and Coulomb counter module; and calibration module. The Fuel Gauge system is able to export information about battery to application such as Battery capacity percentage (REG B9H), Battery Voltage (REG 78H, REG 79H), Battery charging current (REG 7AH, REG 7BH), Battery discharge current (REG 7CH, REG 7DH), Battery maximum capacity (REG E0H, REG E1H), Battery Rdc value (REG BAH, REG BBH).

The Fuel Gauge can be enabled or disabled via REG B8H. The Battery low warning can be set in REG E6, and IRQ (REG 4BH) will be sent out to alert the platform when the battery capacity percentage is lower than the warning level set in REG E6H.

Once a default battery is selected for a particular design, it is highly recommended to calibrate the battery to achieve better Fuel Gauge accuracy. The calibration procedure is documented in separate Application Guide – **AXP288 Battery Calibration Application Guide**. Once the calibration data are available, user can write the calibration info to the following register – REG C0H – DFH (OCV percentage table) on each boot. Or user can choose not to do the calibration and use the default OCV percentage value. Additionally, the Fuel Gauge system is capable to learn the battery characteristic on each Full charge cycle. Information such as Battery Maximum capacity (REG E0H, REG E1H) and Rdc (REG BAH, REG BBH) will be updated automatically over time.

OCV Percentage Table

Table 9-45

Reg Address	Percent	OCV
	0	2.9920
C0	RW(H)	3.1328
C1	RW(H)	3.2736
C2	RW(H)	3.3440
C3	RW(H)	3.4144
C4	RW(H)	3.4848
C5	RW(H)	3.5552
C6	RW(H)	3.5904
C7	RW(H)	3.6080
C8	RW(H)	3.6256
C9	RW(H)	3.6432
CA	RW(H)	3.6608
CB	RW(H)	3.6960
CC	RW(H)	3.7312
CD	RW(H)	3.7664
CE	RW(H)	3.8016
CF	RW(H)	3.8192
D0	RW(H)	3.8368
D1	RW(H)	3.8544
D2	RW(H)	3.8720
D3	RW(H)	3.9072
D4	RW(H)	3.9424
D5	RW(H)	3.9776
D6	RW(H)	4.0128
D7	RW(H)	4.0480
D8	RW(H)	4.0832
D9	RW(H)	4.1184
DA	RW(H)	4.1360
DB	RW(H)	4.1536
DC	RW(H)	4.1888
DD	RW(H)	4.224
DE	RW(H)	4.2592

DF	RW(H)	4.2944
	100	4.3296

9.8 Interrupt Controller

PMIC Interrupt Controller monitors such as low power, bad battery, PWRON pin signal, over temperature, GPIO input edge signals such as trigger events. When the events occur, corresponding IRQ status will be set to 1, and will drive IRQ pin (NMOS open drain) asserted low. When host detect triggered IRQ signal, host will scan through the trigger events and respond accordingly. Meanwhile, Host will reset the IRQ status by writing "1" to status bit. Host will always check every IRQ status from time to time and only will take effect with respective relevant enabled IRQ bit only.

The input edge IRQ of GPIO will only functions when GPIO pin is set as Digital input, and the function will take effect when input edge IRQ is enable . The input will go through about 1ms of de-bounce and corresponding IRQ will trigger when detect rising and falling edge. Rising, falling, or both edge triggering is control by corresponding IRQ register bit.

8bits event timer will issue timeout IRQ. Clearing IRQ doesn't start counter.

9.9 TWSI

The PMIC is compatible with a host-controlled environment, functioned as a slave port enabling serial interface compatible hosts to write to or read from internal registers. The PMIC only responds (ACK) to address 68H/69H.

Table 9-46

BYTE	BIT							
	MSB	6	5	4	3	2	1	0
WRITE	0	1	1	0	1	0	0	0
READ	0	1	1	0	1	0	0	1
I/O DATA BUS	B7	B6	B5	B4	B3	B2	B1	B0

Incremental Read:

The PMIC support incremental read operations in normal TWI mode. The address increases by 1 automatically.

10 Register

Note: hereinafter, "system reset" means that the Register will be reset when the PMIC power off, and "power on reset" means that the Register will be reset when IPSOUT voltage drop below 2.1V .

Register List

Table 10-1

Address	Description	R/W	Default
00	Power source status	R	
01	Power mode and Charger status	R	
02	Power up/down reason register	RW	
03	IC type number	R	51H
04-0F	12 Data buffers	RW	00H
10	Output power on-off control 1	RW	XXH
12	Output power on-off control 2	RW	08H
13	Output power on-off control 3	RW	9CH
14	On/Off synchronous control	RW	48H
15	DLDO1 voltage control	RW	16H
16	DLDO2 voltage control	RW	16H
17	DLDO3 voltage control	RW	16H
18	DLDO4 voltage control	RW	1AH
19	ELDO1 voltage control	RW	00H
1A	ELDO2 voltage control	RW	00H
1B	ELDO3 voltage control	RW	00H
1C	FLDO1 voltage control	RW	0BH
1D	FLDO2/3 voltage control	RW	0BH
20	BUCK6 voltage control	RW	02H
21	BUCK5 voltage control	RW	B2H
22	Reserved	RW	XXH
23	BUCK1 voltage control	RW	B2H
24	BUCK4 voltage control	RW	XXH
25	BUCK3 voltage control	RW	B2H
26	BUCK2 voltage control	RW	B2H
27	BUCK1/2/3/4/5 DVM control	RW	XCH
28	ALDO1 voltage control	RW	17H

Address	Description	R/W	Default
29	ALDO2 voltage control	RW	17H
2A	ALDO3 voltage control	RW	1AH
2C	BC Module Global Register	RW	00H
2D	BC Module VBUS Control and Status Register	RW	30H
2E	BC USB Status Register	RW	00H
2F	BC Detect Status Register	R	20H
30	VBUS path control & Hold voltage setting	RW	21H
31	Power wakeup control & V_{OFF} setting	RW	03H
32	Power Disable, BAT detect and CHGLED pin control	RW	4XH
33	Charger Control 1	RW	CXH
34	Charger Control 2	RW	45H
35	Charger Control 3	RW	18H
36	POK setting	RW	59H
37	POK Power off activity time setting	RW	00H
38	$V_{LTF\text{-}charge}$ setting	RW	A5H
39	$V_{HTF\text{-}charge}$ setting	RW	1FH
3A	Reserved	RW	XXH
3B	BUCK frequency setting	RW	08H
3C	$V_{LTF\text{-}work}$ setting	RW	FCH
3D	$V_{HTF\text{-}work}$ setting	RW	16H
3E	Reserved	RW	XXH
40	IRQ enable 1	RW	D8H
41	IRQ enable 2	RW	FFH
42	IRQ enable 3	RW	FFH
43	IRQ enable 4	RW	03H
44	IRQ enable 5	RW	7CH
45	IRQ enable 6	RW	00H
48	IRQ Status 1	RW	00H
49	IRQ Status 2	RW	00H
4A	IRQ Status 3	RW	00H
4B	IRQ Status 4	RW	00H
4C	IRQ Status 5	RW	00H
4D	IRQ Status 6	R	00H
58	TS pin input ADC data, highest 8bit	R	00H
59	TS pin input ADC data, lowest 8bit	R	00H
5A	GPIO0 pin input ADC data, highest 8bit	R	00H
5B	GPIO0 pin input ADC data, lowest 8bit	R	00H

Address	Description	R/W	Default
78	Average data bit[11:4] for Battery voltage (BATSENSE)	R	00H
79	Average data bit[3:0] for Battery voltage (BATSENSE)	R	00H
7A	Average data bit[11:4] for Battery charge current	R	00H
7B	Average data bit[3:0] for Battery charge current	R	00H
7C	Average data for Battery discharge current highest 8 bit	R	00H
7D	Average data for Battery discharge current lowest 4 bit	R	00H
80	BUCK PWM/PFM mode select	RW	80H
81	Off-Discharge and Output monitor control	RW	FFH
82	ADC Enable	RW	E1H
84	ADC speed setting, TS pin Control	RW	F2H
85	ADC speed setting	RW	B0H
8A	Timer control	RW	00H
8E	Buck output voltage monitor de-bounce time setting	RW	00H/00H/40H
8F	IRQ pin, hot-over shut down	RW	00H
90	GPIO0(GPADC) control	RW	07H
91	GPIO0LDO and GPIO0 high level voltage setting	RW	1AH
92	GPIO1 control	RW	07H
93	GPIO1LDO and GPIO1 high level voltage setting	RW	1AH
94	GPIO signal bit	R	00H
97	GPIO pull down control	RW	00H
9A	Run time Sleep power up sequence 1	RW	00H
9B	Run time Sleep power up sequence 2	RW	00H
9C	Run time Sleep power down sequence 1	RW	00H
9D	Run time Sleep power down sequence 2	RW	00H
9E	Power rail mode in Sleep state	RW	00H
A0	Real time data bit[11:4] for Battery voltage (BATSENSE)	R	00H
A1	Real time data bit[3:0] for Battery voltage (BATSENSE)	R	00H
B8	Fuel Gauge Control	RW	E8H
B9	Battery capacity percentage for indication	R	64H
BA	RDC 1	RW	80H
BB	RDC 0	RW	5DH
BC	OCV 1	R	00H
BD	OCV 0	R	X0H
E0	Battery maximum capacity	RW	00H
E1	Battery maximum capacity	RW	00H
E2	Coulomb meter counter	RW	00H
E3	Coulomb meter counter	RW	00H

E4	OCV Percentage of battery capacity	R	64H
E5	Coulomb meter percentage of battery capacity	R	64H
Address	**Description**	**R/W**	**Default**
E6	Battery capacity percentage warning level	RW	A0H
E8	Fuel gauge tuning control 0	RW	00H
E9	Fuel gauge tuning control 1	RW	00H
EA	Fuel gauge tuning control 2	RW	00H
EB	Fuel gauge tuning control 3	RW	00H
EC	Fuel gauge tuning control 4	RW	00H
ED	Fuel gauge tuning control 5	RW	00H

REG 00H: Power source status

Table 10-2

Bit	Description	R/W
7	Reserved	R
6	Reserved	R
5	VBUS presence indication 0- VBUS not presence （VBUS<3.5V） 1- VBUS presence （VBUS>4.1V）	R
4	Indication of VBUS valid (VBUS_Val)	R
3	VBAT>3.5V or not	R
2	Indication Battery current direction 0: Battery discharge 1: Charging battery	R
1	Reserved	R
0	STARTUP_TRIGGER: indicate the startup trigger is VBUS or not 0: startup trigger is not VBUS; 1: startup trigger is VBUS	R

REG 01H: Power mode and Charger status

Table 10-3

Bit	Description	R/W
7	Indication PMIC die over temperature or not 0-not over temperature; 1-over temperature	R
6	Charging indication	R

	0-Charger is not charging or charging is done; 1-Charger is charging	
5	Battery presence indication 0-No Battery is connected to AXP288; 1-Battery is connected	R
4	REG 01H[5] valid flag 0- REG 01H[5] is invalid 1- REG 01H[5] is valid Indicate whether Battery detected or not yet	R
3	Indicate battery safe mode 0-charger is not in battery safe mode; 1-charger is in battery safe mode	R
2:0	Reserved	R

REG 02H: Power up/down reason register

Reset: Power on reset

Table 10-4

Bit	Description	R/W	Default
7	Power on key override was the shutdown reason, write 1 to clear	R/W	0
6	SOC initiated cold off was the shutdown reason, write 1 to clear	R/W	0
5	PMIC UVLO threshold was the shutdown reason, write 1 to clear	R/W	0
4	Cold reset was the start up reason, write 1 to clear	R/W	0
3	SOC initiated Global Reset was the start up reason, write 1 to clear	R/W	0
2	Battery insertion was the start up reason, write 1 to clear, write 1 to clear	R/W	0
1	Charger insertion was the start up reason, write 1 to clear	R/W	0
0	Power on key was the start up reason, write 1 to clear	R/W	0

REG 03H: IC type no.

Default: 51H

Table 10-5

Bit	Description	R/W
5-4	Reserved	R
7-6 & 3-0	IC type No. 010001: IC is AXP288 Others: Reserved	R

REG 04-0FH: 12 Data buffers

Default: 00H

Reset: Power on reset

Note: As long as one of the external powers, batteries or backup batteries exists, this data will be reserved and free from the startup and shutdown influence.

REG 10H: Output power on-off control 1

Default：XXH

Reset: system reset

Table 10-6

Bit	Description		R/W	Default
7	Reserved			
6	BUCK2 on-off control	0-off; 1-on	RW	1
5	BUCK3 on-off control	0-off; 1-on	RW	1
4	BUCK4 on-off control	0-off; 1-on	RW	1
3	BUCK1 on-off control	0-off; 1-on	RW	1
2	Reserved			
1	BUCK5 on-off control	0-off; 1-on	RW	1
0	BUCK6 on-off control	0-off; 1-on	RW	1

REG 12H: Output power on-off control 2

Default：08H

Reset: system reset

Table 10-7

Bit	Description		R/W	Default
7	Reserved			
6	DLDO4 on-off control	0-off; 1-on	RW	0
5	DLDO3 on-off control	0-off; 1-on	RW	0
4	DLDO2 on-off control	0-off; 1-on	RW	0

3	DLDO1 on-off control	0-off; 1-on	RW	1
2	ELDO3 on-off control	0-off; 1-on	RW	0
1	ELDO2 on-off control	0-off; 1-on	RW	0
0	ELDO1 on-off control	0-off; 1-on	RW	0

REG 13H: Output power on-off control 3

Default：9CH

Reset: system reset

Table 10-8

Bit	Description		R/W	Default
7	ALDO3 on-off control	0-off; 1-on	RW	1
6	ALDO2 on-off control	0-off; 1-on	RW	0
5	ALDO1 on-off control	0-off; 1-on	RW	0
4	FLDO3 on-off control	0-off; 1-on	RW	1
3	FLDO2 on-off control	0-off; 1-on	RW	1
2	FLDO1 on-off control	0-off; 1-on	RW	1
1-0	Reserved			

REG 14H: On/Off synchronous control

Default：48H

Reset: system reset

Table 10-9

Bit	Description	R/W	Default
7	Global reset act as cold reset Enable bit 0:Disable 1:Enable All power rails power down and then power up,64ms delay	RW	0
6	BUCK5 poly-phase control 0：no poly-phase 1：dual phase	RW	1
5	BUCK 3 & 4 change to poly-phase Buck 0: BUCK 3 & 4 is independent, not poly-phase Buck 1: BUCK 3 & 4 is poly-phase Buck	RW	0

4	Select the BUCK2/ 3 /5 Vrun register or Vsleep register 0:Vrun Register 1:Vsleep Register		RW	0
3	If SLP_S0IX_B go high and PLTRST_B status is low for 512ms, PMIC will do a cold reset or not (Reset: power on reset) 0: don't cold reset 1: do a cold reset		RW	1
2	Cold reset Enable set bit 0:Disable 1:Enable All power rails power down and then power up,64ms delay		RW	0
1	Power control register select	1-select buffer register, output value of control register to buffer 0-select the control register	RW	0
0	Output buffer register value	1-outport to control register from buffer Bit[1:0], self clear to 0 after output	RW	0

REG 15H: DLDO1 voltage control

Default：16H

Reset: System reset

Table 10-10

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 2.9V 0.7V-3.3V, 100mV/step	RW	16H

REG 16H: DLDO2 voltage control

Default：16H

Reset: System reset

Table 10-11

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 2.9V 0.7V-3.4V, 100mV/step	RW	10110

	3.4V-4.2V, 200mV/step		

REG 17H: DLDO3 voltage control

Default：16H

Reset: System reset

Table 10-12

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 2.9V 0.7V-3.3V, 100mV/step	RW	10110

REG 18H: DLDO4 voltage control

Default：1AH

Reset: System reset

Table 10-13

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 3.3V 0.7V-3.3V, 100mV/step	RW	11010

REG 19H: ELDO1 voltage control

Default：00H (16H for AXP288D)

Reset: System reset

Table 10-14

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0 0.7-1.9V, 50mV/step	RW	00000 (10110 for AXP288D)

REG 1AH: ELDO2 voltage control

Default：00H

Reset: System reset

Table 10-15

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0 0.7-1.9V, 50mV/step	RW	00000

REG 1BH: ELDO3 voltage control

Default：00H

Reset: System reset

Table 10-16

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0 0.7-1.9V, 50mV/step	RW	00000

REG 1CH: FLDO1 voltage control

Default：0BH

Reset: System reset

Table 10-17

Bit	Description	R/W	Default
7-4	Reserved	RW	000
3-0	voltage setting Bit 3-0, default is 1.25V 0.7-1.45V, 50mV/step	RW	BH

REG 1DH: FLDO2/3 voltage control

Default：0BH

Reset: System reset

Table 10-18

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4	FLDO3 voltage setting 0:BUCK4 / 2 1:FLDOIN/2	RW	0
3-0	FLDO2 voltage setting Bit 3-0, default is 1.25V 0.7-1.45V, 50mV/step	RW	BH

REG 20H: BUCK6 voltage control

Default：02H (11H for AXP288D)

Reset: System reset

Table 10-19

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, 1.6-3.4V, 100mV/step, default is 1.8V (3.3V for AXP288D)	RW	02H (11H for AXP288D)

REG 21H: BUCK5 voltage control

Default：B2H

Reset: System reset

Table 10-20

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 1.0V 0.50-1.20V：10mV/step 1.22-1.30V：20mV/step	RW	32H

REG 22H: Reserved

Default：XXH

Reset: System reset

Table 10-21

Bit	Description	R/W	Default
7-0	Reserved	RW	00

REG 23H: BUCK1 voltage control

Default：B2H

Reset: System reset

Table 10-22

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 1.0V 0.50-1.20V：10mV/step 1.22-1.30V：20mV/step	RW	32H

REG 24H: BUCK4 voltage control

Default：XXH

Reset: System reset

Table 10-23

Bit	Description	R/W	Default			
7	DVM finished or not status bit 0: not finished 1: finished	R	1			
6-0	voltage setting Bit 6-0 0.80-1.12V：10mV/step 1.14-1.84V：20mV/step	RW	BUCK4SET is tied to :	GND	VINT	Floating
			Type 0	1.5V	1.36V	1.24V
			Type 1	0.9V	1.8V	1.0V

Note：type 0 or 1 set by OTP

REG 25H: BUCK3 voltage control

Default：A8H

Reset: System reset

Table 10-24

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1

6-0	voltage setting Bit 6-0, default is 1.0V 0.60-1.10V：10mV/step 1.12-1.52V：20mV/step	RW	28H

REG 26H: BUCK2 voltage control

Default：A8H

Reset: System reset

Table 10-25

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 1.0V 0.60-1.10V：10mV/step 1.12-1.52V：20mV/step	RW	28H

REG 27H: BUCK1 /2 /3 /4 /5 DVM control

Default：XCH

Reset: System reset

Table 10-26

Bit	Description	R/W	Default
7	BUCK2 DVM on-off control 0: disable; 1: enable	RW	1
6	BUCK3 DVM on-off control 0: disable; 1: enable	RW	1
5	BUCK4 DVM on-off control 0: disable; 1: enable	RW	1
4	BUCK1 DVM on-off control 0: disable; 1: enable	RW	1
3	Reserved		
2	BUCK5 DVM on-off control 0: disable; 1: enable	RW	1
1	RSMRST_B drive low when ALDO3 less than 85% or not control 0: not drive low; 1: drive low	RW	0

0	DRAMPWROK drive low when FLDO3 less than 85% or not control 0: not drive low; 1: drive low	RW	0

REG 28H: ALDO1 voltage control

Default：17H

Reset: System reset

Table 10-27

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0 0.7-3.3V, 100mV/step, default is 3.0V	RW	10111

REG 29H: ALDO2 voltage control

Default：17H

Reset: System reset

Table 10-28

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 3.0V 0.7-3.3V, 100mV/step	RW	10111

REG 2AH: ALDO3 voltage control

Default：1AH

Reset: System reset

Table 10-29

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 3.3V 0.7-3.3V, 100mV/step	RW	1AH

REG 2CH: BC Module Global Register

Default：00H

Reset: bit7 is system reset, bit[6:0] Power On reset

Table 10-30

Bit	Description	R/W	Default
7	**DCD_SEL** **DCD Detect Select** Software writes 1 to this bit to select DCD Detection during BC Detect.	RW	0
6-5	**DCD_TIMEOUT_CTL** **DCD Timeout Control** Software writes these fields to configure the DCD timeout value. When the DCD_SEL is set, the BC Module read the MultValIdBc if pin contact has been detected or the time defined on these fields has been expired . When the DCD_SEL is not set, he BC Module read the MultValIdBc if the time defined on these fields has been expired . 00: 300ms 01: 100ms 10: 500ms 11: 900ms	RW	0
4	**Vlgc_Com_Sel** **Vlgc Compare Select** Software writes 1 to this bit to choose the Vlgc compare during Primary Detect when the ID pin is float. When this bit is set, the BC Module is optionally allowed to compare D- with Vlgc beside the Vdp_src comparing. The BC Module determine that it is attached to a DCP or CDP if D- is greater than Vdat_ref, but less than Vlgc. Otherwise, the BC Module determine that it is attached to a SDP, which may actually be a SDP, or a PS2 port, or a proprietary charge.	RW	0
3	**DBP_Timeout_CTL** **DBP Hardware Timeout Control** If this bit is set, the BC Module would clear the DB_Perform bit on the BC_USB_Sta_R register after Tsvld_con_wkb when the DB_Perform bit is set. Note: Tsvld_con_wkb = 45min	RW	0
2	**BC_status** **BC Detection status** Detection finish or not 1:Detecting,when starting BC Detect, set this bit 0:Detect finish	RW	0
1	**Reserved**	RW	0
0	**RS**	RW	0

	Run/Stop Software writes 1 to this bit to start the BC Module operation. A transition from a zero to a one would cause the reset on the BC Module logic. If this bit = 1,when VBUS low go high, BC detection start automatically		

REG 2DH: BC Module VBUS Control and Status Register

Default：30H

Reset: Power On reset

Table 10-31

Bit	Description	R/W	Default
7	**Reserved**	R	0
6	Indicate the first power on status Software write 1 to this bit to indicate not first time power on If Battery not present, and this bit is 0,the VBUS current limit set to 3A,for the F/W update in factory	RW	0
5	DP/DM floating Detection enable 0:disable 1:enable	RW	1
4	DP/DM pull down enable 0:disable 1:enable	RW	1
3	RID detect enable 0:disable 1:enable 1,VBUS presence and REG_2C[0]=1,RID was enabled automatically,do not depend on this bit; 2,VBUS presence or in power on state,set this bit to 1 will enable RID detect	RW	0
2-0	Reserved	RW	0

REG 2EH: BC USB Status Register

Default：40H

Reset: Reset by the VBUS negative edge

Table 10-32

Bit	Description	R/W	Default
7	DB_Perform Dead Battery Perform Both BC Module and software write 1 to this bit to perform unconfig DBP clause and clean it to 0 to	RW	0

	stop the unconfig DBP clause.		
6	Dead battery detect enable bit (Reset: power on reset) 0:disable 1:enable	RW	1
5	Reserved		
4	USB_Mode USB Speed Mode Flag This bit is used in good battery state. It is set by the USB driver to indicate the USB speed mode for the power manage. 0: High-Speed, Full-Speed or Low-Speed Mode 1: Super-Speed Mode	RW	0
3-0	Dev_Bus_State Device Bus State Flag These fields are used in good battery state. They are set by the USB driver to indicate the USB bus state for the power manage. 000b: attached, physical signal pin contact 001b: connected, attached and when the downstream terminal is valid 010b: suspended 011b: configured 100b-111b: reserved	RW	0

REG 2FH: BC Detect Status Register

Default：20H

Reset: Reset by the VBUS negedge

Table 10-33

<table>
<tr><th>Bit</th><th>Description</th><th>R/W</th><th>Default</th></tr>
<tr><td>7-5</td><td>BC_Result
BC Detect Result
These fields indicate the result of BC Detect performance. These fields should be used by the BC Module when the BC_Per bit of the BC_GLOBAL_R register transaction from 1 to 0.
<table>
<tr><td>Value</td><td>Meaning</td><td>Descriptor</td></tr>
<tr><td>000b</td><td>Reserved</td><td>/</td></tr>
<tr><td>001b</td><td>SDP</td><td>The insert port is Standard Downstream Port</td></tr>
<tr><td>010b</td><td>CDP</td><td>The insert port is Charging Downstream Port</td></tr>
<tr><td>011b</td><td>DCP</td><td>The insert port is Dedicated Charging Port</td></tr>
<tr><td>100b</td><td>Reserved</td><td>/</td></tr>
</table></td><td>R</td><td>001</td></tr>
</table>

	101b	Reserved	/			
	110b	Reserved	/			
	111b	Reserved	/			
4-0	**Reserved**				R	00000

REG 30H: VBUS path control & Hold voltage setting

Default：21H

Reset: Bit [7] & bit [2] reset signal is System reset, and Bit [6:3] & bit [1:0] reset signal is Power on reset

Table 10-34

Bit	Description		R/W	Default
7	VBUS path select control (VBUS_SEL) when VBUS valid 0: VBUS path select ed 1: VBUS path Not selected		RW	0
6	Reserved			
5	V_{HOLD} setting bit 2	000: 4.0V; 001: 4.1V; 010: 4.2V 011: 4.3V; 100: 4.4V; 101: 4.5V 110: 4.6V; 111: 4.7V	RW	1
4	V_{HOLD} setting bit 1		RW	0
3	V_{HOLD} setting bit 0		RW	0
2	Reserved		RW	0
1-0	Current limit default when BC1.2 detection result is non SDP ： 00：900mA 01：1500mA 10：2000mA 11：2500mA		RW	01

REG 31H: Power wakeup control & V_{OFF} setting

Default：03H

Reset: Bit 3 reset signal is system reset, Bit [7-4] and Bit [2-0] reset signal is Power on reset

Table 10-35

Bit	Description	R/W	Default
7	PWROK drive low or not when Power wake up and REG 31_[3]=1 0: not drive low 1: drive low in wake up period	RW	0
6	Reserved	RW	0
5	Soft Power wakeup, Write 1 to this bit, the output power will be waked up, then this bit will clear itself	RW	0
4	Control bit for IRQ output and wakeup trigger when REG 31_[3] is 1	RW	0

	0: IRQ pin is masked and IRQ can wakeup AW1660 when REG 31_[3] is 1 1: IRQ pin is normal and IRQ can't wakeup AW1660 when REG 31_[3] is 1			
3	Enable bit for the function that output power be waked up by IRQ source, or IRQ pin, or REG 31_[5], etc. write 1 to this bit will clear itself 0: function is disable 1: function is enable		RW	0
2	V_{OFF} setting bit 2	000-2.6V; 001-2.7V; 010-2.8V; 011-2.9V; 100-3.0V; 101-3.1V; 110-3.2V; 111-3.3V	RW	0
1	V_{OFF} setting bit 1		RW	1
0	V_{OFF} setting bit 0		RW	1

REG 32H: Power Disable, BAT detect and CHGLED pin control

Default：4XH

Reset: Bit 7 reset signal is system reset, and Bit [6:0] reset signal is Power on reset

Table 10-36

Bit	Description		R/W	Default
7	Reserved			
6	Battery detection function control: 0-disable; 1-enable		RW	1
5-4	CHGLED pin control	00: Hi-Z 01: 25% 0.5Hz toggle 10: 25% 2Hz toggle 11: drive low	RW	00
3	CHGLED pin control	0: controlled by REG 32H[5:4] 1: controlled by Charger	RW	0
2	Reserved		RW	0
1-0	control bit for Delay time between PWROK signal and power good time 00: 8ms; 01: 16ms; 10: 32ms; 11: 64ms		RW	11

REG 33H: Charger Control 1

Default：CXH

Reset: Bit [7] reset is system reset, Bit [6:0] reset is power on reset

Table 10-37

Bit	Description	R/W	Default
7	Charger enable control 0-disable, 1-enable	RW	1
6-5	Charger target voltage setting 00: 4.10V; 01: 4.15V; 10: 4.2V; 11: 4.35V	RW	10

4	Charger end condition setting: 0-when I_{CHARGE}<10% I_{CHG}， Charge is done; 1-when I_{CHARGE}<20% I_{CHG}， Charge is done;	RW	0
3-0	Charge Current setting 200mA-2.8A, 200mA/step, default is 1200mA, 14steps, 1110-1111 reserved.	RW	X

REG 34H: Charger Control 2

Default：45H

Reset: Power on reset

Table 10-38

Bit	Description		R/W	Default
7	Pre-charge Timer length setting 1	00: 40 minutes; 01: 50 minutes; 10: 60 minutes; 11: 70 minutes.	RW	0
6	Pre-charge Timer length setting 0		RW	1
5	Charger output turn off or not when charging is end & the PMIC is on state 0: turn off; 1: do not turn off		RW	0
4	CHGLED Type select when REG 32_[3] is 1 0: Type A; 1: Type B		RW	0
3	reserved		RW	0
2	reserved		RW	1
1	Fast charge maximum time setting 1	00: 6 hours; 01: 8 hours; 10: 10 hours; 11: 12 hours.	RW	0
0	Fast charge maximum time setting 0		RW	1

REG 35H: Charger Control 3

Default：18H

Reset: [7:4] is VBUS negedge reset , others Power on reset

Table 10-39

Bit	Description	R/W	Default
7-4	VBUS current limit select when VBUS Current limited mode is enable 0000-100mA 0001-500mA 0010-900mA 0011-1500mA 0100-2000mA 0101-2500mA 0110-3000mA 0111-3500mA 1xxx-4000mA	RW	0001
3	Charger temperature loop enable 0: disable 1:enable	RW	1
2-0	Reserved		

REG 36H: POK setting

Default：59H

Reset: Bit 3 is reset by system reset, the others is reset by Power on reset

Table 10-40

Bit	Description		R/W	Default
7	ONLEVEL setting 1	00: 128ms; 01: 1s;	RW	0
6	ONLEVEL setting 0	10: 2s; 11: 3s.	RW	1
5	IRQLEVEL setting 1	00: 1s; 01: 1.5s;	RW	0
4	IRQLEVEL setting 0	10: 2s; 11: 2.5s.	RW	1
3	Enable bit of the function which will shut down the PMIC when POK is larger than OFFLEVEL 0-disable; 1-enable		RW	1
2	The PMIC auto turn on or not when it shut down after off level POK 0: not turn on; 1: auto turn on		RW	0
1	OFFLEVEL setting 1	00: 4s; 01: 6s;	RW	0
0	OFFLEVEL setting 0	10: 8s; 11: 10s.	RW	1

REG 37H: POK Power off activity time setting

Default：00H

Reset: Power on reset

Table 10-41

Bit	Description	R/W	Default
7-3	Reserved		
2-0	Power off activity time setting 0/10/20/30/40/50/60/70 S	R/W	000

REG 38H: $V_{LTF\text{-}charge}$ setting

Default：A5H

Reset: Power on reset

Bit	Description		R/W	Default
7-0	$V_{LTF\text{-}charge}$ setting, M	M*10H，M=A5H:2.112V;range is 0V-3.264V	RW	A5H

REG 39H: $V_{HTF\text{-}charge}$ setting

Default：1FH

Reset: Power on reset

Table 10-42

Bit	Description		R/W	Default
7-0	$V_{LHF\text{-}charge}$ setting, N	N*10H， N=1FH:0.397V;range is 0V-3.264V	RW	1FH

REG 3AH: Reserved

Default：XXH

Reset: Power on reset, bit7 is system reset

Table 10-43

Bit	Description	R/W	Default
7-0	Reserved		

REG 3BH: Buck frequency setting

Default：08H

Reset: Power on reset

Table 10-44

Bit	Description		R/W	Default
7	Buck and PWM charger frequency spread enable 0: disable; 1: enable		RW	0
6	Buck and PWM charger frequency spread range control 0: 50KHz; 1: 100KHz		RW	0
5	Reserved			
4	BUCK1/5 mode select 0:Always PWM 1:PSM/PWM Auto switch		RW	0
3-0	Buck frequency setting bit 3-0	f_{OSC}: 3MHz *(1+ (8-N) *0.04) N=08: 3MHz Every step f_{OSC} error is ±5%	RW	1000

REG 3CH: $V_{LTF\text{-}work}$ setting

Default：FCH

Reset: Power on reset

Table 10-45

Bit	Description		R/W	Default
7-0	$V_{LTF-work}$ setting, M	M*10H， M=FCH:3.226V;range is 0V-3.264V	RW	FCH

REG 3DH: $V_{HTF-work}$ setting

Default：16H

Reset: Power on reset

Table 10-46

Bit	Description		R/W	Default
7-0	$V_{HTF-work}$ setting, N	N*10H， N=16H:0.282V;range is 0V-3.264V	RW	16H

REG 40H: IRQ enable 1

Default：D8H

Reset: Power on reset

Table 10-48

Bit	Description	R/W	Default
7	Same as bit4	RW	1
6	Same as bit3	RW	1
5	Same as bit2	RW	0
4	VBUS over voltage IRQ enable	RW	1
3	VBUS from low go high IRQ enable	RW	1
2	VBUS from high go low IRQ enable	RW	0
1-0	Reserved		

REG 41H: IRQ enable 2

Default：FFH

Reset: Power on reset

Table 10-49

Bit	Description	R/W	Default
7	Battery append IRQ enable	RW	1
6	Battery absent IRQ enable	RW	1
5	Battery maybe bad IRQ enable	RW	1

4	Quit battery safe mode IRQ enable	RW	1
3	Charger is charging IRQ enable	RW	1
2	Battery charge done IRQ enable	RW	1
1-0	Reserved		

REG 42H: IRQ enable 3

Default：FFH

Reset: Power on reset

Table 10-50

Bit	Description	R/W	Default
7	Battery over temperature in charge mode IRQ (CBTOIRQ) enable	RW	1
6	Quit Battery over temperature in charge mode IRQ (QCBTOIRQ) enable	RW	1
5	Battery under temperature in charge mode IRQ (CBTUIRQ) enable	RW	1
4	Quit Battery under temperature in charge mode IRQ (QCBTUIRQ) enable	RW	1
3	Battery over temperature in work mode IRQ (WBTOIRQ) enable	RW	1
2	Quit Battery over temperature in work mode IRQ (QWBTOIRQ) enable	RW	1
1	Battery under temperature in work mode IRQ (WBTUIRQ) enable	RW	1
0	Quit Battery under temperature in work mode IRQ (QWBTUIRQ) enable	RW	1

REG 43H: IRQ enable 4

Default：03H

Reset: Power on reset

Table 10-51

Bit	Description	R/W	Default
7	The PMIC temperature over the warning level 2 IRQ (OTIRQ) enable	RW	0
6-3	Reserved		
2	GPADC(GPIO0) ADC convert finished IRQ enable	RW	0
1	Enable bit for IRQ which indicate battery capacity ratio being lower than warning level 1, (WL1IRQ); normally, for low power warning requisition	RW	1
0	Enable bit for IRQ which indicate battery capacity ratio being lower than warning level 2, (WL2IRQ); normally, for power off requisition	RW	1

REG 44H: IRQ enable 5

Default：7CH

Reset: System reset

Table 10-52

Bit	Description	R/W	Default
7	Event timer timeout IRQ enable	RW	0
6	POK positive edge IRQ (POKPIRQ) enable	RW	1
5	POK negative edge IRQ (POKNIRQ) enable	RW	1
4	POK short time active IRQ (POKSIRQ) enable	RW	1
3	POK long time active IRQ (POKLIRQ) enable	RW	1
2	POK off time active IRQ (POKOIRQ) enable	RW	1
1	GPIO1 input edge IRQ enable	RW	0
0	GPIO0 input edge IRQ enable	RW	0

REG 45H: IRQ enable 6

Default：00H

Reset: System reset

Table 10-53

Bit	Description	R/W	Default
7-2	Reserved		
1	BC_USB_ChngInEn BC USB Status Change Interrupt Enable BC_USB_ChngEvnt Interrupt Enable. BC Detection result changed or not	RW	0
0	MV_ChngIntEn Rid MV_ChngEvnt Interrupt Enable.	RW	0

REG 48H: IRQ Status 1

Default：00H

Reset: Power on reset

Table 10-54

Bit	Description	R/W	Default
7	Same as bit4, write 1 to it or VBUS drop to normal will clear it	RW	0
6	Same as bit3, write 1 to it or VBUS from high go low will clear it	RW	0
5	Same as bit2, write 1 to it or VBUS from low go high will clear it	RW	0
4	VBUS over voltage IRQ, write 1 to it or VBUS drop to normal will clear it	RW	0

3	VBUS from low go high IRQ, write 1 to it or VBUS from high go low will clear it	RW	0
2	VBUS from high go low IRQ, write 1 to it or VBUS from low go high will clear it	RW	0
1-0	Reserved	RW	0

REG 49H: IRQ Status 2

Default：00H

Reset: power on reset

Table 10-55

Bit	Description	R/W	Default
7	Battery append IRQ, write 1 to it or Battery remove will clear it	RW	0
6	Battery absent IRQ, write 1 to it or Battery append will clear it	RW	0
5	Battery maybe bad IRQ, write 1 to it or PMIC quit battery safe mode will clear it	RW	0
4	Quit battery safe mode IRQ, write 1 to it or The PMIC enter battery- safe mode will clear it	RW	0
3	Charger is charging IRQ, write 1 to it or charging is stop will clear it	RW	0
2	Battery charge done IRQ, write 1 to it or charger restart charging will clear it	RW	0
1-0	Reserved		

REG 4AH: IRQ Status 3

Default：00H

Reset: power on reset

Table 10-56

Bit	Description	R/W	Default
7	CBTOIRQ, write 1 to it or Battery temperature drop to normal will clear it	RW	0
6	QCBTOIRQ, write 1 to it or Battery over temperature will clear it	RW	0
5	CBTUIRQ, write 1 to it or Battery temperature rise to normal will clear it	RW	0
4	QCBTUIRQ, write 1 to it or Battery under temperature will clear it	RW	0
3	WBTOIRQ, write 1 to it or Battery drop to temperature will clear it	RW	0
2	QWBTOIRQ, write 1 to it or Battery over temperature will clear it	RW	0
1	WBTUIRQ, write 1 to it or Battery rise to temperature will clear it	RW	0
0	QWBTUIRQ, write 1 to it or Battery under temperature will clear it	RW	0

REG 4BH: IRQ Status 4

Default：00H

Reset: Bit [7] reset is power on reset, Bit [6:0] reset is system reset

Table 10-57

Bit	Description	R/W	Default
7	OTIRQ, write 1 to it or IC temperature drop to normal will clear it	RW	0
6-3	Reserved	RW	0
2	GPADC(GPIO0) ADC convert finished IRQ, write 1 will clear it	RW	0
1	IRQ which indicate battery capacity ratio being lower than warning level 1, (WL1IRQ); write 1 to it or system power rise up to warning level 1 will clear it	RW	0
0	IRQ which indicate battery capacity ratio being lower than warning level 2, (WL2IRQ); write 1 to it or system power rise up to warning level 2 will clear it	RW	0

REG 4CH: IRQ Status 5

Default：00H

Reset: System reset

Table 10-58

Bit	Description	R/W	Default
7	Event timer timeout IRQ, write 1 will clear it	RW	0
6	POKPIRQ, write 1 to it will clear it	RW	0
5	POKNIRQ, write 1 to it will clear it	RW	0
4	POKSIRQ, write 1 to it will clear it	RW	0
3	POKLIRQ, write 1 to it will clear it	RW	0
2	POKOIRQ, write 1 to it will clear it	RW	0
1	GPIO1 input edge IRQ, write 1 will clear it	RW	0
0	GPIO0 input edge IRQ, write 1 will clear it	RW	0

REG 4DH: IRQ Status 6

Default：00H

Reset: Reset by VBUS negedge

Table 10-59

Bit	Description	R/W	Default
7-2	Reserved		
1	BC_USB_ChngEvnt BC USB Status Change Event This bit indicates that there is a change in the BC_USB_Sta_R register. When this bit is 1, and the interrupt on the BC_Charge_ChngInEn is 1, the BC Module will issue an interrupt to the controller. This bit and associated interrupt is clean by writing '1'.	R	0

	MV_ChngEvnt MultValIdBc Multi-Valued input changed Event This bit indicates that there is a change in the value of MultValIdBc field. When this bit is 1, and the interrupt on the MV_ChngIntEn is 1, the BC Module will issue an interrupt to the controller.		
0	This bit and associated interrupt is clean by writing '1'.	R	0

REG 58H: TS pin input ADC data, highest 8bit

Default：00H

Reset: System reset

Table 10-60

Bit	Description	R/W	Default
7-0	TS pin input ADC data highest 8bits，Default is Battery temperature	R	00

REG 59H: TS pin input ADC data, lowest 4bit

Default：00H

Reset: System reset

Table 10-61

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	TS pin input ADC data lowest 4bits，Default is Battery temperature	R	00

REG 5AH: GPADC pin input ADC data, highest 8bit

Default：00H

Reset: System reset

Table 10-62

Bit	Description	R/W	Default
7-0	GPADC pin input ADC data, highest 8bit	R	00

REG 5BH: GPADC pin input ADC data, lowest 4bit

Default：00H

Reset: System reset

Table 10-63

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	GPADC pin input ADC data, lowest 4bit	R	00

REG 78H: Average data bit[11:4] for Battery voltage (BATSENSE)

Default：00H

Reset: System reset

Table 10-64

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery voltage (BATSENSE)	R	00

REG 79H: Average data bit[3:0] for Battery voltage (BATSENSE)

Default：00H

Reset: System reset

Table 10-65

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	Average data bit[3:0] for Battery voltage (BATSENSE)	R	00

REG 7AH: Average data bit[11:4] for Battery charge current

Default：00H

Reset: System reset

Table 10-66

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery charge current	R	00

REG 7BH: Average data bit[3:0] for Battery charge current

Default：00H

Reset: System reset

Table 10-67

Bit	Description	R/W	Default
7-4	Reserved	R	00

3-0	Average data bit[3:0] for Battery charge current	R	00

REG 7CH: Average data bit[11:4] for Battery discharge current

Default：00H

Reset: System reset

Table 10-68

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery discharge current	R	00

REG 7DH: Average data bit[3:0] for Battery discharge current

Default：00H

Reset: System reset

Table 10-69

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	Average data bit[3:0] for Battery discharge current	R	00

REG 80H: Buck PWM/PFM mode select

Default：80H

Reset: system reset

Table 10-70

Bit	Description		R/W	Default
7	BUCK output over voltage turn off PMIC function enable: 0-disable; 1-enable Suggest set this bit to 0 when performing Vrun going down to Vsleep		R/W	1
	BUCK1/BUCK5	0.5~1.13V, 33.3%; 1.14~1.3V, 25%		
	BUCK2/BUCK3	0.6~1.36V, 33.3%; 1.37~1.52V, 25%		
	BUCK4	0.8~1.11V, 33.3%; 1.12~1.43V, 29%; 1.44~1.84V, 21.2%		
	BUCK6	1.6~2.3V, 21%; 2.4~3.1V, 17.6%; 3.2~3.4V, 11%		
6	BUCK2 PFM/PWM control: 0: auto switch 1: always PWM		RW	0
5	BUCK3 PFM/PWM control: 0: auto switch 1: always PWM		RW	0
4	BUCK4 PFM/PWM control: 0: auto switch 1: always PWM		RW	0
3	BUCK1 PFM/PWM control: 0: auto switch 1: PSM/PWM When this bit is set as '1', refer to REG3B bit [4] for BUCK mode select		RW	0

2	Reserved	RW	0
1	BUCK5 PFM/PWM control: 0: auto switch 1: PSM/PWM When this bit is set as '1', refer to REG3B bit [4] for BUCK mode select	RW	0
0	BUCK6 PFM/PWM control: 0: auto switch 1: always PWM	RW	0

REG 81H: Off-Discharge and Output monitor control

Default：80H

Reset: Power on reset

Table 10-71

Bit	Description	R/W	Default
7	Internal off-Discharge enable for Buck & LDO 0-disable; 1-enable	RW	1
6	BUCK2 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable;	RW	0
5	BUCK3 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable;	RW	0
4	BUCK4 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable;	RW	0
3	BUCK1 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable;	RW	0
2	Reserved		
1	BUCK5 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable;	RW	0
0	BUCK6 85% Low voltage turn off PMIC function enable: 0-disable; 1-enable;	RW	0

REG 82H: ADC Enable

Default：E1H

Reset: Power on reset

Table 10-72

Bit	Description		R/W	Default
7	BAT voltage ADC enable	0: off, 1: on	RW	1
6	BAT current ADC enable	0: off, 1: on	RW	1
5	Die temperature ADC enable	0: off, 1: on	RW	1
4	GPIO0 ADC enable	0: off, 1: on	RW	0
3-1	Reserved			

0	TS pin input to ADC enable	0: off, 1: on	RW	1

REG 84H: ADC speed setting, TS pin Control

Default：F2H

Reset: power on reset

Table 10-73

Bit	Description		R/W	Default
7-6	Current source from GPIO0 pin control: 00: 20uA; 01: 40uA; 10: 60uA; 11: 80uA		RW	11
5-4	Current source from TS pin control: 00: 20uA; 01: 40uA; 10: 60uA; 11: 80uA		RW	11
3	reserved		RW	0
2	TS pin function select: 0-TS pin is the battery temperature sensor input and will affect the charger 1-TS pin is an External input for ADC and do not affect the charger		RW	0
1-0	Current source from TS pin on/off enable bit [1:0]	00: off 01: on when charging battery, off when not charging 10: on in ADC phase and off when out of the ADC phase, for power saving 11: always on	RW	10

REG 85H: ADC speed setting

Default：B0H

Reset: power on reset

Table 10-74

Bit	Description		R/W	Default
7	TS/GPIO0 ADC speed setting bit 1	100×2^n	RW	1
6	TS/GPIO0 ADC speed setting bit 0	So Fs=25, 50, 100, 200Hz	RW	0
5	Vol/Cur ADC speed setting bit 1	100×2^n	RW	1
4	Vol/Cur ADC speed setting bit 0	So Fs=100, 200, 400, 800Hz	RW	1
3	Reserved			
2	GPIO0 ADC work mode 1:output current 0:not output current		RW	0
1-0	Reserved		RW	00

REG 8AH: Timer control

Default：00H

Reset: System reset

Table 10-75

Bit	Description	R/W	Default
7	Timer time out status It indicate that timer time out when this bit from low go high Write this bit to 1, will clear the status and the timer	RW	0
6-0	Set threshold of the timer Write these 7 bits to all 0, will disable the timer	RW	0000000

REG 8EH: Buck output voltage monitor de-bounce time setting

Default：40H

Reset: Power on reset

Table 10-76

Bit	Description	R/W	Default
8E[7:6]	Buck output voltage monitor de-bounce time setting, 00-62us; 01-124us; 10-186us; 11-248us	RW	01
8E_[5:0]	Reserved	RW	00

REG 8FH: IRQ pin, hot-over shut down

Default：00H

Reset: Power on reset

Table 10-77

Bit	Description	R/W	Default
7	Reserved	RW	0
6-4	Reserved		
3	The function control that 16s' POK trigger power on reset: 0-disable; 1-enable	RW	0
2	The PMIC shut down or not when Die temperature is over the warning level 3 0-not shut down; 1-shut down	RW	0
1	Voltage recovery enable bit when AXP288 wakeup from REG31H[3]=1 0: recovery to the vboot 1: not recovery to the vboot	RW	0
0	Reserved	RW	0

REG 90H: GPIO0 (GPADC) control

Default：07H

Reset: system reset

Table 10-78

Bit	Description		R/W	Default
7	Enable GPIO0 Positive edge trigger IRQ or wake up when GPIO0 is digital input 0: disable; 1: enable		RW	0
6	Enable GPIO0 Negative edge trigger IRQ or wake up when GPIO0 is digital input 0: disable; 1: enable		RW	0
5-3	Reserved		RW	0
2	GPIO0 pin function control bit 2	000: drive low 001: drive high 010: digital input, trigger point is about 1.2V 011: low noise LDO on 100: low noise LDO off 101-111: Floating, if ADC enable，then work as ADC input mode	RW	1
1	GPIO0 pin function control bit 1		RW	1
0	GPIO0 pin function control bit 0		RW	1

REG 91H: GPIO0LDO and GPIO0 high level voltage setting

Default：1AH

Reset: system reset

Table 10-79

Bit	Description	R/W	Default
7-5	Reserved		
4-0	GPIO0LDO and GPIO0 High level voltage setting bit 4-0 From 0.7 to 3.3V, 100mV/step, 11011-11111 reserved	RW	11010

REG 92H: GPIO1 control

Default：07H

Reset: system reset

Table 10-80

Bit	Description	R/W	Default
7	Enable GPIO1 Positive edge trigger IRQ or wake up when GPIO1 is digital input 0: disable; 1: enable	RW	0

6	Enable GPIO1 Negative edge trigger IRQ or wake up when GPIO1 is digital input 0: disable; 1: enable		RW	0
5-3	Reserved			
2	GPIO1 pin function control bit 2	000: drive low 001: drive high 010: digital input, trigger point is about 1.2V 011: low noise LDO on 100: low noise LDO off 101-111: Floating	RW	1
1	GPIO1 pin function control bit 1		RW	1
0	GPIO1 pin function control bit 0		RW	1

REG 93H: GPIO1LDO and GPIO1 high level voltage setting

Default：1AH

Reset: system reset

Table 10-81

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	GPIO1LDO and GPIO1 High level voltage setting bit 4-0 From 0.7 to 3.3V, 100mV/step, 11011-11111 reserved	RW	11010

REG 94H: GPIO signal bit

Default：00H

Reset: system reset

Table 10-82

Bit	Description	R/W	Default
7-2	Reserved		
1	This bit reflect the logic level of the GPIO1 pin when configured as digital input	R	0
0	This bit reflect the logic level of the GPIO0 pin when configured as digital input	R	0

REG 97H: GPIO pull down control

Default：00H

Reset: system reset

Table 10-83

Bit	Description	R/W	Default
7-2	Reserved		

1	GPIO1 Pull down control in digital input mode 0: off 1: on	RW	0
0	GPIO0 Pull down control in digital input mode 0: off 1: on	RW	0

REG 9AH: Run time Sleep power up sequence 1

Default：00H

Reset: System reset

Table 10-84

Bit	Description	R/W	Default
7-5	When BUCK2 controlled by SLP_S0IX_B, the power up sequence setting bit2-0 000-100:5 steps	RW	000
4-2	When BUCK3 controlled by SLP_S0IX_B, the power up sequence setting bit2-0 000-100:5 steps	RW	000
1-0	When BUCK1 controlled by SLP_S0IX_B, the power up sequence setting bit2-1 000-100:5 steps	RW	00

REG 9BH: Run time Sleep power up sequence 2

Default：00H

Reset: System reset

Table 10-85

Bit	Description	R/W	Default
7	When BUCK1 controlled by SLP_S0IX_B, the power up sequence setting bit0	RW	0
6-4	When BUCK5 controlled by SLP_S0IX_B, the power up sequence setting bit2-0 000-100:5 steps	RW	000
3-1	When FLDO1 controlled by SLP_S0IX_B, the power up sequence setting bit2-0 000-100:5 steps	RW	000
0	When BUCK2 controlled by SLP_S0IX_B, the power down sequence setting bit2	RW	0

REG 9CH: Run time Sleep power down sequence 1

Default：00H

Reset: System reset

Table 10-86

7-6	When BUCK2 controlled by SLP_S0IX_B, the power down sequence setting bit1-0 000-100:5 steps	RW	00
5-3	When BUCK3 controlled by SLP_S0IX_B, the power down sequence setting bit2-0 000-100:5 steps	RW	000
2-0	When BUCK1 controlled by SLP_S0IX_B, the power down sequence setting bit2-0 000-100:5 steps	RW	000

REG 9DH: Run time Sleep power down sequence 2

Default：00H

Reset: System reset

Table 10-87

7-5	When BUCK5 controlled by SLP_S0IX_B, the power down sequence setting bit2-0 000-100:5 steps	RW	000
4-2	When FLDO1 controlled by SLP_S0IX_B, the power down sequence setting bit2-0 000-100:5 steps	RW	000
1-0	Reserved		

REG 9EH: Power rail mode in Sleep state

Default：00H

Reset: System reset

Table 10-88

Bit	Description	R/W	Default
7-5	Reserved		
4	When BUCK2 controlled by SLP_S0IX_B, power state in sleep mode: 0:off 1:Vsleep	RW	0
3	When BUCK3 controlled by SLP_S0IX_B, power state in sleep mode: 0:off 1:Vsleep	RW	0
2	When BUCK1 controlled by SLP_S0IX_B, power state in sleep mode: 0:off 1:Vsleep	RW	0
1	When BUCK5 controlled by SLP_S0IX_B, power state in sleep mode: 0:off 1:Vsleep	RW	0
0	When FLDO1 controlled by SLP_S0IX_B, power state in sleep mode: 0:off 1:Vsleep	RW	0

REG A0H: Real time data bit[11:4] for Battery voltage (BATSENSE)

Default：00H

Reset: System reset

Table 10-89

Bit	Description	R/W	Default
7-0	Real time data bit[11:4] for Battery voltage (BATSENSE)	R	00

REG A1H: Real time data bit[3:0] for Battery voltage (BATSENSE)

Default：00H

Reset: System reset

Table 10-90

Bit	Description	R/W	Default
7-4	Real time data bit[3:0] for Battery voltage (BATSENSE)	R	00
3-0	Reserved	R	00

REG B8H: Fuel Gauge Control

Default：E8H

Reset: power on reset

Table 10-91

Bit	Description	R/W	Default
7	fuel gauge enable control(including OCV and coulomb meter) 0-Disable 1-Enable	RW	1
6	Coulomb meter enable control 0-Disable 1-Enable	RW	1
5	Battery maximum capacity calibration enable control 0-Disable 1-Enable	RW	1
4	Battery maximum capacity calibration status 0: Not calibrating 1: Is calibrating	R	0
3	OCV-SOC curve calibration enable control 0-Disable	RW	1

	1-Enable Suggest set this bit as 0		
2	OCV-SOC curve calibration status 0-Not calibrating 1-Is calibrating	R	0
1-0	Reserved	RW	0

REG B9H: Battery capacity percentage for indication

Default：64H

Reset: Power on reset

Table 10-92

Bit	Description	R/W	Default
7	Indicating if battery capacity percentage for indication is valid: 0-Not valid 1-Is valid	R	0
6-0	Battery capacity percentage for indication	R	64H

REG BAH: RDC 1

Default：80H

Reset: Bit [7] & [4-0] reset is power on reset

Table 10-93

Bit	Description	R/W	Default
7	RDC calculation control; 0: disable; 1: enable	RW	1
6	RDC was right detected or not flag： 1-Y 0-N	R	0
5	RDC has detected or not during this power on time： 1-Y 0-N	R	0
4-0	RDC value HSB 5 bit	RW	00000

REG BBH: RDC 0

Default：5DH

Reset: power on reset

Table 10-94

Bit	Description	R/W	Default
7-0	RDC value LSB 8bit	RW	5DH

REG BCH: OCV 1

Default：00H

Reset: power on reset

Table 10-95

Bit	Description	R/W	Default
7-0	OCV HSB 8bit	R	00H

REG BDH: OCV0

Default：00H

Reset: power on reset

Table 10-96

Bit	Description	R/W	Default
7-4	Reserved		
3-0	OCV LSB 4bit	R	0000

REG E0H: Battery maximum capacity

Default：00H

Reset: Power on reset

Table 10-97

Bit	Description	R/W	Default
7	Indicating if battery maximum capacity is valid: 0-Not valid 1-Is valid	R/W	0
6-0	battery maximum capacity bit[14:8]	RW	00H

REG E1H: Battery maximum capacity

Default：00H

Reset: Power on reset

Table 10-98

Bit	Description	R/W	Default
7-0	battery maximum capacity bit[7:0](Unit: 1.456mAh)	RW	00H

REG E2H: Coulomb meter counter1

Default：00H

Reset: Power on reset

Table 10-99

Bit	Description	R/W	Default
7	Indicating if coulomb meter counter is valid: 0-Not valid 1-Is valid	RW	0
6-0	Coulomb meter counter[14:8]	RW	00H

REG E3H: Coulomb meter counter2

Default：00H

Reset: Power on reset

Table 10-100

Bit	Description	R/W	Default
7-0	Coulomb meter counter[7:0] (Unit: 1.456mAh)	RW	00H

REG E4H: OCV Percentage of battery capacity

Default：64H

Reset: Power on reset

Table 10-101

Bit	Description	R/W	Default
7	Indicating if OCV percentage of battery capacity is valid 0-Not valid 1-Is valid	R	0
6-0	OCV percentage of battery capacity	R	64H

REG E5H: Coulomb meter percentage of battery capacity

Default：64H

Reset: Power on reset

Table 10-102

Bit	Description	R/W	Default
7	Indicating if coulomb meter percentage of battery capacity is valid: 0-Not valid 1-Is valid	R	0
6-0	Coulomb meter percentage of battery capacity	R	64H

REG E6H: Battery capacity percentage warning level

Default：A0H

Reset: Power on reset

Table 10-103

Bit	Description	R/W	Default
7-4	Warning level 1: Warning threshold, 5-20%, 1% per step	RW	1010
3-0	Warning level 2: Shutting down threshold, 0-15%, 1% per step	RW	0000

REG E8H: Fuel gauge tuning control 0

Default：00H

Reset: Power on reset

Table 10-104

Bit	Description	R/W	Default
7-3	Reserved		
2-0	Battery capacity percentage for indication update minimum interval 000-30s 001-60s 010-120s 011-164s 100-immediately update when changed 101-5s 110-10s 111-20s	RW	0

REG E9H: Fuel gauge tuning control 1

Default：00H

Reset: Power on reset

Table 10-105

Bit	Description	R/W	Default
7-6	OCV Percentage calibrate the Coulomb meter percentage, maximum time interval 00-60s 01-120s 10-15s 11-30s	RW	0
5-3	Wait for the stability for charge when in RDC calculation 000-180s 001-240s 010-300s 011-600s 100-30s 101-60s 110-90s 111-120s	RW	0
2-0	Wait for the stability for discharge when in RDC calculation 000-180s 001-240s 010-300s 011-600s 100-30s 101-60s 110-90s 111-120s	RW	0

REG EAH: Fuel gauge tuning control 2

Default：00H

Reset: Power on reset

Table 10-106

Bit	Description	R/W	Default
7-6	OCV Percentage Debounce setting(only when the change continuous the same direction as more than N times, then the ocv percentage increase or decrease)N: 00-4 01-8 10-1 11-2	RW	0
5-4	Coulomb meter Percentage Debounce setting(only when the change continuous the	RW	0

	same direction as more than N times, then the ocv percentage increase or decrease)N: 00-4 01-8 10-1 11-2		
3	Battery maximum capacity calibration start condition: 0-OCV percentage ＜ (REG E6H[3:0] + 3) 1-OCV percentage ＜ (REG E6H[3:0] + 6)	RW	0
2	Battery maximum capacity calibration end condition 0 0-OCV percentage ≥ 95% 1-OCV percentage ＝ 100%	RW	0
1	Battery maximum capacity calibration end condition 1 0-wait for charge finished 1-do not wait for charge finished	RW	0
0	Battery maximum capacity calibration end condition 2 (wait Nms for the charge finished indication signal after REG 01H[6] clear to 0,N: 0-68 1-120	RW	0

REG EBH: Fuel gauge tuning control 3

Default：00H

Reset: Power on reset

Table 10-107

Bit	Description	R/W	Default
7	When charge status bit REG 01H[6] = 1,the percentage of indication can be decrease or not 0-decrease enable 1-decrease disable	RW	0
6-4	When REG 01H[6] = 1， percentage of indication decrease hysteresis(N) setting 000-4% 001-5% 010-6% 011-7% 100-0% 101-1% 110-2% 111-3%	RW	0

3	Calculation RDC current condition setting 0-≥300mA 1-≥150mA	RW	0
2-0	Calibrate RDC percentage changed threshold setting 000-4% 001-5% 010-6% 011-7% 100-0% 101-1% 110-2% 111-3% calibration：△OCVPCT > N	RW	0

REG ECH: Fuel gauge tuning control 4

Default：00H

Reset: Power on reset

Table 10-108

Bit	Description	R/W	Default
7	ADC current data include offset0 or not(For debug) 0-Enable 1-Disable	RW	0
6	ADC current data offset0 smooth control(For debug) 0-Enable 1-Disable	RW	0
5	RDC re-calculate when PMIC power on for power off 0-Disable 1-Enable	RW	0
4-3	The minimum battery voltage for RDC calculation 00-3.5V 01-3.6V 10-3.7V 11-3.4V	RW	00
2-0	Coulomb counter calibration threshold，relative with REG_E6_[3:0] 000-REG_E6H[3:0]+7(default) 001-REG_E6H[3:0]+8 010-REG_E6H[3:0]+9	RW	000

	011-REG_E6H[3:0]+10 100-REG_E6H[3:0]+3 101-REG_E6H[3:0]+4 110-REG_E6H[3:0]+5 111-REG_E6H[3:0]+6		

REG EDH: Fuel gauge tuning control 5

Default：00H

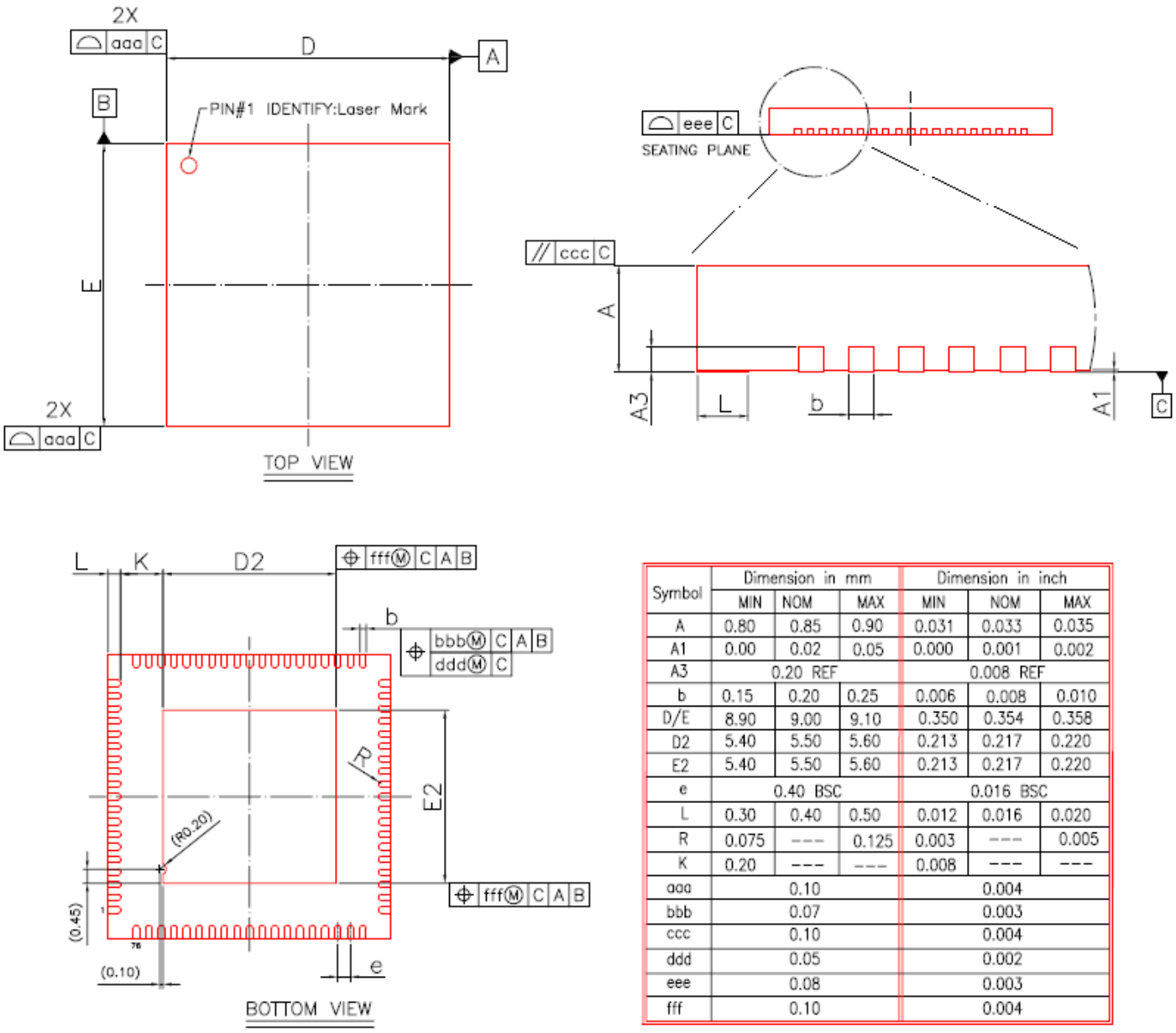
Reset: Power on reset

Table 10-109

Bit	Description	R/W	Default
7	OCV percentage relative with the charge/discharge rate control 0-Disable 1-Enable	RW	0
6	Update time when rate > 0.5C 0-30S 1-15S	RW	0
5-4	Update time when rate < 0.5C and rate > 0.1C 00-60S 01-75S 10-30S 11-45S	RW	00
3-2	Update time when rate < 0.1C 00-120S 01-180S 10-240S 11-60S	RW	00
1-0	Fixed update time 00-30S 01-45S 10-60S 11-15S	RW	00

11 Package

AXP288 is available in 9mm x 9mm 76-pin QFN package



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	8.90	9.00	9.10	0.350	0.354	0.358
D2	5.40	5.50	5.60	0.213	0.217	0.220
E2	5.40	5.50	5.60	0.213	0.217	0.220
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.075	---	0.125	0.003	---	0.005
K	0.20	---	---	0.008	---	---
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

Figure 11-1

Example for 9mm x 9mm 76-pin QFN board layout

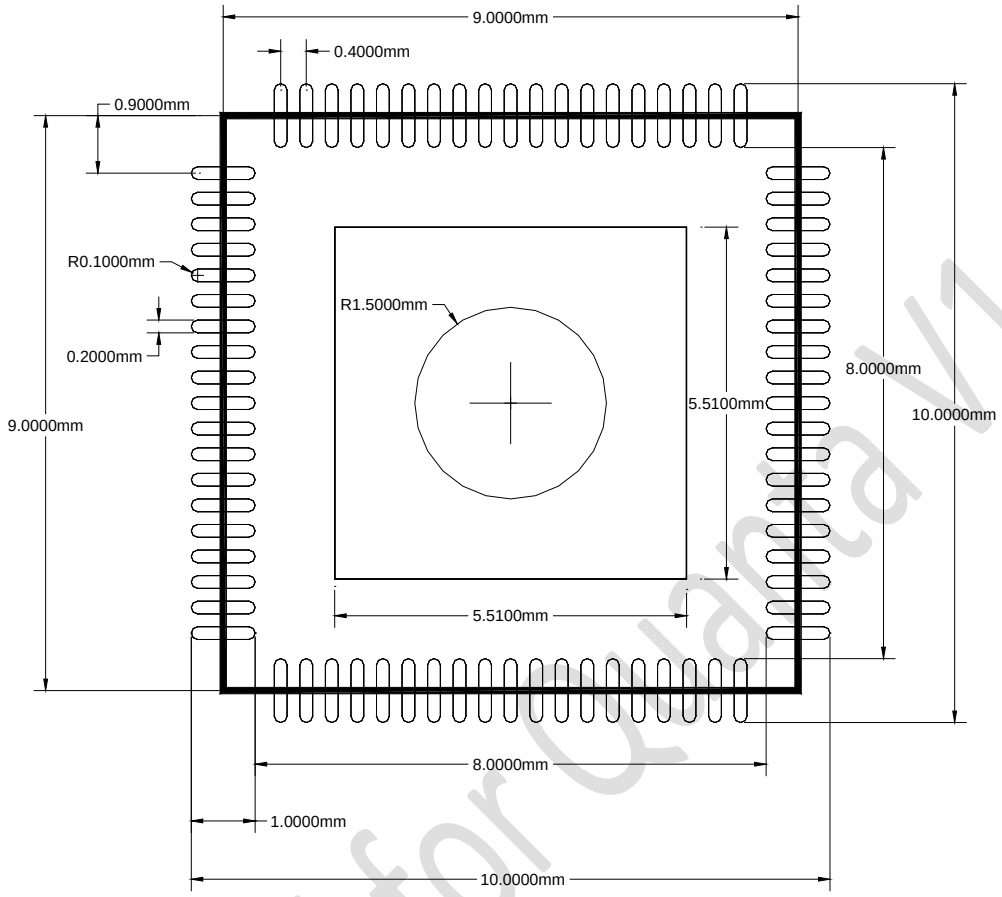


Figure 11-2

Package materials information

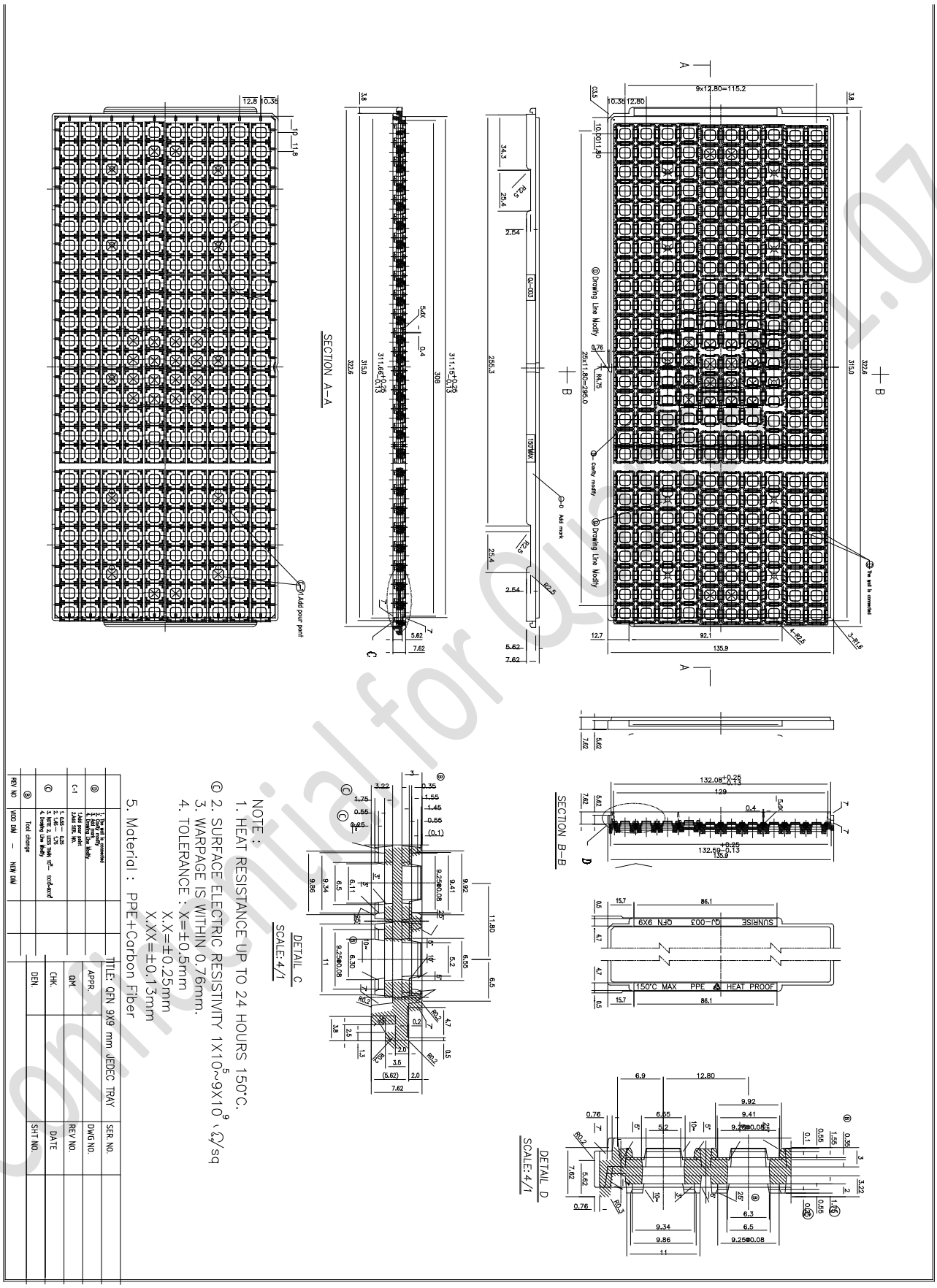


Figure 11-3

Order Information

Table 11

Type	Quantity	Part Number
Tray	260pcs/Tray 10Trays/package	AXP288/AXP288C/AXP288D