Data Sheet

LTC7890

Low I_Q, Dual, 2-Phase Synchronous Step-Down Controller for GaN FETs

FEATURES

- GaN drive technology fully optimized for GaN FETs
- Wide V_{IN} range: 4 V to 100 V
- Wide output voltage range: 0.8 V ≤ V_{OUT} ≤ 60 V
- No catch, clamp, or bootstrap diodes needed
- Internal smart bootstrap switches prevent overcharging of high-side driver supplies
- Internally optimized, smart near zero dead times or resistor adjustable dead times
- Split output gate drivers for adjustable turn on and turn off driver strengths
- Accurate adjustable driver voltage and UVLO
- Low I_Q: 5 µA (48 V_{IN} to 5 V_{OUT}, Ch 1 On)
- Programmable frequency (100 kHz to 3 MHz)
- Synchronizable frequency (100 kHz to 3 MHz)
- Spread spectrum frequency modulation
- 40-lead (6 mm × 6 mm), side wettable, QFN package

APPLICATIONS

- Industrial power systems
- Military avionics and medical systems
- Telecommunications power systems

GENERAL DESCRIPTION

The LTC7890 is a high performance, dual step-down, dc-to-dc switching regulator controller that drives all N-channel synchronous gallium nitride (GaN) field effect transistor (FET) power stages from input voltages up to 100 V. The LTC7890 solves many of the challenges traditionally faced when using GaN FETs. The LTC7890 simplifies the application design while requiring no protection diodes and no other additional external components compared to a silicon metal-oxide semiconductor field effect transistor (MOSFET) solution.

The internal smart bootstrap switches prevent overcharging of the BOOSTx pin to the SWx pin high-side driver supplies during dead times, protecting the gate of the top GaN FET. The LTC7890 internally optimizes the gate driver timing on both switching edges to achieve smart near zero dead times, significantly improving efficiency and allowing for high frequency operation, even at high input voltages. Alternatively, the user can adjust the dead times with external resistors for margin or to tailor the application.

The gate drive voltage of the LTC7890 can be precisely adjusted from 4 V to 5.5 V to optimize performance and to allow the use of different GaN FETs or even logic level MOSFETs.

TYPICAL APPLICATION CIRCUIT

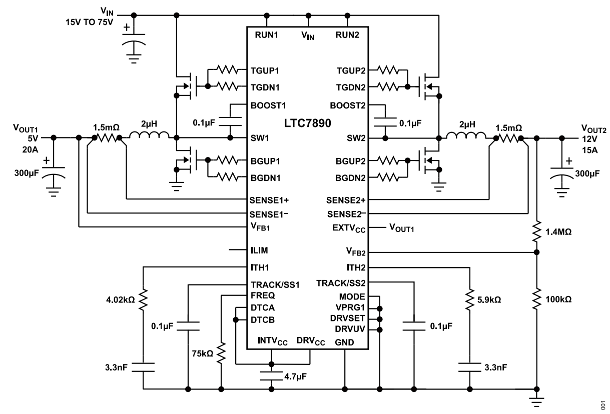

Figure 1. Typical Application Circuit

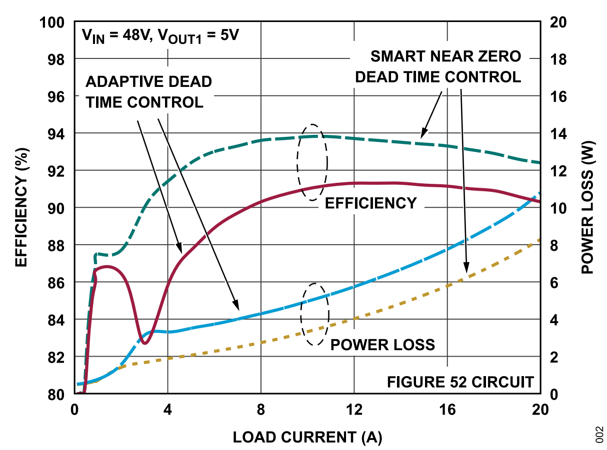

Figure 2. Efficiency and Power Loss vs. Load Current

Note that throughout this data sheet, multifunction pins, such as PLLIN/SPREAD, are referred to either by the entire pin name or by a single function of the pin, for example, PLLIN, when only that function is relevant.

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REVISION HISTORY

4/2023—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

T_J = −40°C to +150°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{IN} = 12 V, RUN1 and RUN2 = 12 V, VPRG1 = floating, $EXTV_{CC}$ = 0 V, DRVSET = 0 V, DRVUV = 0 V, TGUP1 = TGDN1 = TGxx1, BGUP1 = BGDN1 = BGxx1, TGUP2 = TGDN2 = TGxx2, BGUP2 = BGDN2 = BGxx2, and DTCA and DTCB = 0 V, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT SUPPLY						
Input Supply Operating Range	V_{IN}		4		100	V
Total Quiescent Supply Current in Regulation	I_Q	48 V to 5 V, no load, RUN2 = 0 V[1]		5		µA
		14 V to 3.3 V, no load, RUN2 = 0 V[1]		14		µA
CONTROLLER OPERATION						
Regulated Output Voltage Set Point	V_{OUT1}, V_{OUT2}		0.8		60	V
Channel 1 Regulated Feedback Voltage[2]	V_{FB1}	V_{IN} = 4 V to 100 V, ITH1 voltage = 0.6 V to 1.2 V				
		VPRG1 = floating, T_A = 25°C	0.792	0.8	0.808	V
		VPRG1 = floating	0.788	0.8	0.812	V
		VPRG1 = 0 V	4.925	5.0	5.075	V
		VPRG1 = $INTV_{CC}$	11.82	12	12.18	V
Channel 2 Regulated Feedback Voltage[2]	V_{FB2}	V_{IN} = 4 V to 100 V, ITH2 voltage = 0.6 V to 1.2 V				
		T_A = 25°C	0.792	0.8	0.808	V
			0.788	0.8	0.812	V
Channel 1 Feedback Current[2]		VPRG1 = floating, T_A = 25°C	–50	0	+50	nA
		VPRG1 = 0 V or $INTV_{CC}$, T_A = 25°C		1	2	µA
Channel 2 Feedback Current[2]		T_A = 25°C	–50	0	+50	nA
Feedback Overvoltage Threshold (Relative to V_{FBx})		T_A = 25°C	7	10	13	%
Transconductance Amplifier[2]	g_{M1}, g_{M2}	ITH1 and ITH2 = 1.2 V, sink and source current = 5 µA		1.8		mMho
Maximum Current Sense Threshold	$V_{SENSE(MAX)}$	V_{FBx} = 0.7 V, $SENSEx^-$ = 3.3 V				
		ILIM = 0 V	21	26	31	mV
		ILIM = floating	45	50	55	mV
		ILIM = $INTV_{CC}$	67	75	83	mV
$SENSE1^+$ and $SENSE2^+$ Pin Current	I_{SENSE1^+}, I_{SENSE2^+}	$SENSE1^+$ and $SENSE2^+$ = 3.3 V, T_A = 25°C	−1		+1	µA
$SENSE1^-$ Pin Current	I_{SENSE1^-}	$SENSE1^-$ < 3 V		1		µA
		3.2 V ≤ $SENSE1^-$ < $INTV_{CC}$ – 0.5 V		75		µA
		$SENSE1^-$ > $INTV_{CC}$ + 0.5 V		725		µA
$SENSE2^-$ Pin Current		$SENSE2^-$ < $INTV_{CC}$ – 0.5 V	–2		+2	µA
		$SENSE2^-$ > $INTV_{CC}$ + 0.5 V		650		µA
Soft Start Charge Current		TRACK/SS1 and TRACK/SS2 = 0 V	9.5	12	14.5	µA
RUNx Pin On Threshold		RUNx rising	1.15	1.20	1.25	V
RUNx Pin Hysteresis				120		mV
DC SUPPLY CURRENT						
V_{IN} Shutdown Current		RUN1 and RUN2 = 0 V		1		µA
V_{IN} Sleep Mode Current		$SENSE1^-$ < 3.2 V, $EXTV_{CC}$ = 0 V				
One Channel On				15		µA
Both Channels On				19		µA
Sleep Mode Current[3], Only Channel 1 On		$SENSE1^-$ ≥ 3.2 V				
V_{IN} Current		$EXTV_{CC}$ = 0 V		5		µA
V_{IN} Current		$EXTV_{CC}$ ≥ 4.8 V		1		µA
$EXTV_{CC}$ Current		$EXTV_{CC}$ ≥ 4.8 V		6		µA
$SENSE1^-$ Current				10		µA

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Sleep Mode Current[3], Both Channels On		SENSE1⁻ ≥ 3.2 V, $EXTV_{CC}$ ≥ 4.8 V				
V_{IN} Current				1		μA
$EXTV_{CC}$ Current				7		μA
SENSE1⁻ Current				12		μA
Pulse Skipping (PS) or Forced Continuous Mode (FCM), V_{IN} or $EXTV_{CC}$ Current[3]						
One Channel On				2		mA
Both Channels On				3		mA
GATE DRIVERS						
TGxxx or BGxxx On Resistance		DRVSET = $INTV_{CC}$				
Pull-Up				2.0		Ω
Pull-Down				1.0		Ω
BOOSTx to DRV_{CC} Switch On Resistance		DRVSET = $INTV_{CC}$		7		Ω
TGxxx or BGxxx Transition Time[4]						
Rise Time				25		ns
Fall Time				15		ns
TGxxx Off to BGxxx On Delay[4]		DTCA = 0 V				
Synchronous Switch On Delay Time				20		ns
BGxxx Off to TGxxx On Delay[4]		DTCB = 0 V				
Top Switch On Delay Time				20		ns
BGxxx Falling to SWx Rising Delay[5]		DTCB = $INTV_{CC}$ or resistor				
		DTCA = $INTV_{CC}$		2		ns
		DTCA = 50 kΩ		25		ns
		DTCA = 100 kΩ		40		ns
SWx Falling to BGxxx Rising Delay[5]		DTCA = $INTV_{CC}$ or resistor				
		DTCB = $INTV_{CC}$		0.5		ns
		DTCB = 50 kΩ		25		ns
		DTCB = 100 kΩ		40		ns
TGxxx Minimum On-Time[6]	$t_{ON(MIN)}$			40		ns
Maximum Duty Cycle		Output in dropout, FREQ = 0 V		99		%
LOW DROPOUT (LDO) LINEAR REGULATORS						
$INTV_{CC}$ Voltage for V_{IN} and $EXTV_{CC}$ LDOs		$EXTV_{CC}$ = 0 V for V_{IN} LDO, 12 V for $EXTV_{CC}$ LDO				
		DRVSET = $INTV_{CC}$	5.2	5.5	5.7	V
		DRVSET = 0 V	4.8	5.0	5.2	V
		DRVSET= 64.9 kΩ	4.5	4.75	5.0	V
DRV_{CC} Load Regulation		DRV_{CC} load current = 0 mA to 100 mA, T_A = 25°C		1	3	%
Undervoltage Lockout	UVLO					
DRV_{CC} Rising		DRVUV = $INTV_{CC}$	4.8	5.0	5.2	V
		DRVUV = 0 V	3.6	3.8	4.0	V
		DRVUV = floating	4.2	4.4	4.6	V
DRV_{CC} Falling		DRVUV = $INTV_{CC}$	4.55	4.75	4.95	V
		DRVUV = 0 V	3.4	3.6	3.8	V
		DRVUV = floating	4.0	4.18	4.4	V
$EXTV_{CC}$ LDO Switchover Voltage						
$EXTV_{CC}$ Rising		DRVUV = $INTV_{CC}$ or floating, T_A = 25°C	5.75	5.95	6.15	V
		DRVUV = 0 V, T_A = 25°C	4.6	4.76	4.9	V
$EXTV_{CC}$ Switchover Hysteresis						
$EXTV_{CC}$ Falling		DRVUV = $INTV_{CC}$ or floating		390		mV
		DRVUV = 0 V		220		mV

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SPREAD SPECTRUM OSCILLATOR AND PHASE-LOCKED LOOP (PLL)						
Fixed Frequency	f_{OSC}	PLLIN/SPREAD = 0 V				
Low Fixed Frequency		FREQ = 0 V, T_A = 25°C	320	370	420	kHz
High Fixed Frequency		FREQ = $INTV_{CC}$	2.0	2.25	2.5	MHz
Programmable Frequency		FREQ = 374 kΩ		100		kHz
		FREQ = 75 kΩ, T_A = 25°C	450	500	550	kHz
		FREQ = 12.5 kΩ		3		MHz
Synchronizable Frequency Range	f_{SYNC}	PLLIN/SPREAD = external clock	0.1		3	MHz
PLLIN Input High Level			2.2			V
PLLIN Input Low Level					0.5	V
Spread Spectrum Frequency Range (Relative to f_{OSC})		PLLIN/SPREAD = $INTV_{CC}$				
Minimum Frequency				0		%
Maximum Frequency				20		%
PGOODx OUTPUTS						
PGOODx Voltage Low		PGOODx = 2 mA, T_A = 25°C		0.2	0.4	V
PGOODx Leakage Current		PGOODx = 5 V, T_A = 25°C			±1	µA
PGOODx Trip Level (V_{FBx} with Respect to Set Regulated Voltage)		T_A = 25°C				%
V_{FBx} Rising			7	10	13	
Hysteresis				1.6		%
V_{FBx} Falling			−13	−10	−7	%
Hysteresis				1.6		%
PGOODx Delay for Reporting a Fault				25		µs

[1] This specification is not tested in production.

[2] The LTC7890 is tested in a feedback loop that servos ITHx voltage (V_{ITHx}) to a specified voltage and measures the resultant feedback voltage (V_{FBx}).

[3] SENSE1− bias current is reflected to the input supply by the formula $I_{VIN} = I_{SENSE1^-} \times V_{OUT1}/(V_{IN} \times \eta)$, where η is the efficiency.

[4] Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

[5] SWx falling to BGxxx rising and BGxxx falling to SWx rising delay times are measured at the rising and falling thresholds on SWx and BGxxx of approximately 1 V. See Figure 41 and Figure 42.

[6] The minimum on-time condition specified for inductor peak-to-peak ripple current is >40% of the maximum load current (I_{MAX}) (see the Minimum On-Time Considerations section).

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Rating
Input Supply (V_{IN})	–0.3 V to +100 V
RUN1 and RUN2	–0.3 V to +100 V
BOOST1 and BOOST2	–0.3 V to +106 V
SW1 and SW2	–5 V to +100 V
BOOST1 to SW1 and BOOST2 to SW2	–0.3 V to +6 V
BGUP1, BGDN1, BGUP2, and BGDN2[1]	Not applicable
TGUP1, TGDN1, TGUP2, and TGDN2[1]	Not applicable
$EXTV_{CC}$	–0.3 V to +30 V
DRV_{CC} and $INTV_{CC}$	–0.3 V to +6 V
V_{FB1}	–0.3 V to +15 V
V_{FB2}	–0.3 V to +6 V
PLLIN/SPREAD and FREQ	–0.3 V to +6 V
TRACK/SS1, TRACK/SS2, ITH1, and ITH2	–0.3 V to +6 V
DRVSET and DRVUV	–0.3 V to +6 V
MODE, ILIM, and VPRG1	–0.3 V to +6 V
PGOOD1 and PGOOD2	–0.3 V to +6 V
DTCA and DTCB	–0.3 V to +6 V
$SENSE1^+$, $SENSE2^+$, $SENSE1^-$, and $SENSE2^-$	–0.3 V to +65 V
$SENSE1^+$ to $SENSE1^-$ and $SENSE2^+$ to $SENSE2^-$	
Continuous	–0.3 V to +0.3 V
<1 ms	–100 mA to +100 mA
Operating Junction Temperature Range[2]	–40°C to +150°C
Storage Temperature Range	–65°C to +150°C

[1] Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only. Otherwise, permanent damage can occur.

[2] The LTC7890 is specified over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$, where θ_{JA} is the package thermal impedance and equals 34°C/W for the 40-lead (6 mm × 6 mm), side wettable, quad flat no lead (QFN) package.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

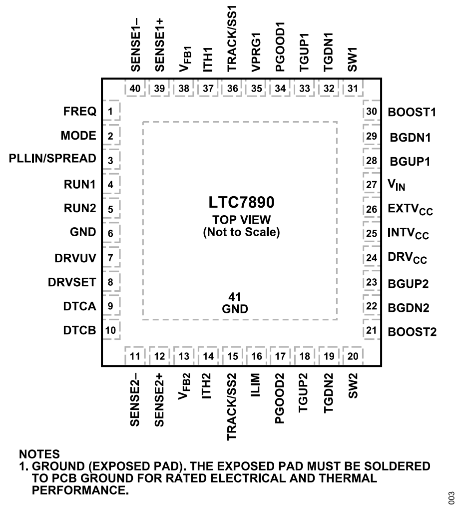

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FREQ	Frequency Control Pin for the Internal Voltage Controlled Oscillator (VCO). Connect FREQ to GND for a fixed frequency of 370 kHz. Connect FREQ to $INTV_{CC}$ for a fixed frequency of 2.25 MHz. Program frequencies between 100 kHz and 3 MHz by using a resistor between FREQ and GND. Minimize the capacitance on FREQ.
2	MODE	Mode Select Input. This input determines how the LTC7890 operates at light loads. Connect MODE to GND to select Burst Mode® operation. An internal 100 kΩ resistor to GND also invokes Burst Mode operation when MODE is floating. Connect MODE to $INTV_{CC}$ to force continuous inductor current operation. Tying MODE to $INTV_{CC}$ through a 100 kΩ resistor selects the pulse skipping operation.
3	PLLIN/SPREAD	External Synchronization Input to Phase Detector/Spread Spectrum Enable. When an external clock is applied to PLLIN/SPREAD, the PLL forces the rising TGxx1 signal to synchronize with the rising edge of the external clock. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator, or to GND to disable spread spectrum dithering.
4	RUN1	Run Control Input for Channel 1. Forcing RUN1 less than 1.08 V disables controller switching. Forcing RUN1 and RUN2 less than 0.7 V shuts down the LTC7890, reducing I_Q to approximately 1 µA. Tie the RUN1 pin to V_{IN} for always on operation.
5	RUN2	Run Control Input for Channel 2. Forcing RUN2 less than 1.08 V disables controller switching. Forcing RUN1 and RUN2 less than 0.7 V shuts down the LTC7890, reducing I_Q to approximately 1 µA. Tie the RUN2 pin to V_{IN} for always on operation.
6	GND	Ground. The GND pin and the exposed pad must be soldered to PCB ground for rated electrical and thermal performance.
7	DRVUV	DRV_{CC} UVLO and $EXTV_{CC}$ Switchover Program Pin. DRVUV determines the $INTV_{CC}$ UVLO and $EXTV_{CC}$ switchover rising and falling thresholds, as listed in Table 1.
8	DRVSET	$INTV_{CC}$ Regulation Program Pin. DRVSET sets the regulation point for the $INTV_{CC}$ LDO linear regulators. Connect DRVSET to GND to set $INTV_{CC}$ to 5 V. Connect DRVSET to $INTV_{CC}$ to set $INTV_{CC}$ to 5.5 V. Program voltages between 4 V and 5.5 V by placing a resistor (50 kΩ to 110 kΩ) between DRVSET and GND. The resistor and an internal 20 µA source current create a voltage used by the $INTV_{CC}$ LDO regulator to set the regulation point.
9	DTCA	Dead Time Control Pin for Bottom FET Off to Top FET On Delay. Connect DTCA to GND to program an adaptive dead time delay of approximately 20 ns. Connect DTCA to $INTV_{CC}$ to program a smart near zero delay between BGUPx falling and SWx rising. Connect a 10 kΩ to 200 kΩ resistor between DTCA and GND to add additional delay (from 7 ns to 60 ns) between BGUPx falling and SWx rising. This setting applies to both channels.
10	DTCB	Dead Time Control Pin for Top FET Off to Bottom FET On Delay. Connect DTCB to GND to program an adaptive dead time delay of approximately 20 ns. Connect DTCB to $INTV_{CC}$ to program a smart near zero delay between SWx falling and BGDNx rising. Connect a 10 kΩ to 200 kΩ resistor between DTCB and GND to add additional delay (from 7 ns to 60 ns) between SWx falling and BGDNx rising. This setting applies to both channels.
11	$SENSE2^-$	Negative Input to the Differential Current Comparator for Channel 2. The $SENSE2^-$ pin supplies current to the current comparator of Channel 2 when $SENSE2^-$ is greater than $INTV_{CC}$.
12	$SENSE2^+$	Positive Input to the Differential Current Comparator for Channel 2. The ITH2 pin voltage and controlled offset between the $SENSE2^-$ and $SENSE2^+$ pins, in conjunction with the current sense resistor (R_{SENSE}), set the current trip threshold.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 3. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
13	V_{FB2}	Error Amplifier Feedback Input for Channel 2. V_{FB2} receives the remotely sensed feedback voltage for Channel 2 from an external resistive divider across the output. Tie V_{FB2} to $INTV_{CC}$ for a 2-phase single output application, in which both channels share V_{FB1}, ITH1, and TRACK/SS1.
14	ITH2	Error Amplifier Output and Switching Regulator Compensation Point for Channel 2. The current comparator trip point increases with this control voltage.
15	TRACK/SS2	External Tracking/Soft Start Input for Channel 2. TRACK/SS2 regulates the V_{FB2} voltage to the lesser of 0.8 V or the voltage on the TRACK/SS2 pin. An internal 12 µA pull-up current source is connected to TRACK/SS2. A capacitor to GND at TRACK/SS2 sets the ramp time to the final regulated output voltage. The ramp time is equal to 1 ms for every 12.5 nF of capacitance. Alternatively, a resistor divider on another voltage supply connected to TRACK/SS2 allows the output to track the other supply during startup.
16	ILIM	Current Comparator Sense Voltage Range Input. Tying ILIM to GND or $INTV_{CC}$ or floating ILIM sets the maximum current sense threshold to one of three different levels (25 mV, 75 mV, or 50 mV, respectively).
17	PGOOD2	Power-Good Open-Drain Logic Output for Channel 2. PGOOD2 is pulled to GND when the voltage on V_{FB2} is not within ±10% of its set point.
18	TGUP2	High Current Gate Driver Pull-Up for Top FET for Channel 2. TGUP2 pulls up to BOOST2. Tie TGUP2 directly to the top FET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between TGUP2 and the top FET gate to adjust the gate rising slew rate.
19	TGDN2	High Current Gate Driver Pull-Down for Top FET for Channel 2. TGDN2 pulls down to SW2. Tie TGDN2 directly to the top FET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between TGDN2 and the top FET gate to adjust the gate falling slew rate.
20	SW2	Switch Node Connection to Inductor for Channel 2.
21	BOOST2	Bootstrapped Supply to the Top Side Floating Driver for Channel 2. Connect a capacitor between the BOOST2 and SW2 pins. An internal switch provides power to the BOOST2 pin from DRV_{CC} when the bottom FET turns on. The voltage swing at the BOOST2 pin is from DRV_{CC} to (V_{IN} + DRV_{CC}).
22	BGDN2	High Current Gate Driver Pull-Down for Bottom FET for Channel 2. BGDN2 pulls down to GND. Tie BGDN2 directly to the bottom FET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between BGDN2 and the bottom FET gate to adjust the gate falling slew rate. BGDN2 also serves as the Kelvin sense of the bottom FET gate during turn on.
23	BGUP2	High Current Gate Driver Pull-Up for Bottom FET for Channel 2. BGUP2 pulls up to DRV_{CC}. Tie BGUP2 directly to the bottom FET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between BGUP2 and the bottom FET gate to adjust the gate rising slew rate. BGUP2 also serves as the Kelvin sense of the bottom FET gate during turn off.
24	DRV_{CC}	Gate Driver Power Supply Pin. The gate drivers are powered from DRV_{CC}. Connect DRV_{CC} to $INTV_{CC}$ by a separate trace to the $INTV_{CC}$ bypass capacitor.
25	$INTV_{CC}$	Output of the Internal LDO Regulator. The $INTV_{CC}$ voltage regulation point is set by the DRVSET pin. $INTV_{CC}$ must be decoupled to GND with a 4.7 µF to 10 µF ceramic or other low equivalent series resistance (ESR) capacitor.
26	$EXTV_{CC}$	External Power Input to an Internal LDO Regulator Connected to DRVCC. This LDO regulator supplies $INTV_{CC}$ power, bypassing the internal V_{IN} LDO regulator whenever $EXTV_{CC}$ is higher than the $EXTV_{CC}$ switchover voltage. See the $EXTV_{CC}$ connection in the Power and Bias Supplies (VIN, EXTVCC, DRVCC, and INTVCC) section and INTVCC Regulators (OPTI-DRIVE) section. Do not exceed 30 V on $EXTV_{CC}$. Connect $EXTV_{CC}$ to GND if the $EXTV_{CC}$ LDO regulator is not used.
27	V_{IN}	Main Supply Pin. A bypass capacitor must be tied between V_{IN} and GND.
28	BGUP1	High Current Gate Driver Pull-Up for Bottom FET for Channel 1. BGUP1 pulls up to DRV_{CC}. Tie BGUP1 directly to the bottom FET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between BGUP1 and the bottom FET gate to adjust the gate rising slew rate. BGUP1 also serves as the Kelvin sense of the bottom FET gate during turn off.
29	BGDN1	High Current Gate Driver Pull-Down for Bottom FET for Channel 1. BGDN1 pulls down to GND. Tie BGDN1 directly to the bottom FET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between BGDN1 and the bottom FET gate to adjust the gate falling slew rate. BGDN1 also serves as the Kelvin sense of the bottom FET gate during turn on.
30	BOOST1	Bootstrapped Supply to the Top Side Floating Driver for Channel 1. Connect a capacitor between the BOOST1 and SW1 pins. An internal switch provides power to the BOOST1 pin from DRV_{CC} when the bottom FET turns on. The voltage swing at the BOOST1 pin is from DRV_{CC} to (V_{IN} + DRV_{CC}).
31	SW1	Switch Node Connection to Inductor for Channel 1.
32	TGDN1	High Current Gate Driver Pull-Down for Top FET for Channel 1. TGDN1 pulls down to SW1. Tie TGDN1 directly to the top FET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between TGDN1 and the top FET gate to adjust the gate falling slew rate.
33	TGUP1	High Current Gate Driver Pull-Up for Top FET for Channel 1. TGUP1 pulls up to BOOST1. Tie TGUP1 directly to the top FET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between TGUP1 and the top FET gate to adjust the gate rising slew rate.
34	PGOOD1	Power-Good Open-Drain Logic Output for Channel 1. PGOOD1 is pulled to GND when the voltage on V_{FB1} is not within ±10% of its set point.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 3. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
35	VPRG1	Output Voltage Control Pin for Channel 1. VPRG1 sets the adjustable output mode for Channel 1 using the external feedback resistors or the fixed 12 V or 5 V output mode. Floating VPRG1 programs the output from 0.8 V to 60 V with an external resistor divider, regulating V_{FB1} to 0.8 V. Connect VPRG1 to $INTV_{CC}$ or GND to program the output to 12 V or 5 V, respectively, through an internal resistor divider on V_{FB1}.
36	TRACK/SS1	External Tracking/Soft Start Input for Channel 1. TRACK/SS1 regulates the V_{FB1} voltage to the lesser of 0.8 V or the voltage on the TRACK/SS1 pin. An internal 12 µA pull-up current source is connected to TRACK/SS1. A capacitor to GND at TRACK/SS1 sets the ramp time to the final regulated output voltage. The ramp time is equal to 1 ms for every 12.5 nF of capacitance. Alternatively, a resistor divider on another voltage supply connected to TRACK/SS1 allows the output to track the other supply during startup.
37	ITH1	Error Amplifier Output and Switching Regulator Compensation Point for Channel 1. The current comparator trip point increases with this control voltage.
38	V_{FB1}	Error Amplifier Feedback Input for Channel 1. If VPRG1 is floating, V_{FB1} receives the remotely sensed feedback voltage for Channel 1 from an external resistive divider across the output. If VPRG1 is tied to GND or $INTV_{CC}$, V_{FB1} receives the remotely sensed output voltage directly.
39	$SENSE1^+$	Positive Input to the Differential Current Comparator for Channel 1. The ITH1 pin voltage and controlled offset between the $SENSE1^-$ and $SENSE1^+$ pins, in conjunction with R_{SENSE}, set the current trip threshold.
40	$SENSE1^-$	Negative Input to the Differential Current Comparator for Channel 1. The $SENSE1^-$ pin supplies current to the current comparator of Channel 1 when $SENSE1^-$ is greater than $INTV_{CC}$. When $SENSE1^-$ is 3.2 V or greater, the pin supplies the majority of the sleep mode I_Q instead of V_{IN}, further reducing the input referred I_Q.
41	GND (EPAD)	Ground (Exposed Pad). The exposed pad must be soldered to PCB ground for rated electrical and thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

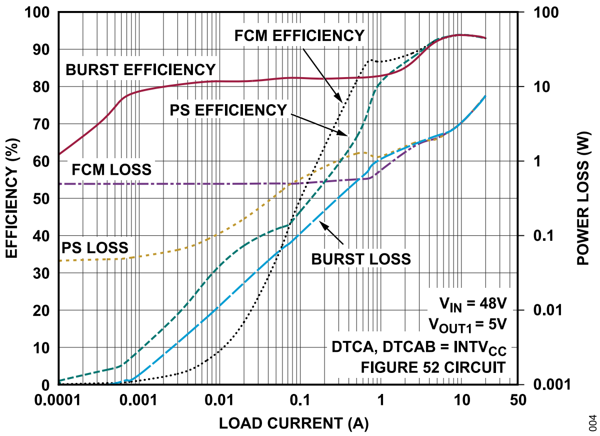

Figure 4. Efficiency and Power Loss vs. Load Current

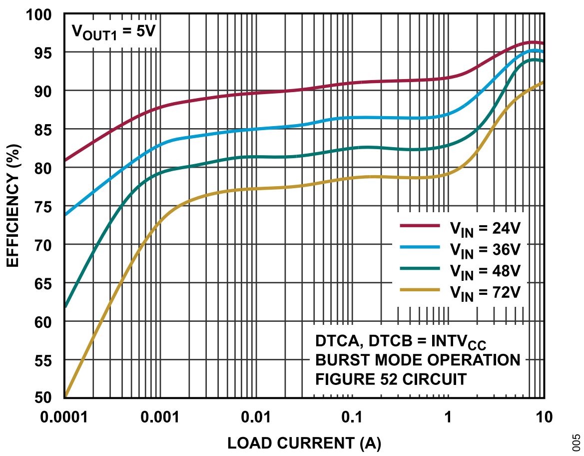

Figure 5. Efficiency vs. Load Current

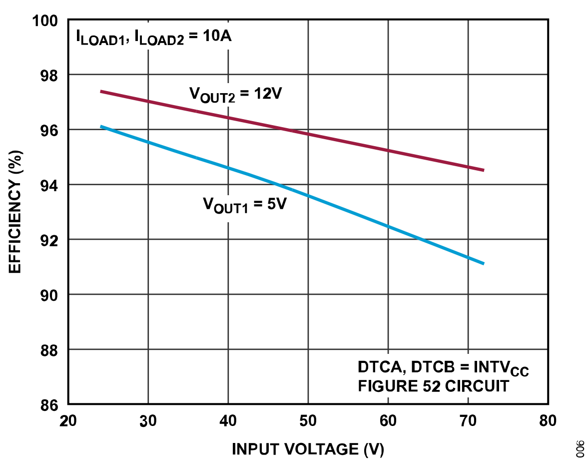

Figure 6. Efficiency vs. Input Voltage (I_{LOAD1}, I_{LOAD2} Are Load Currents)

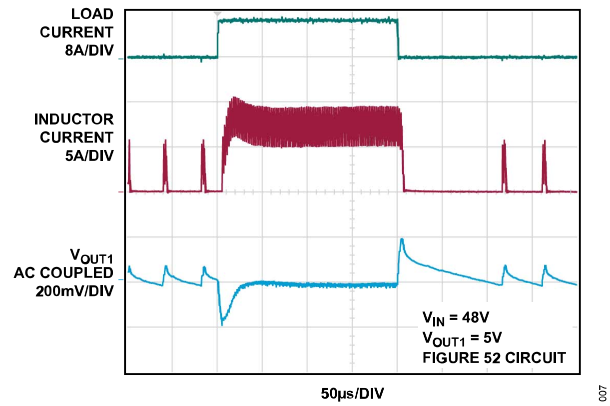

Figure 7. Load Step Burst Mode Operation

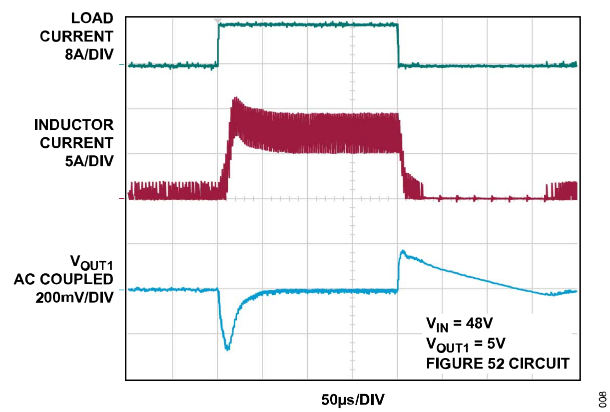

Figure 8. Load Step Pulse Skipping Mode

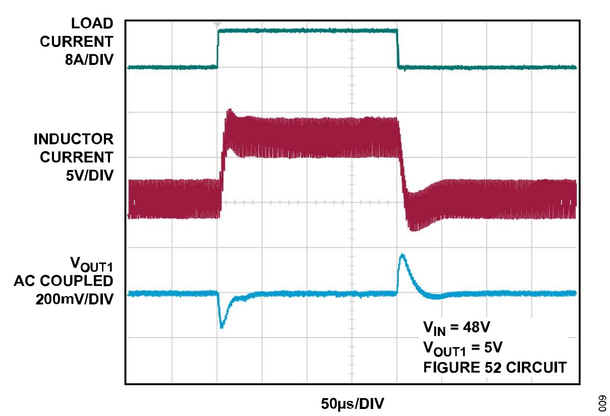

Figure 9. Load Step Forced Continuous Mode

TYPICAL PERFORMANCE CHARACTERISTICS

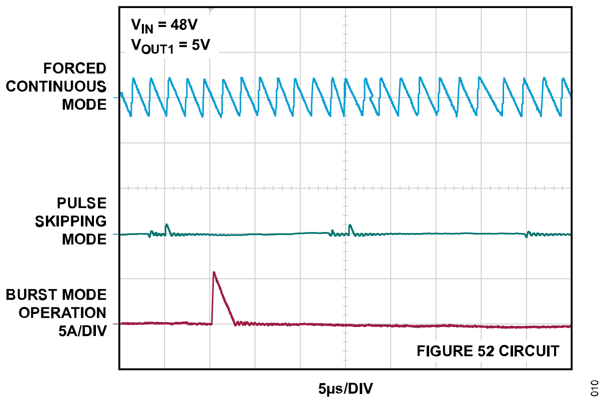

Figure 10. Inductor Current at Light Load

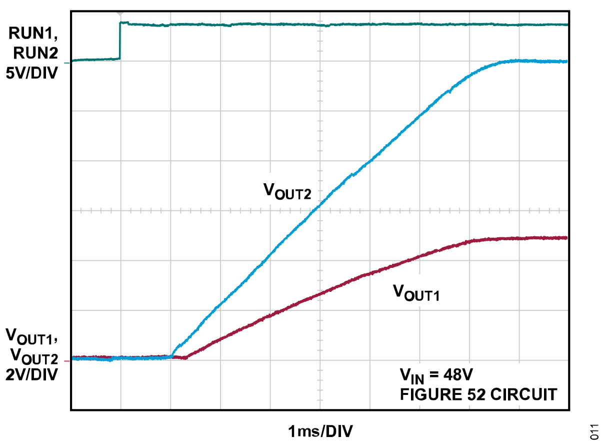

Figure 11. Soft Startup

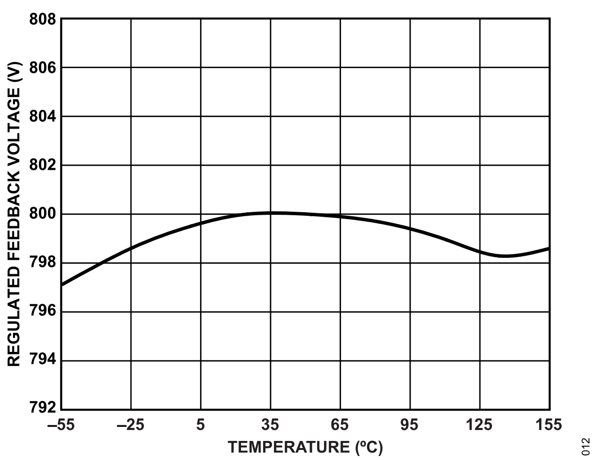

Figure 12. Regulated Feedback Voltage vs. Temperature

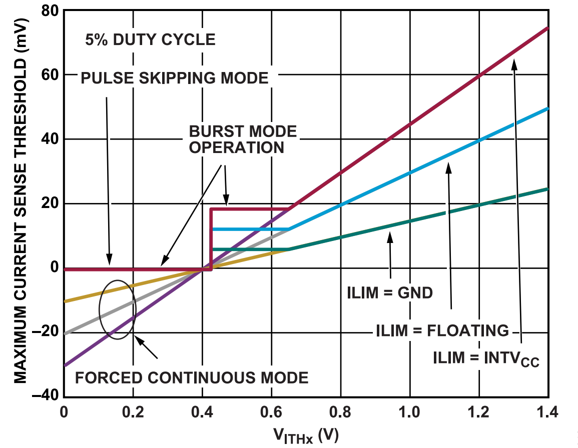

Figure 13. Maximum Current Sense Threshold vs. V_{ITHx}

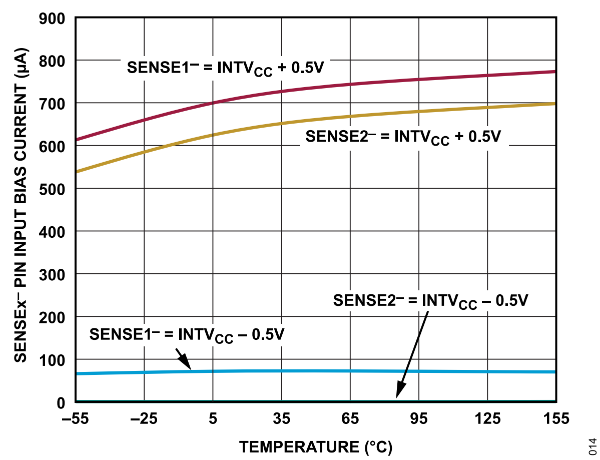

Figure 14. SENSEx– Pin Input Bias Current vs. Temperature

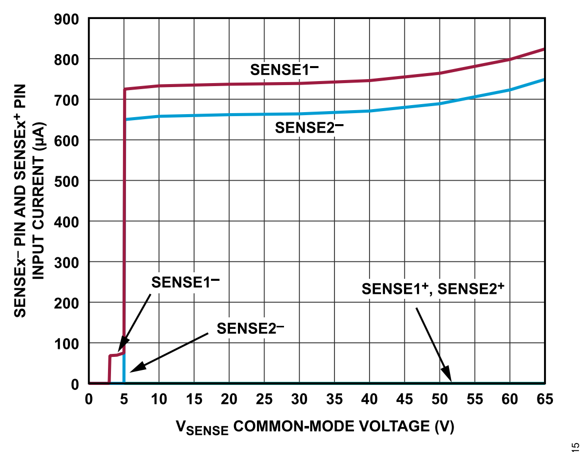

Figure 15. SENSEx– Pin and SENSEx+ Pin Input Current vs. V_{SENSE} Common-Mode Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

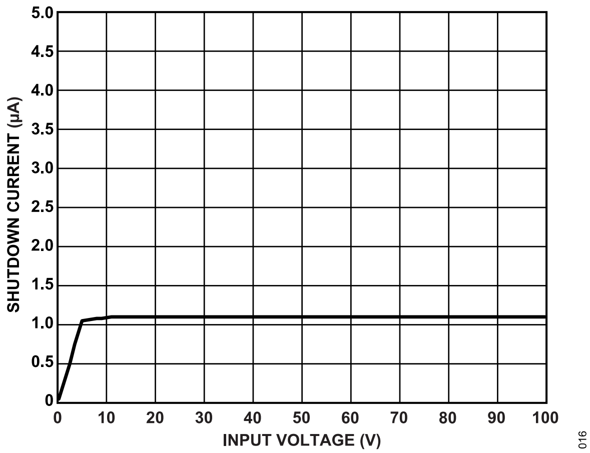

Figure 16. Shutdown Current vs. Input Voltage

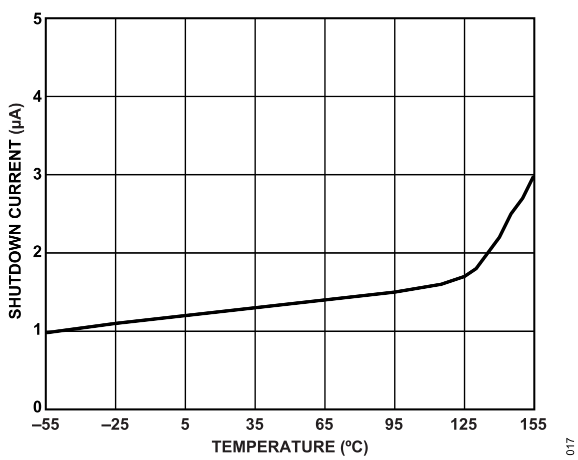

Figure 17. Shutdown Current vs. Temperature

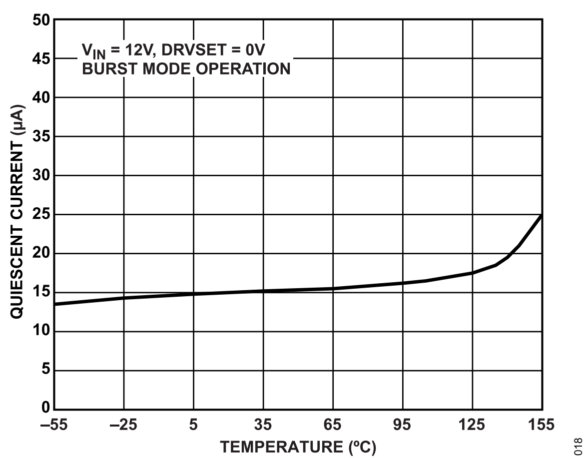

Figure 18. Quiescent Current vs. Temperature

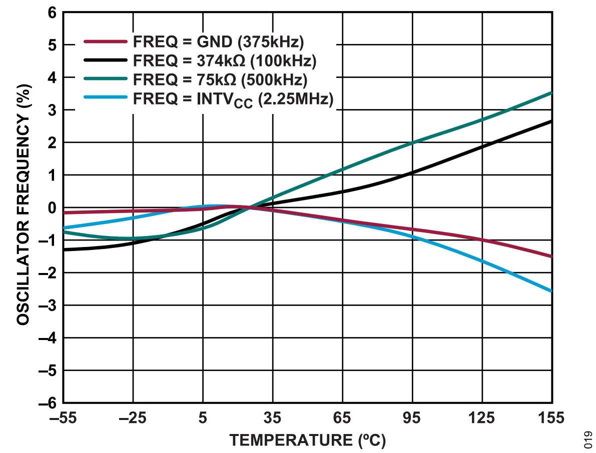

Figure 19. Oscillator Frequency vs. Temperature

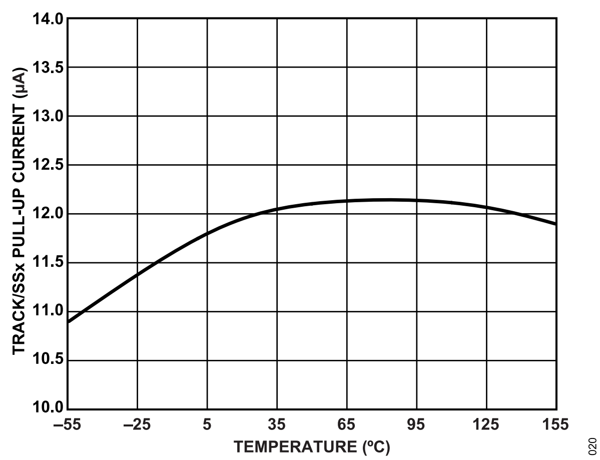

Figure 20. TRACK/SSx Pull-Up Current vs. Temperature

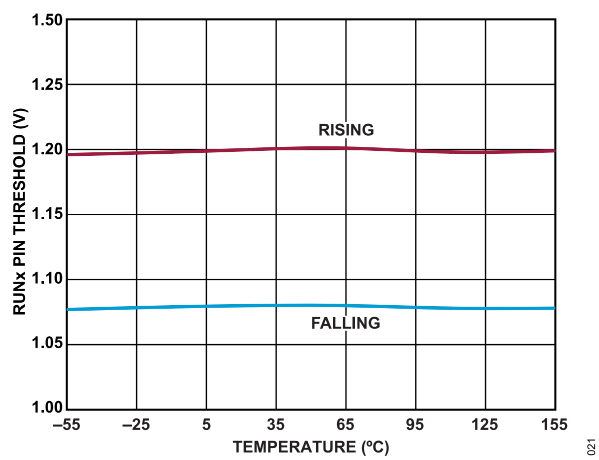

Figure 21. RUNx Pin Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

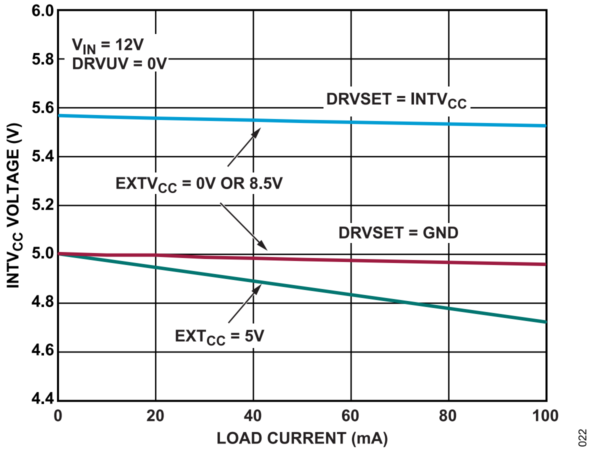

Figure 22. $INTV_{CC}$ Voltage vs. Load Current

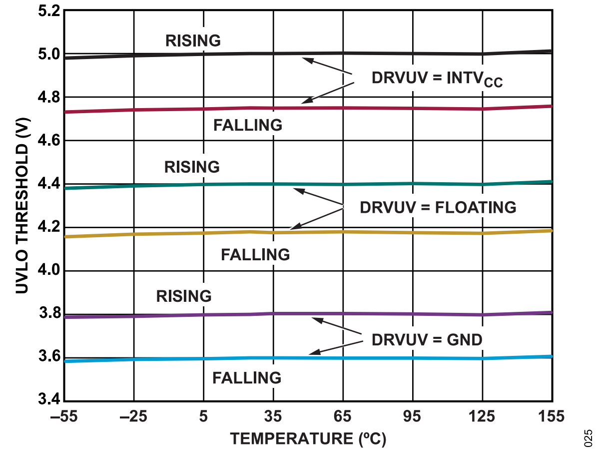

Figure 25. UVLO Threshold vs. Temperature

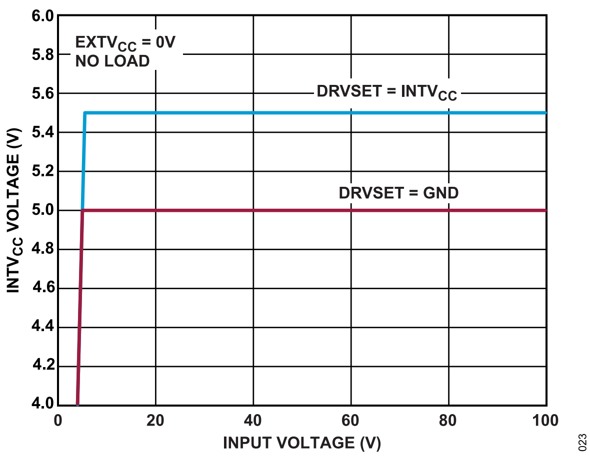

Figure 23. $INTV_{CC}$ Voltage vs. Input Voltage

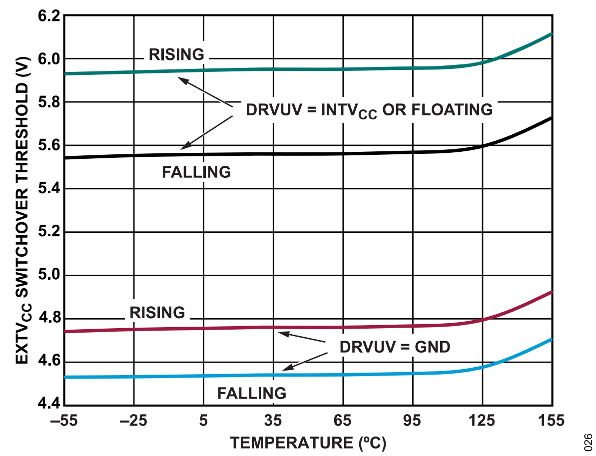

Figure 26. $EXTV_{CC}$ Switchover Threshold vs. Temperature

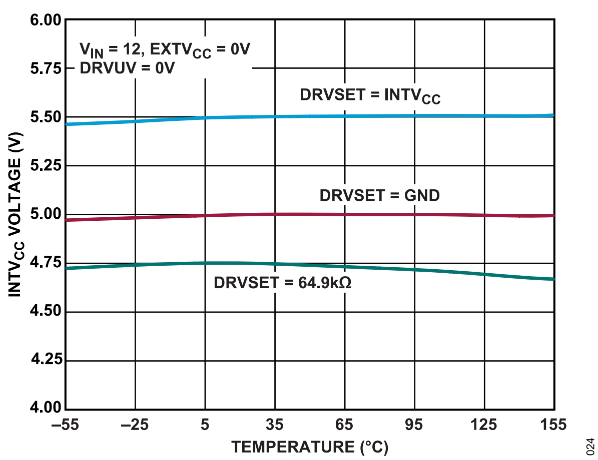

Figure 24. $INTV_{CC}$ Voltage vs. Temperature

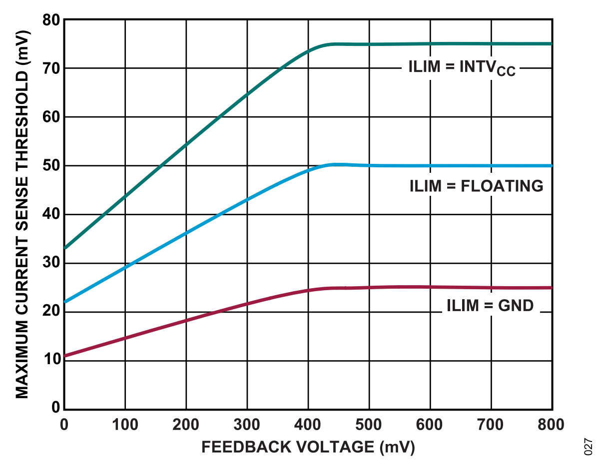

Figure 27. Maximum Current Sense Threshold vs. Feedback Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

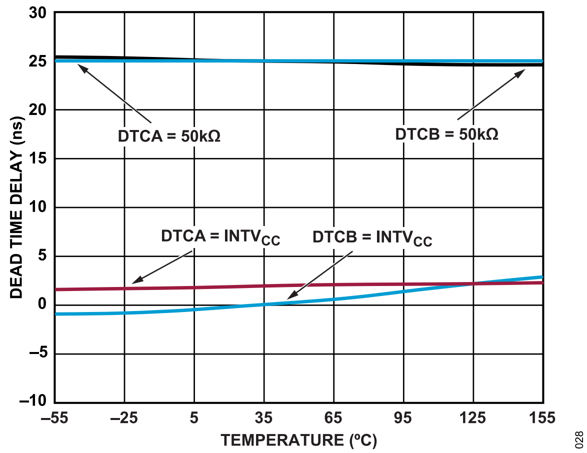

Figure 28. Dead Time Delay vs. Temperature

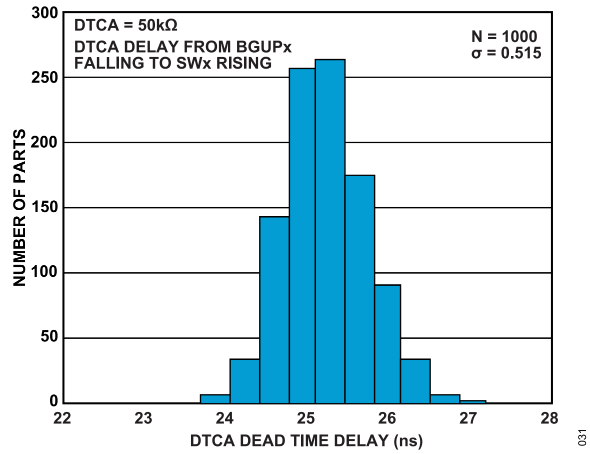

Figure 31. DTCA = 50 kΩ Dead Time Delay Histogram

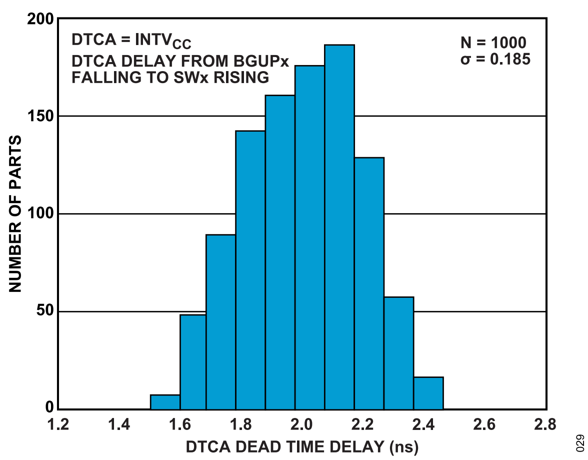

Figure 29. Smart Near Zero DTCA Dead Time Delay Histogram (δ Is the Standard Deviation of Dead Time Delay)

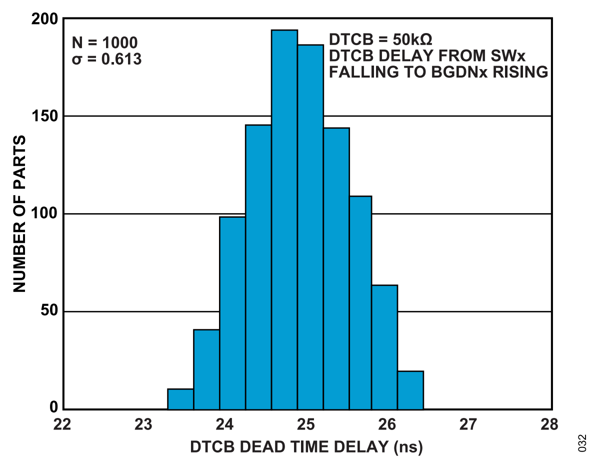

Figure 32. DTCB = 50 kΩ Dead Time Delay Histogram

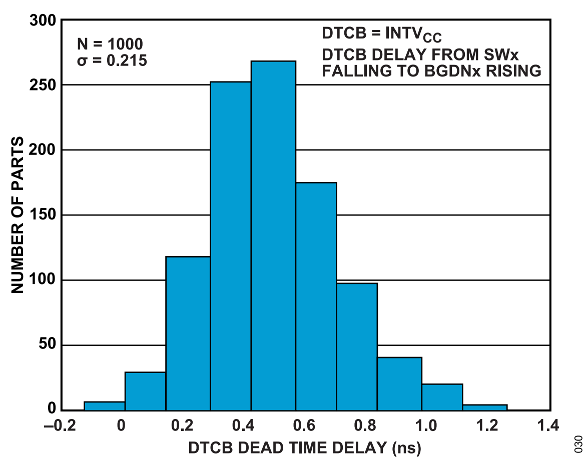

Figure 30. Smart Near Zero DTCB Dead Time Delay Histogram

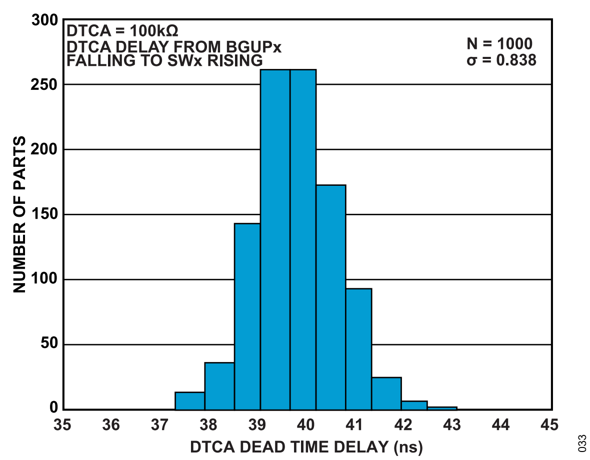

Figure 33. DTCA = 100 kΩ Dead Time Delay Histogram

TYPICAL PERFORMANCE CHARACTERISTICS

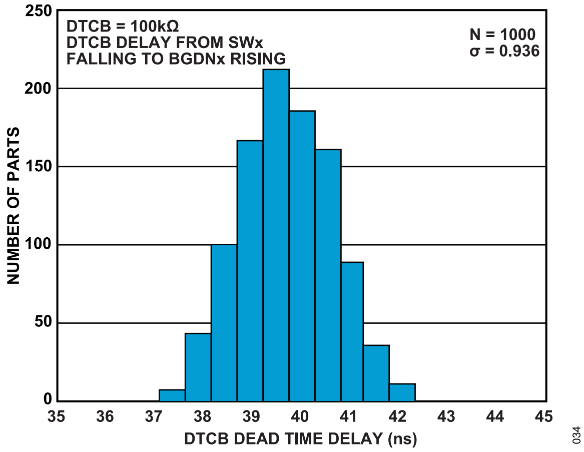

Figure 34. DTCB = 100 kΩ Dead Time Delay Histogram

THEORY OF OPERATION

FUNCTIONAL DIAGRAM

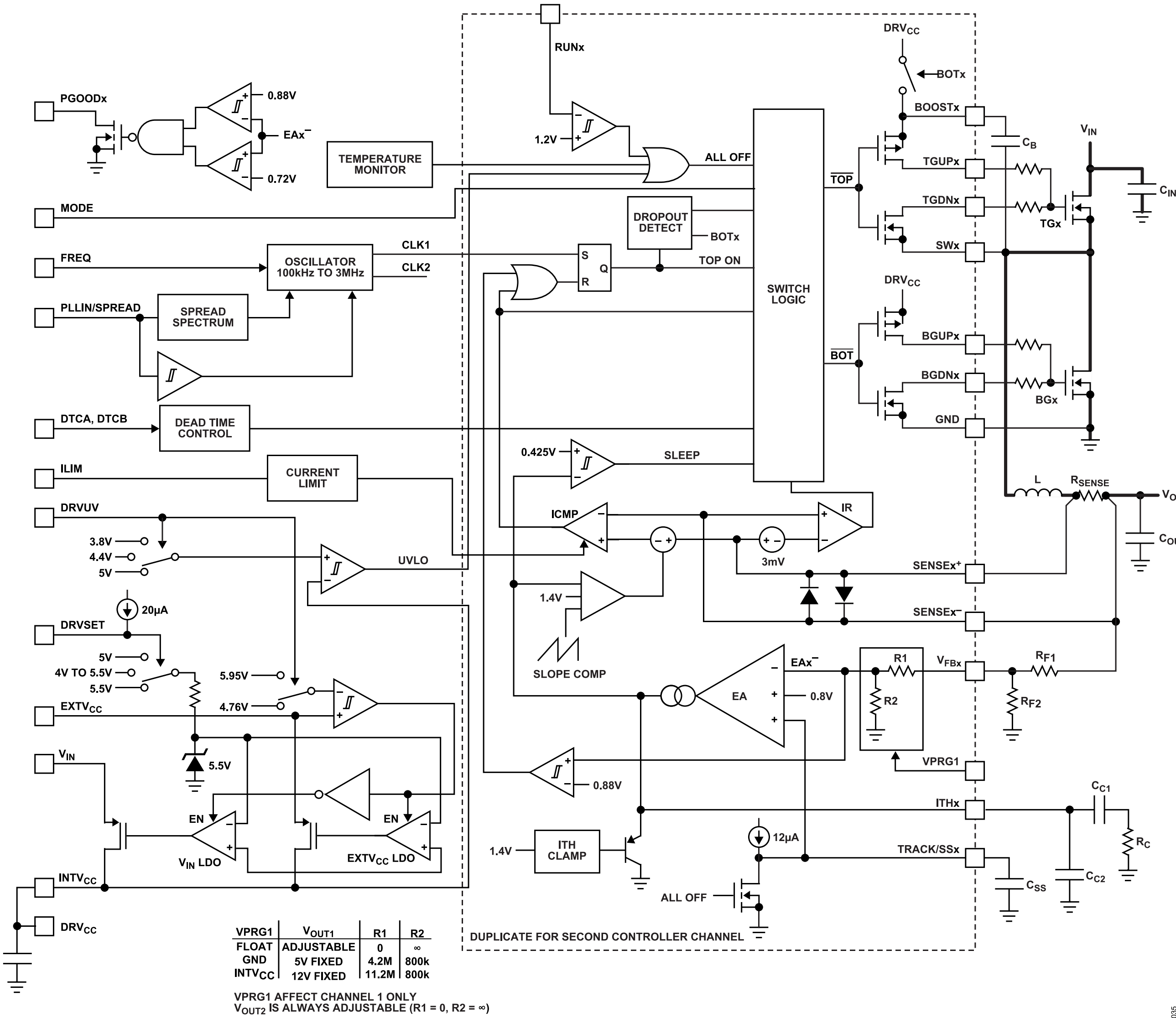

Figure 35. Functional Diagram

MAIN CONTROL LOOP

The LTC7890 is a dual synchronous controller using a constant frequency, peak current mode architecture. The two controller channels operate 180° out of phase, which reduces the required input capacitance and power supply induced noise. During normal operation, the external top FET turns on when the clock sets the set/reset (SR) latch, causing the inductor current to increase. The main switch turns off when the main current comparator, ICMP, resets the SR latch. After the top FET is turned off each cycle, the bottom FET turns on, which causes the inductor current to decrease until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier. The error amplifier compares the output voltage feedback signal at the V_{FBx} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUTx}, to GND) to the internal 0.8 V reference voltage. When the load current increases, it causes a slight decrease in V_{FBx} relative to the reference, which causes the error amplifier to increase the ITHx voltage until the average inductor current matches the new load current.

POWER AND BIAS SUPPLIES (V_{IN}, $EXTV_{CC}$, DRV_{CC}, AND $INTV_{CC}$)

The $INTV_{CC}$ pin supplies power for the top and bottom FET drivers and most of the internal circuitry. The supply for the FET drivers is derived from the DRV_{CC} pin, which must be tied to the $INTV_{CC}$ pin to supply power to the gate drivers. LDO linear regulators are

THEORY OF OPERATION

available from both the V_{IN} pin and the $EXTV_{CC}$ pin to provide power to $INTV_{CC}$, which can be programmed from 4 V to 5.5 V through control of the DRVSET pin. When the $EXTV_{CC}$ pin is tied to a voltage less than its switchover voltage, the V_{IN} LDO regulator supplies power to $INTV_{CC}$. If $EXTV_{CC}$ is taken more than its switchover voltage, the V_{IN} LDO regulator turns off and the $EXTV_{CC}$ LDO regulator turns on. When enabled, the $EXTV_{CC}$ LDO regulator supplies power to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source, such as the LTC7890 switching regulator output.

HIGH-SIDE BOOTSTRAP CAPACITOR

Each top FET driver is biased from the floating bootstrap capacitor (C_B), which normally recharges through an internal switch between BOOSTx and DRV_{CC} whenever the bottom FET turns on. The internal switch is high impedance whenever the bottom FET is off, which prevents the bootstrap capacitor from overcharging whenever SWx rings less than GND during the dead times.

If the input voltage decreases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top FET continuously. The dropout detector detects this event and forces the top FET off and the bottom FET on for a short time every tenth cycle to allow C_{Bx} to recharge, resulting in a 99% duty cycle at 370 kHz operation and approximately 98% duty cycle at 2 MHz operation. If the bootstrap capacitor voltage falls to approximately less than 75% of the $INTV_{CC}$ voltage, the boost refresh pulses increase to every fourth cycle to deliver more charge to C_{Bx}, resulting in slightly lower duty cycles in dropout.

DEAD TIME CONTROL (DTCA AND DTCB PINS)

The LTC7890 dead time delays can be programmed from near zero to 60 ns by configuring the DTCA and DTCB pins. The DTCA pin programs the dead time associated with the bottom FET turning off and the top FET turning on. The DTCB pin programs the dead time associated with top FET turning off and the bottom FET turning on. In this section, TGx represents the voltage sensed at the top FET gate and BGx represents the voltage sensed at the bottom FET gate.

Tying the DTCA pin to GND programs adaptive dead time control, which means the driver logic waits for the bottom FET to turn off before turning on the top FET. Adaptive dead time control results in dead times of approximately 20 ns between BGx falling to TGx rising.

Tying the DTCB pin to GND programs adaptive dead time control, which means the driver logic waits for the top FET to turn off before turning on the bottom FET. Adaptive dead time control results in dead times of approximately 20 ns between TGx falling to BGx rising.

Tying the DTCA pin to $INTV_{CC}$ programs smart near zero dead time control, which reduces the delay between the rising edge of SWx to the falling edge of BGx to near zero. Placing a resistor between the DTCA pin and GND adds additional delay between SWx rising and BGx falling from 7 ns to 60 ns. See the Dead Time Control (DTCA and DTCB Pins) section on dead time control for more information.

Tying the DTCB pin to $INTV_{CC}$ programs smart near zero dead time control, which reduces the delay between the falling edge of SWx to the rising edge of BGx to near zero. Placing a resistor between the DTCB pin and GND adds additional delay between SWx falling and BGx rising from 7 ns to 60 ns. See the Dead Time Control (DTCA and DTCB Pins) section on dead time control for more information.

STARTUP AND SHUTDOWN (RUNX AND TRACK/SSX PINS)

The two channels of the LTC7890 can be independently shut down using the RUN1 and RUN2 pins. Pulling a RUNx pin to less than 1.08 V shuts down the main control loop for that channel. Pulling both RUNx pins to less than 0.7 V disables both controllers and most internal circuits, including the $INTV_{CC}$ LDO regulators. In this shutdown state, the LTC7890 draws only 1 μA of I_B.

The RUNx pin must be externally pulled up or driven directly by logic. Each RUNx pin can tolerate up to 100 V (absolute maximum). Therefore, the RUNx pin can be tied to V_{IN} in always on applications where one or both controllers are enabled continuously and never shut down. Additionally, a resistive divider from V_{IN} to a RUNx pin can be used to set a precise input UVLO so that the power supply does not operate to less than the user adjustable level.

The startup of each channel's V_{OUTx} is controlled by the voltage on the corresponding TRACK/SSx pin. When the voltage on the TRACK/SSx pin is less than the 0.8 V internal reference voltage, the LTC7890 regulates the V_{FBx} voltage to the TRACK/SSx pin voltage instead of the 0.8 V reference voltage. This method allows the TRACK/SSx pin to be used as a soft start, which smoothly ramps the output voltage on startup, limiting the input supply inrush current. An external capacitor from the TRACK/SSx pin to GND is charged by an internal 12 μA pull-up current, creating a voltage ramp on the TRACK/SSx pin. As the TRACK/SSx voltage rises linearly from 0 V to 0.8 V (and beyond), V_{OUTx} rises smoothly from zero to its final value.

Alternatively, the TRACK/SSx pin can make the startup of V_{OUTx} track that of another supply. Typically, this tracking requires connecting to the TRACK/SSx pin through an external resistor divider from the other supply to GND (see the RUNx Pins and Undervoltage Lockout section and Soft Start and Tracking (TRACK/SSx Pin) section).

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LIGHT LOAD OPERATION: BURST MODE OPERATION, PULSE SKIPPING MODE, OR FORCED CONTINUOUS MODE (MODE PIN)

The LTC7890 can be set to enter high efficiency Burst Mode operation, constant frequency pulse skipping mode, or forced continuous conduction mode at light load currents.

To select Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse skipping mode, tie the MODE pin to a dc voltage greater than 1.2 V and less than $INTV_{CC}$ – 1.3 V. An internal 100 kΩ resistor to GND invokes Burst Mode operation when the MODE pin is floating, and pulse skipping mode when the MODE pin is tied to $INTV_{CC}$ through an external 100 kΩ resistor.

When the controllers are enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of its maximum value, even though the voltage on the ITHx pin may indicate a lower value. If the average inductor current is higher than the load current, the error amplifier decreases the voltage on the ITHx pin. When the ITHx voltage drops to less than 0.425 V, the internal sleep signal goes high (enabling sleep mode) and both external FETs turn off. The ITHx pin is then disconnected from the output of the error amplifier and parked at 0.45 V.

In sleep mode, much of the internal circuitry turns off, reducing the I_Q drawn by the LTC7890. If one channel is in sleep mode and the other channel is shut down, the LTC7890 draws only 15 µA of I_Q. If both channels are in sleep mode, the LTC7890 draws only 20 µA of I_Q. When V_{OUT} on Channel 1 is 3.2 V or higher, the majority of this I_Q is supplied by the $SENSE1^-$ pin, which further reduces the input referred I_Q by the ratio of V_{IN}/V_{OUT} multiplied by the efficiency.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the output of the error amplifier rises. When the output voltage drops enough, the ITHx pin is reconnected to the output of the error amplifier, the sleep signal goes low, and the controller resumes normal operation by turning on the top FET on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the bottom FET just before the inductor current reaches zero, preventing it from reversing and going negative. Therefore, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITHx pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

When the MODE pin is connected for pulse skipping mode, the LTC7890 operates in pulse-width modulation (PWM) pulse skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At light loads, ICMP can remain tripped for several cycles and force the top FET to stay off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference, as compared to Burst Mode operation. Pulse skipping mode provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Unlike forced continuous mode and pulse skipping mode, Burst Mode operation cannot be synchronized to an external clock. Therefore, if Burst Mode operation is selected and the switching frequency is synchronized to an external clock applied to the PLLIN/SPREAD pin, the LTC7890 switches from Burst Mode operation to forced continuous mode.

FREQUENCY SELECTION, SPREAD SPECTRUM, AND PHASE-LOCKED LOOP (FREQ AND PLLIN/SPREAD PINS)

The free running switching frequency of the LTC7890 controller is selected using the FREQ pin. Tying FREQ to GND selects 370 kHz, whereas tying FREQ to $INTV_{CC}$ selects 2.25 MHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 100 kHz and 3 MHz.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the LTC7890 can operate in spread spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency within typical boundaries of the frequency set by the FREQ pin and +20%.

A phase-locked loop (PLL) is available on the LTC7890 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. The PLL of the LTC7890 aligns the turn-on of the external top FET of Channel 1 to the rising edge of the synchronizing signal. The turn-on of the external top FET of Channel 2 is 180° out of phase to the rising edge of the external clock source.

The PLL frequency is prebiased to the free running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only must make slight changes to synchronize the rising edge of the external clock to the rising edge of TG1. For more rapid lock in to the external clock, use the FREQ pin to set the internal oscillator to approximately the frequency of the external clock. The PLL of the LTC7890 is guaranteed to lock to an external clock source whose frequency is between 100 kHz and 3 MHz.

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The PLLIN/SPREAD pin is transistor-transistor logic (TTL)-compatible with thresholds of 1.6 V (rising) and 1.1 V (falling), and this pin is guaranteed to operate with a clock signal swing of 0.5 V to 2.2 V.

OUTPUT OVERVOLTAGE PROTECTION

The LTC7890 has an overvoltage comparator for each channel that guards against transient overshoots as well as other more serious conditions that can cause output overvoltage. When the V_{FBx} pin rises more than 10% above its regulation point of 0.8 V, the top FET turns off, and the inductor current is not allowed to reverse.

FOLDBACK CURRENT

When the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft start interval (as long as the V_{FBx} voltage is keeping up with the TRACK/SSx voltage).

POWER-GOOD

The LTC7890 has a PGOODx pin for each channel that is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOODx pin low when the V_{FBx} voltage is not within ±10% of the 0.8 V reference. The PGOODx pin is also pulled low when the RUNx pin is low (shut down). When the V_{FBx} voltage is within the ±10% requirement, the MOSFET turns off, and the PGOODx pin is allowed to be pulled up by an external resistor to a source no greater than 6 V, such as $INTV_{CC}$.

APPLICATIONS INFORMATION

Figure 1 is a basic LTC7890 application circuit. External component selection is largely driven by the load requirement and begins with the selection of the inductor, current sense components, operating frequency, and light load operating mode. The remaining power stage components, consisting of the input and output capacitors and power FETs, can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then, the remaining external components are selected, such as for soft start, biasing, and loop compensation.

INDUCTOR VALUE CALCULATION

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of FET switching and gate charge losses. In addition to this trade-off, the effect of the inductor value on the ripple current and low current operation must also be considered. The inductor value has a direct effect on the ripple current.

The maximum average inductor current ($I_{L(MAX)}$) is equal to the maximum output current. The peak current is equal to the average inductor current plus half of the inductor ripple current (ΔI_L), which decreases with higher inductance (L) or higher frequency (f) and increases with higher V_{IN}, as shown in Equation 1:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

Accepting larger values of ΔI_L allows the use of low inductance but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \times I_{L(MAX)}$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) cause this transition to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values cause the burst frequency to decrease.

INDUCTOR CORE SELECTION

When the value for L is known, select the type of inductor. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is dependent on the inductance value selected. As inductance increases, core losses decrease. However, because increased inductance requires more turns of wire, copper losses increase.

Ferrite designs have low core loss and are preferred for high switching frequencies. Therefore, design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This collapse results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

CURRENT SENSE SELECTION

The LTC7890 can be configured to use either inductor dc resistance (DCR) sensing or low value resistor sensing. The choice between the two current sensing schemes is a design trade-off between cost, power consumption, and accuracy. DCR sensing is popular because it saves on expensive current sensing resistors and is more power efficient, particularly in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. The selection of other external components is driven by the load requirement and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and the inductor value.

The SENSEx$^+$ and SENSEx$^-$ pins are the inputs to the current comparator. The common-mode voltage range on these pins is 0 V to 65 V (the absolute maximum), enabling the LTC7890 to regulate output voltages up to a maximum of 60 V. The SENSEx$^+$ pin is high impedance, drawing less than ≈1 µA. This high impedance allows the current comparator to be used in inductor DCR sensing. The impedance of the SENSEx$^-$ pin changes depending on the common-mode voltage. When less than $INTV_{CC}$ – 0.5 V, the SENSEx$^-$ pin is relatively high impedance, drawing ≈75 µA for SENSE1$^-$ and ≈1 µA for SENSE2$^-$. When the SENSEx$^-$ pin is more than $INTV_{CC}$ + 0.5 V, a higher current (≈700 µA) flows into the pin. Between $INTV_{CC}$ – 0.5 V and $INTV_{CC}$ + 0.5 V, the current transitions from the smaller current to the higher current. The SENSE1$^-$ pin has an additional ≈75 µA current when its voltage is above 3.2 V to bias internal circuitry from V_{OUT1} instead of V_{IN}, which reduces the input referred supply current.

Filter components mutual to the sense lines must be placed close to the LTC7890, and the sense lines must run close together to a Kelvin connection underneath the current sense element (shown in Figure 36). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (see Figure 38), the R1 resistor must be placed close to the switching node to prevent noise from coupling into sensitive small signal nodes.

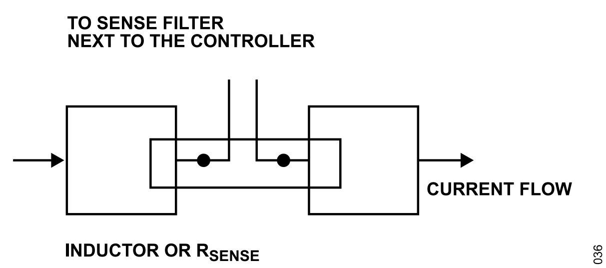

Figure 36. Sense Lines Placement with Inductor or Sense Resistor

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LOW VALUE RESISTOR CURRENT SENSING

Figure 37 shows a typical sensing circuit using a discrete resistor. R_{SENSE} is chosen based on the required output current. The current comparator of the controller has a $V_{SENSE(MAX)}$ of 50 mV, 25 mV, or 75 mV, as determined by the state of the ILIM pin. The current comparator threshold voltage sets the peak inductor current.

Using the maximum inductor current ($I_{L(MAX)}$) and ripple current (ΔI_L) (as described in the Inductor Value Calculation section), the target sense resistor value is given by Equation 2, as follows:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (2)$$

To ensure that the application delivers the full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in Table 1.

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal for lower inductor value (<3 µH) or higher current (>5 A) applications. This error is proportional to the input voltage and can degrade line regulation or cause loop instability. Placing an RC filter (filter resistor, R_F and filter capacitor, C_F) into the SENSEx$^+$ and SENSEx$^-$ pins, as shown in Figure 37, can be used to compensate for this error. For optimal cancellation of the ESL, set the RC filter time constant to $R_F \times C_F = ESL/R_{SENSE}$. In general, select C_F to be in the range of 1 nF to 10 nF and calculate the corresponding R_F. Surface-mount sense resistors in low ESL, wide footprint geometries are recommended to minimize this error. If not specified in the data sheet of the manufacturer, the ESL can be approximated as 0.4 nH for a resistor with a 1206 footprint and 0.2 nH for a resistor with a 1225 footprint.

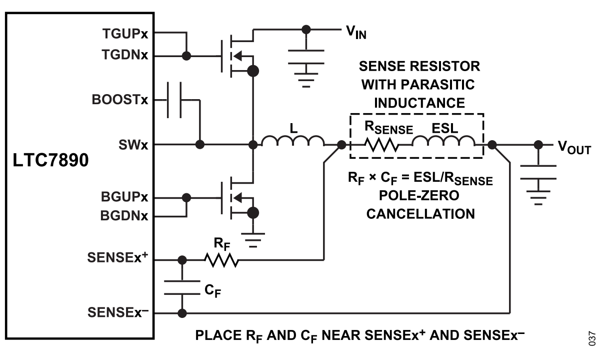

Figure 37. Using a Resistor to Sense Current

INDUCTOR DCR CURRENT SENSING

For applications requiring the highest possible efficiency at high load currents, the LTC7890 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 38. The DCR of the inductor represents the small amount of dc winding resistance of the copper, which can be less than 1 mΩ for low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor costs several points of efficiency compared to inductor DCR sensing.

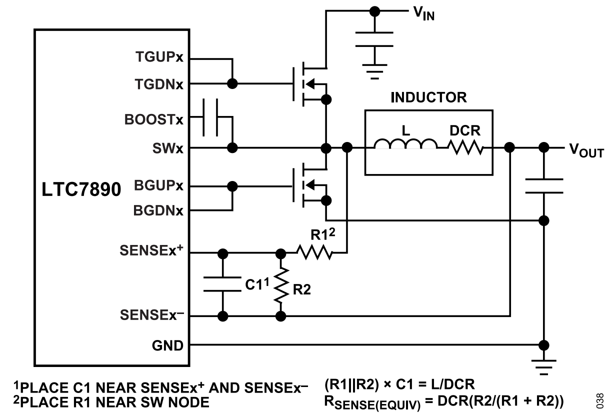

Figure 38. Using the Inductor DCR to Sense Current ($R_{SENSE(EQUIV)}$ Is Equivalent Sensed Resistance)

If the external (R1||R2) × C1 time constant is chosen to be equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. The DCR can be measured using an inductance, capacitance, and resistance (LCR) meter. However, the DCR tolerance is not always the same and varies with temperature. Consult the data sheet of the manufacturer for detailed information.

Using $I_{L(MAX)}$ and ΔI_L (as described in the Inductor Value Calculation section), the target sense resistor value is given by Equation 3, as follows:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (3)$$

To ensure that the application delivers the full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in Table 1.

Next, determine the DCR of the inductor. When provided, use the maximum value noted by the manufacturer, typically given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C. To scale the maximum inductor DCR (DCR_{MAX}) to the desired sense resistor (R_D) value, use the divider ratio given by Equation 4, as follows:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}} \quad (4)$$

C1 is typically selected to be in the range of 0.1 µF to 0.47 µF. This range forces the equivalent resistance (R1||R2) to around

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2 kΩ, reducing the error that can result from the ≈1 μA current of the SENSEx+ pin.

R1||R2 is scaled to the room temperature inductance and the maximum DCR given by Equation 5, as follows:

$$R1 \parallel R2 = \frac{L}{(\text{DCR at } 20°\text{C}) \times C1} \quad (5)$$

The sense resistor values are given by Equation 6 and Equation 7, as follows:

$$R1 = \frac{R1 \parallel R2}{R_D} \quad (6)$$

$$R2 = \frac{R1 \times R_D}{1 - R_D} \quad (7)$$

The maximum power loss (P_{LOSS}) in R1 is related to duty cycle and occurs in continuous mode at the maximum input voltage ($V_{IN(MAX)}$) given by Equation 8, as follows:

$$P_{LOSS} \ in \ R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \times V_{OUT}}{R1} \quad (8)$$

Ensure that R1 has a power rating higher than P_{LOSS} in R1. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses, and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

SETTING THE OPERATING FREQUENCY

Selecting the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses but requires larger inductance values and/or more output capacitance to maintain low output ripple voltage.

In higher voltage applications, transition losses contribute more significantly to power loss, and a proper balance between size and efficiency is achieved with a switching frequency between 300 kHz and 900 kHz. Lower voltage applications benefit from lower switching losses and can operate at switching frequencies up to 3 MHz, if desired. The switching frequency is set using the FREQ and PLLIN/SPREAD pins, as shown in Table 4.

Table 4. Setting the Switching Frequency Using FREQ and PLLIN/SPREAD

FREQ Pin	PLLIN/SPREAD Pin	Frequency
0 V	0 V	370 kHz
$INTV_{CC}$	0 V	2.25 MHz
Resistor to GND	0 V	100 kHz to 3 MHz
0 V, $INTV_{CC}$, or Resistor to GND	External clock, 100 kHz to 3 MHz	Phase-locked to external clock
0 V, $INTV_{CC}$, or Resistor to GND	$INTV_{CC}$	Spread spectrum, f_{OSC} modulated 0% to +20%

Tying the FREQ pin to GND selects 370 kHz, whereas tying FREQ to $INTV_{CC}$ selects 2.25 MHz. Placing a resistor between FREQ and GND allows the frequency to be programmed anywhere between 100 kHz and 3 MHz. Choose a FREQ pin resistor (R_{FREQ}) from Figure 39 or Equation 9, as follows:

$$R_{FREQ}(\text{in k}\Omega) = 37 \text{ MHz}/f_{OSC} \quad (9)$$

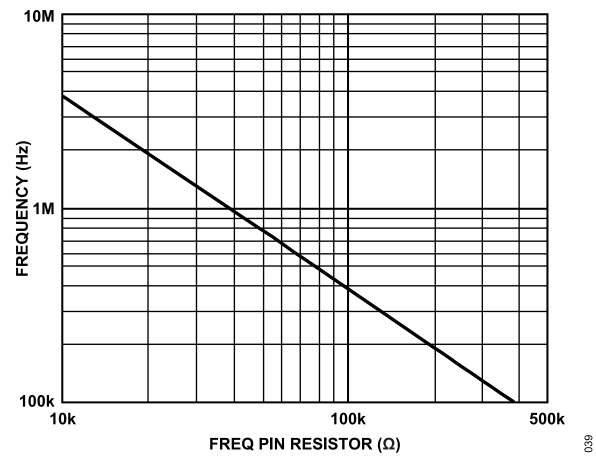

Figure 39. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

To improve EMI performance, spread spectrum mode can be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When spread spectrum mode is enabled, the switching frequency modulates within the frequency selected by the FREQ pin and +20%. Spread spectrum mode can be used in any operating mode selected by the MODE pin (Burst Mode, pulse skipping, or forced continuous mode).

A PLL is also available on the LTC7890 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. After the PLL locks, TGxx1 is synchronized to the rising edge of the external clock signal, and TGxx2 is 180° out of phase from TGxx1. See the Phase-Locked Loop and Frequency Synchronization section for details.

SELECTING THE LIGHT LOAD OPERATING MODE

The LTC7890 can be set to enter high efficiency Burst Mode operation, constant frequency pulse skipping mode, or forced continuous conduction mode at light load currents. To select Burst Mode

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operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse skipping mode, tie the MODE pin to $INTV_{CC}$ through a 100 kΩ resistor. An internal 100 kΩ resistor from the MODE pin to GND selects Burst Mode if the pin is floating. When synchronized to an external clock through the PLLIN/SPREAD pin, the LTC7890 operates in pulse skipping mode if it is selected. Otherwise, the LTC7890 operates in forced continuous mode. Table 5 summarizes the use of the MODE pin to select the light load operating mode.

Table 5. Using the MODE Pin to Select Light Load Operating Mode

MODE Pin	Light Load Operating Mode	Mode When Synchronized
0 V or Floating	Burst Mode	Forced continuous
100 kΩ to $INTV_{CC}$	Pulse skipping	Pulse skipping
$INTV_{CC}$	Forced continuous	Forced continuous

The requirements of each application dictate the appropriate choice for light load operating mode. In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom FET before the inductor current reaches zero, preventing it from reversing and going negative. Therefore, the regulator operates in discontinuous operation. In addition, when the load current is light, the inductor current begins bursting at frequencies lower than the switching frequency and enters a low current sleep mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light loads.

In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of the load. In this mode, the efficiency at light loads is considerably lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

In pulse skipping mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At very light loads, the PWM comparator can remain tripped for several cycles and force the top FET to remain off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference compared to Burst Mode operation. Pulse skipping mode provides higher light load efficiency than forced continuous mode but not nearly as high as Burst Mode operation. Consequently, pulse skipping mode represents a compromise between light load efficiency, output ripple, and EMI.

In some applications, it can be desirable to change the light load operating mode based on the conditions present in the system. For example, if a system is inactive, the user can select high efficiency Burst Mode operation by keeping the MODE pin set to 0 V. When the system wakes, the user can send an external clock to PLLIN/SPREAD or tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode. These types of mode changes can allow an individual application to benefit from the advantages of each light load operating mode.

DEAD TIME CONTROL (DTCA AND DTCB PINS)

The dead time delays of the LTC7890 can be adjusted from near zero to 60 ns by configuring the DTCA pin and DTCB pin. Refer to Figure 40, Figure 41, and Figure 42, which show the TGx minus SWx, BGx, and SWx waveforms for each DTCx pin setting. In the DTCx Pins Tied to GND (Adaptive Dead Time Control), DTCx Pins Tied to INTVCC (Smart Near Zero Dead Time Control), and DTCx Pins Connected with a Resistor to GND sections, TGx represents the voltage sensed at the top FET gate (the threshold for TGx falling is sensed at the TGUPx pin), and BGx represents the voltage sensed at the bottom FET gate (the thresholds for BGx rising and falling are sensed at the BGDNx and BGUPx pins, respectively). The SWx waveforms represent operation in continuous conduction mode with positive inductor current. The DTCA pin programs the dead time associated with the bottom FET turning off and the top FET turning on (SWx transitioning from low to high). The DTCB pin programs the dead time associated with top FET turning off and the bottom FET turning on (SWx transitioning from high to low).

DTCx Pins Tied to GND (Adaptive Dead Time Control)

Tying the DTCA pin and DTCB pin to GND programs adaptive dead time control. In adaptive control (see Figure 40), the dead time is measured between one FET turning off and the other FET turning on. Tying the DTCA pin to GND fixes the delay between BGx falling and TGx minus SWx rising to approximately 20 ns. Tying the DTCB pin to GND fixes the delay between TGx minus SWx falling and BGx rising to approximately 20 ns.

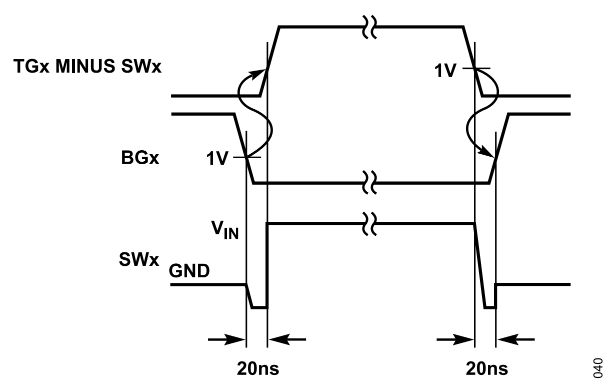

Figure 40. DTCx Pins Tied to GND–Adaptive Dead Time Control

DTCx Pins Tied to $INTV_{CC}$ (Smart Near Zero Dead Time Control)

Figure 41 shows the timing waveforms when the DTCx pins are tied to $INTV_{CC}$. Tying the DTCA pin to $INTV_{CC}$ reduces the delay between BGx falling and SWx rising to near zero. Tying the DTCB pin to $INTV_{CC}$ reduces the delay between SWx falling and BGx

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rising to near zero (with positive inductor current when the top FET turns off). Note the rising edge of BGx (sensed at the BGDN pin) and SWx is defined as the moment its voltage rises to ~1 V (with respect to GND). Likewise, the falling edge of BGx (sensed at the BGUP pin) and SWx is the moment its voltage falls to ~1 V.

For the DTCB transition, if the SWx node does not fall to 1 V approximately 20 ns after the top FET turns off (inductor current is small or negative), the bottom FET turns on automatically. This 20 ns timeout sets the maximum delay between TGx minus SWx falling and BGx rising.

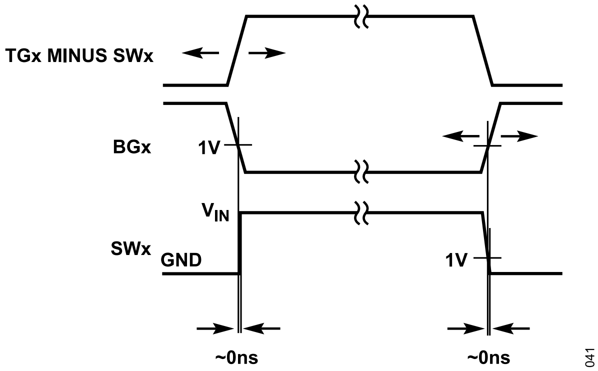

Figure 41. DTCx Pins Tied to $INTV_{CC}$—Smart Near Zero Dead Time Control

DTCx Pins Connected with a Resistor to GND

Connecting a resistor between the DTCx pins and GND programs an additional delay from 7 ns to 60 ns between the SWx and BGx edges (see Figure 42). A resistor tied to the DTCA pin inserts additional delay between BGx falling and SWx rising. A resistor tied to the DTCB pin to GND inserts an additional delay between SWx falling and BGx rising. Figure 43 shows the relationship between the DTCx pin resistor value and the programmed delay between the BGx and SWx edges. This resistor must not be less than 10 kΩ.

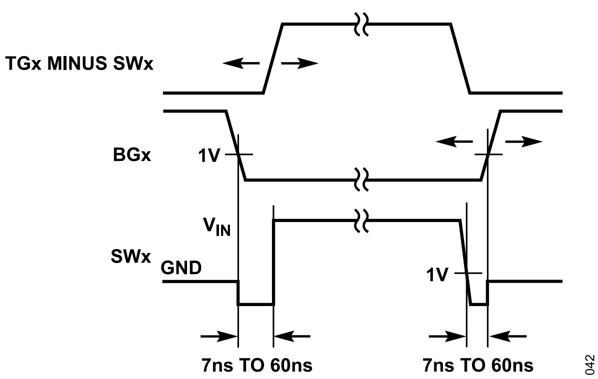

Figure 42. DTCx Pins with Resistor to GND–Adjustable Dead Time Control

With a resistor on the DTCx pins, the maximum delay between one FET turning off and the other FET turning on is set to approximately 30 ns beyond the programmed delay time. For the DTCA transition (SWx from low to high), this timeout can be reached if the bottom FET turns off with negative inductor current (for example, light load currents in forced continuous mode), such that SWx slews high immediately after the bottom FET turns off.

If one of the DTCx pins is programmed with a resistor, the other DTCx pin must be programmed with a resistor or tied to $INTV_{CC}$ for proper dead time control operation. Unexpected dead time delays can result if one DTCx pin is programmed with a resistor or tied to $INTV_{CC}$, while the other DTCx pin is tied to GND.

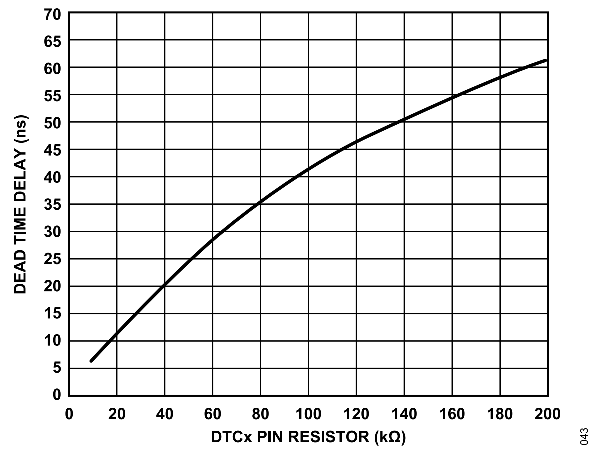

Figure 43. Relationship Between Dead Time Delay and Resistor Value at DTCx Pins

POWER FET SELECTION

Two external power FETs must be selected for the LTC7890: one N-channel FET for the top (main) switch and one N-channel FET for the bottom (synchronous) switch. The peak-to-peak gate drive levels are set by the $INTV_{CC}$ regulation point (4 V to 5.5 V). Most GaN FETs can be driven comfortably within this $INTV_{CC}$ regulation window. If using silicon MOSFETs, logic level threshold MOSFETs must be used in most applications. Pay close attention to the breakdown voltage (BVD_{SS}) specification for the FETs as well.

Selection criteria for the power FETs include the on resistance ($R_{DS(ON)}$), Miller capacitance (C_{MILLER}), input voltage, and maximum output current. C_{MILLER} can be approximated from the gate charge curve typically provided in the data sheet of the FET manufacturer. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat, divided by the specified change in the voltage difference between the drain and source terminals of the FET (V_{DS}). This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom FETs are given by Equation 10 and Equation 11, as follows:

$$Main\ Switch\ Duty\ Cycle = V_{OUT}/V_{IN} \quad (10)$$

$$Synchronous\ Switch\ Duty\ Cycle = (V_{IN} - V_{OUT})/V_{IN} \quad (11)$$

The FET power dissipation at the maximum output current is given by Equation 12 and Equation 13, as follows:

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$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER}) \times \left(\frac{1}{V_{INTCC}-V_{THMIN}}+\frac{1}{V_{THMIN}}\right)(f) \quad (12)$$

$$P_{SYNC} = \frac{V_{IN}-V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} \quad (13)$$

where:

P_{MAIN} is the power dissipation from the main switch.
δ is the temperature dependency of $R_{DS(ON)}$ ($\delta \approx 0.005/°C$).
R_{DR} is the effective driver resistance at the Miller threshold voltage of the FET ($R_{DR} \approx 2\ \Omega$).
V_{INTCC} is the $INTV_{CC}$ voltage.
V_{THMIN} is the typical FET minimum threshold voltage.
P_{SYNC} is the power dissipation from the synchronous switch.

Both FETs have I^2R losses (I^2R is the power loss equation of the FETs when on in steady state), whereas the main N-channel equations include an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20 V, the high current efficiency generally improves with larger FETs. However, for V_{IN}> 20 V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} provides higher efficiency. The synchronous FET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

C_{IN} AND C_{OUT} SELECTION

The selection of the input capacitance (C_{IN}) is usually based on the worst case rms current drawn through the input network (battery, fuse, or capacitor). The highest V_{OUT} × output current (I_{OUT}) product must be used in Equation 14 to determine the maximum rms capacitor current requirement.

Increasing the output current drawn from the other controller actually decreases the input rms ripple current from its maximum value. The out of phase technique typically reduces the rms ripple current of the input capacitor by a factor of 30% to 70% when compared to a single-phase power supply solution.

In continuous mode, the source current of the top FET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, use a low effective series resistance (ESR) capacitor sized for the maximum rms current (I_{RMS}). At I_{MAX}, the maximum rms capacitor current is given by Equation 14, as follows:

$$C_{IN}\ \ Required\ \ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left((V_{OUT})(V_{IN}-V_{OUT})\right)^{1/2} \quad (14)$$

Equation 14 has a maximum at V_{IN} = 2 V_{OUT}, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that the ripple current ratings of capacitor manufacturers are often based on only 2000 hours of life. This basis makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors can be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7890, ceramic capacitors can also be used for C_{IN}. Consult the manufacturer if there is any question.

The benefit of the LTC7890 2-phase operation can be calculated by using this equation for the higher power controller and then calculating the loss that would result if both controller channels switched on at the same time. The total rms power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the ESR of the input capacitor. This result is why the requirement of the input capacitor previously calculated for the worst case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design is only fully realized when the source impedance of the power supply and/or battery is included in the efficiency testing.

Place the drains of the top FETs within 1 cm of each other, and ensure these drains share common C_{IN}. Separating the drains and C_{IN} can produce undesirable resonances at V_{IN}.

Placing a small (0.1 µF to 1 µF) bypass capacitor between the chip V_{IN} pin and GND close to the LTC7890 is also suggested. An optional 1 Ω to 10 Ω resistor placed between C_{IN} and the V_{IN} pin provides further isolation from a noisy input supply.

The selection of the output capacitance (C_{OUT}) is driven by the ESR. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated to Equation 15, as follows:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8(f)C_{OUT}}\right) \quad (15)$$

where:

ΔI_L is the ripple current in the inductor.
f is the operating frequency.

The output ripple is highest at the maximum input voltage because ΔI_L increases with the input voltage.

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SETTING THE OUTPUT VOLTAGE

The LTC7890 output voltages are set by an external feedback resistor divider carefully placed across the output, as shown in Figure 44 and Figure 45. The regulated output voltage is determined by Equation 16, as follows:

$$V_{OUT} = 0.8(1 + (R_B/R_A))\ \text{V} \quad (16)$$

Place the R_A and R_B resistors close to the V_{FBx} pin to minimize PCB trace length and noise on the sensitive V_{FBx} node. Take care to route the V_{FBx} trace away from noise sources, such as the inductor or the SWx trace. To improve frequency response, a feedforward capacitor (C_{FF}) can be used.

Channel 1 of the LTC7890 can be programmed to a fixed 12 V or 5 V output through control of the VPRG1 pin. Figure 45 shows how the V_{FB1} pin is issued to sense the output voltage in fixed output mode. Tying VPRG1 to $INTV_{CC}$ or GND programs V_{OUT1} to 12 V or 5 V, respectively. Floating VPRG1 sets V_{OUT1} to adjustable output mode using external resistors.

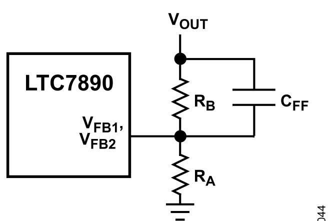

Figure 44. Setting Adjustable Output Voltage

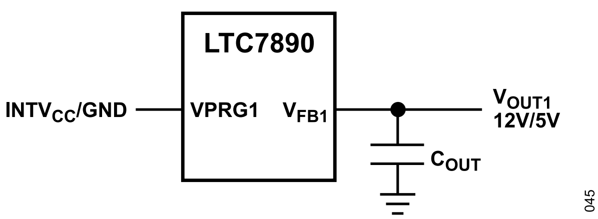

Figure 45. Setting Fixed 12 V or 5 V Voltage

For applications with multiple output voltage levels, select Channel 1 to be the lowest output voltage that is greater than 3.2 V. When the $SENSE1^-$ pin (connected to V_{OUT1}) is above 3.2 V, it biases some internal circuitry instead of V_{IN}, thereby increasing light load Burst Mode efficiency. Similarly, connect $EXTV_{CC}$ to the lowest output voltage that is greater than the $EXTV_{CC}$ rising switchover threshold as determined by the DRVUV pin. $EXTV_{CC}$ then supplies the high current gate drivers and relieves additional I_B from V_{IN}, further reducing the V_{IN} pin current to ≈1 µA in sleep.

RUNX PINS AND UNDERVOLTAGE LOCKOUT

The two channels of the LTC7890 are enabled using the RUN1 and RUN2 pins. The RUNx pin has a rising threshold of 1.2 V with 120 mV of hysteresis. Pulling a RUNx pin less than 1.08 V shuts down the main control loop and resets the soft start for that channel. Pulling both RUN1 and RUN2 less than 0.7 V disables the controller and most internal circuits, including the $INTV_{CC}$ LDO regulators. In this state, the LTC7890 draws only ≈1 µA of I_B.

The RUNx pins are high impedance so these pins must be externally pulled up or pulled down or driven directly by logic. The RUNx pins can tolerate up to 100 V (the absolute maximum). Therefore, these pins can be conveniently tied to V_{IN} in always on applications where the controller is enabled continuously and never shut down. Do not float the RUNx pins.

The RUNx pins can also be configured as precise UVLOs on the input supply with a resistor divider from V_{IN} to GND, as shown in Figure 46.

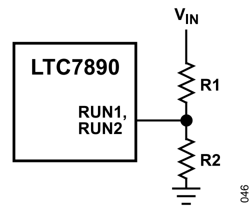

Figure 46. Using the RUN1 and RUN2 Pins as an UVLO

The V_{IN} UVLO thresholds can be computed by Equation 17 and Equation 18, as follows:

$$\text{UVLO Rising} = 1.2(1 + (R1/R2))\ \text{V} \quad (17)$$

$$\text{UVLO Falling} = 1.08(1 + (R1/R2))\ \text{V} \quad (18)$$

The current that flows through the R1 and R2 divider adds to the shutdown, sleep, and active current of the LTC7890. Take care to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the MΩ range can be required to keep the impact on quiescent shutdown and sleep currents low.

SOFT START AND TRACKING (TRACK/SSX PIN)

The startup of each V_{OUTx} is controlled by the voltage on the TRACK/SSx pin (TRACK/SS1 for Channel 1 and TRACK/SS2 for Channel 2). When the voltage on the TRACK/SSx pin is less than the internal 0.8 V reference, the LTC7890 regulates the V_{FBx} pin voltage to the voltage on the TRACK/SSx pin instead of the internal reference. The TRACK/SSx pin can program an external soft start function or allow V_{OUTx} to track another supply during startup.

Soft start is enabled by connecting a capacitor from the TRACK/SSx pin to GND. An internal 12 µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SSx pin. The LTC7890 regulates its feedback voltage (and hence V_{OUTx}) according to the voltage on the TRACK/SSx pin, allowing V_{OUTx} to rise smoothly from 0 V to its final regulated value. For a desired soft start time (t_{SS}), select a soft start capacitor (C_{SS}) = t_{SS} × 15 nF/ms.

Alternatively, the TRACK/SSx pin can track another supply during startup, as shown qualitatively in Figure 47 and Figure 48. To track another supply, connect a resistor divider from the leader supply (V_{LEADER}) to the TRACK/SSx pin of the follower supply (V_{OUTx}),

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as shown in Figure 49. During startup, V_{OUTx} tracks V_{LEADER}, according to the ratio set by the resistor divider in Equation 19:

$$\frac{V_{LEADER}}{V_{OUTx}} = \frac{R_A}{R_{TRACKA}} \times \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B} \quad (19)$$

Set Track A resistance (R_{TRACKA}) = Resistance A (R_A) and Track B resistance (R_{TRACKB}) = Resistance B (R_B) for coincident tracking (V_{OUTx} = V_{LEADER} during startup).

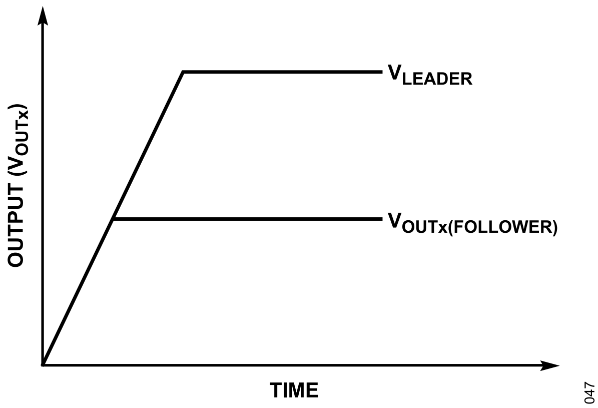

Figure 47. Coincident Tracking

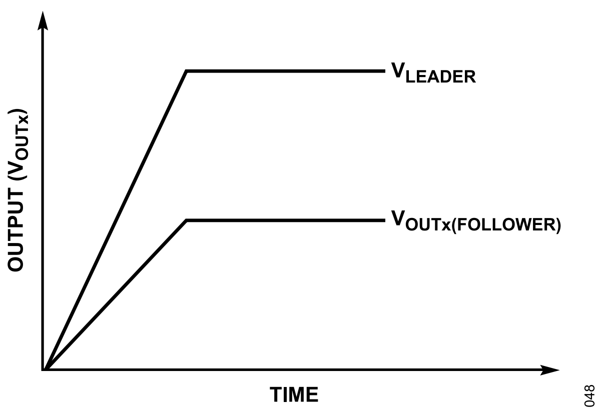

Figure 48. Ratiometric Tracking

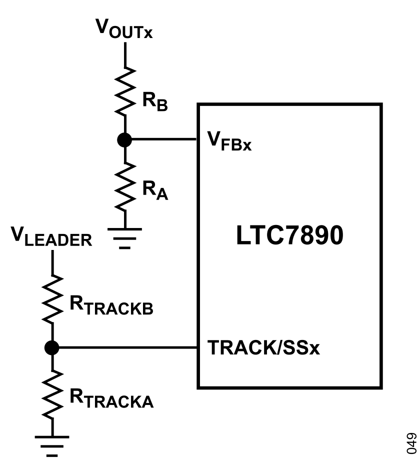

Figure 49. Using the TRACK/SS1 Pin and TRACK/SS2 Pin for Tracking

2-PHASE SINGLE OUTPUT OPERATION

For high power applications, the two channels can be operated in a 2-phase single output configuration. The channels switch 180° out of phase, which reduces the required output capacitance in addition to the required input capacitance and power supply induced noise. To configure the LTC7890 for 2-phase operation, tie V_{FB2} to $INTV_{CC}$, ITH2 to GND, and RUN2 to RUN1.

The RUN1, V_{FB1}, ITH1, and TRACK/SS1 pins are then used to control both channels, but each channel uses its own ICMP and IR comparators to monitor their respective inductor currents. Figure 54 and Figure 56 show typical applications configured for single output 2-phase operation.

$INTV_{CC}$ REGULATORS (OPTI-DRIVE)

The LTC7890 features two separate internal LDO linear regulators that supply power at the $INTV_{CC}$ pin from either the V_{IN} pin or the $EXTV_{CC}$ pin, depending on the $EXTV_{CC}$ pin voltage and connections to the DRVSET and DRVUV pins. The DRV_{CC} pin is the supply pin for the FET gate drivers and must be connected to the $INTV_{CC}$ pin. The V_{IN} LDO regulator and the $EXTV_{CC}$ LDO regulator regulate $INTV_{CC}$ between 4 V and 5.5 V, depending on how the DRVSET pin is set. Each LDO regulator can provide a peak current of at least 100 mA.

Bypass the $INTV_{CC}$ pin to GND with a minimum of 4.7 µF ceramic capacitor and place it as close as possible to the pin. It is recommended to place an additional 1 µF ceramic capacitor next to the DRV_{CC} pin and GND pin to supply the high frequency transient currents required by the FET gate drivers.

The DRVSET pin programs the $INTV_{CC}$ supply voltage, and the DRVUV pin selects the different $INTV_{CC}$ UVLO and $EXTV_{CC}$ switchover threshold voltages. Table 6 summarizes the different DRVSET pin configurations along with the voltage settings that go with each configuration. Table 7 summarizes the different DRVUV pin configurations and voltage settings. Tying the DRVSET pin to $INTV_{CC}$ programs $INTV_{CC}$ to 5.5 V. Tying the DRVSET pin to GND programs $INTV_{CC}$ to 5.0 V. Place a 43 kΩ to 100 kΩ resistor between DRVSET and GND to program the $INTV_{CC}$ voltage between 4 V to 5.5 V, as shown in Figure 50.

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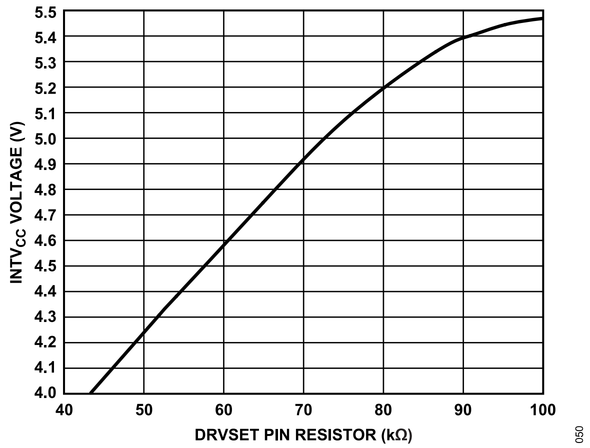

Figure 50. Relationship Between $INTV_{CC}$ Voltage and Resistor Value at the DRVSET Pin

Table 6. DRVSET Pin Configurations and Voltage Settings

DRVSET Pin	$INTV_{CC}$ Voltage (V)
GND	5.0
$INTV_{CC}$	5.5
Resistor to GND, 43 kΩ to 100 kΩ	4 to 5.5

Table 7. DRVUV Pin Configurations and Voltage Settings

DRVUV Pin	$INTV_{CC}$ UVLO Rising and Falling Thresholds (V)	$EXTV_{CC}$ Switchover Rising and Falling Thresholds (V)
GND	3.8 and 3.6	4.76 and 4.54
Floating	4.4 and 4.18	5.95 and 5.56
$INTV_{CC}$	5 and 4.75	5.95 and 5.56

High input voltage applications in which large FETs are driven at high frequencies can exceed the maximum junction temperature rating for the LTC7890. The $INTV_{CC}$ current, which is dominated by the gate charge current, can be supplied by either the V_{IN} LDO regulator or the $EXTV_{CC}$ LDO regulator. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.76 V or 5.95 V, as determined by the DRVUV pin), the V_{IN} LDO regulator is enabled. In this case, power dissipation for the IC is equal to V_{IN} × $INTV_{CC}$ current (I_{INTVCC}). The gate charge current is dependent on the operating frequency, as discussed in the Efficiency Considerations section. To estimate the junction temperature, use the equation detailed in Table 2. For example, the LTC7890 $INTV_{CC}$ current is limited to less than 49 mA from a 48 V supply when not using the $EXTV_{CC}$ supply at an ambient temperature of 70°C, as shown in Equation 20:

$$T_J = 70°C + (49\ mA)(48\ V)(34°C/W) = 150°C \quad (20)$$

To prevent exceeding the maximum junction temperature, check the input supply current while operating in continuous conduction mode (MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above its rising switchover threshold, the V_{IN} LDO regulator turns off and the $EXTV_{CC}$ LDO regulator enables. The $EXTV_{CC}$ LDO regulator remains on as long as the voltage applied to $EXTV_{CC}$ remains above its falling switchover threshold. The $EXTV_{CC}$ LDO regulator attempts to regulate the $INTV_{CC}$ voltage to the voltage as programmed by the DRVSET pin. Therefore, while $EXTV_{CC}$ is less than the programmed voltage set by the DRVSET pin, the LDO regulator is in dropout, and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage (up to an absolute maximum of 30 V), $INTV_{CC}$ is regulated to the programmed voltage. Using the $EXTV_{CC}$ LDO regulator allows the FET driver and control power to be derived from the switching regulator output of the LTC7890 (4.7 V ≤ V_{OUT} ≤ 30 V) during normal operation and from the V_{IN} LDO regulator when the output is out of regulation (for example, startup or short-circuit). If more current is required through the $EXTV_{CC}$ LDO regulator than is specified, add an external Schottky diode between the $EXTV_{CC}$ and $INTV_{CC}$ pins. In this case, do not apply more than 6 V to the $EXTV_{CC}$ pin.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from a LTC7890 switching regulator output because the V_{IN} current resulting from the driver and control currents is scaled by a factor of $V_{OUTx}/(V_{IN}$ × efficiency). For 5 V to 30 V switching regulator outputs, connect the $EXTV_{CC}$ pin to V_{OUTx}. Tying the $EXTV_{CC}$ pin to an 8.5 V supply reduces the junction temperature in Equation 20 from 150°C to the results given by Equation 21, as follows:

$$T_J = 70°C + (49\ mA)(8.5\ V)(34°C/W) = 84°C \quad (21)$$

However, for 3.3 V and other low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This connection causes the internal V_{IN} LDO regulator to power $INTV_{CC}$, resulting in an efficiency penalty of up to 10% or more at high input voltages.
2. $EXTV_{CC}$ connected directly to a LTC7890 switching regulator output. This connection is the normal connection for an application with an output range of 5 V to 30 V and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available, it can be used to power $EXTV_{CC}$, provided that it is compatible with the FET gate drive requirements. This supply can be higher or lower than V_{IN}. However, a lower $EXTV_{CC}$ voltage results in higher efficiency.
4. $EXTV_{CC}$ connected to an output derived boost or charge pump. For LTC7890 switching regulators where outputs are less than 5 V, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output derived voltage that is boosted to greater than the $EXTV_{CC}$ switchover threshold.

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TOPSIDE FET DRIVER SUPPLY (C_B)

External bootstrap capacitors (C_B) connected to the BOOSTx pins supply the gate drive voltage for the topside FETs. C_B in Figure 35 is charged through an internal switch from DRV_{CC} when the SWx pin is low and the bottom FET is tuned on. The on resistance of the internal switch is approximately 7 Ω.

When the topside FET turns on, the driver places the C_B voltage across the gate source of the desired FET, which enhances the FET and turns on the topside switch. The switch node voltage, SWx, rises to V_{IN} and the BOOSTx pin follows. With the topside FET on, the boost voltage is more than the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of C_B needs to be 100 times that of the total input capacitance of the topside FETs. For a typical application, a value of C_B = 0.1 µF is sufficient.

MINIMUM ON-TIME CONSIDERATIONS

The minimum on time ($t_{ON(MIN)}$) is the smallest time duration that the LTC7890 is capable of turning on the top FET. $t_{ON(MIN)}$ is determined by the internal timing delays and the gate charge required to turn on the FET. Low duty-cycle applications can approach this minimum on-time limit. Take care to ensure the results in Equation 22, as follows:

$$t_{ON(MIN)} < (V_{OUT}/(V_{IN} \times f)) \tag{22}$$

If the duty cycle falls to less than what can be accommodated by the minimum on time, the controller begins to skip cycles. The output voltage continues to regulate, but the ripple voltage and current increase. The minimum on time for the LTC7890 is approximately 40 ns. However, as the peak sense voltage decreases, the minimum on time gradually increases up to about 60 ns. This change is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops to less than the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

FAULT CONDITIONS: CURRENT LIMIT AND FOLDBACK

The LTC7890 includes current foldback to reduce the load current when the output is shorted to GND. If the output voltage falls below 70% of its regulation point, the maximum sense voltage is progressively lowered from 100% to 40% of its maximum value. Under short-circuit conditions with low duty cycles, the LTC7890 begins cycle skipping to limit the short-circuit current. In this situation, the bottom FET dissipates most of the power, but less than in normal operation. The short-circuit ripple current ($\Delta I_{L(SC)}$) is determined by the $t_{ON(MIN)} \approx 40$ ns, the input voltage, and the inductor (L) value given by Equation 23, as follows:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \times V_{IN}/L \tag{23}$$

The resulting average short-circuit current (I_{SC}) is given by Equation 24, as follows:

$$I_{SC} = 40\,\% \times I_{LIM(MAX)} - \Delta I_{L(SC)}/2 \tag{24}$$

where $I_{LIM(MAX)}$ is the maximum peak inductor current.

FAULT CONDITIONS: OVERVOLTAGE PROTECTION

If an output voltage rises 10% more than its set regulation point, the top FET turns off and remains off until the overvoltage condition clears. During the overvoltage condition, the inductor current is also not allowed to reverse, except during the boost refresh pulses described in the High-Side Bootstrap Capacitor section.

FAULT CONDITIONS: OVERTEMPERATURE PROTECTION

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating (such as a short from $INTV_{CC}$ to GND), internal overtemperature shutdown circuitry shuts down the LTC7890. When the internal die temperature exceeds 180°C, the $INTV_{CC}$ LDO regulator and gate drivers disable. When the die cools to 160°C, the LTC7890 enables the $INTV_{CC}$ LDO regulator and resumes operation, beginning with a soft start startup. Avoid long-term overstress (T_J > 125°C) because it can degrade the performance or shorten the life of the device.

PHASE-LOCKED LOOP AND FREQUENCY SYNCHRONIZATION

The LTC7890 has an internal PLL that allows the turn on of the top FET to be synchronized to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin.

Rapid phase locking can be achieved by using the FREQ pin to set a free running frequency near the desired synchronization frequency. Before synchronization, the PLL is prebiased to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase lock and synchronization. Although it is not required, placing the free running frequency near the external clock frequency prevents the oscillator from passing through a large range of frequencies as the PLL locks.

When synchronized to an external clock, the LTC7890 operates in pulse skipping mode if it is selected by the MODE pin, or in forced continuous mode otherwise. The LTC7890 is guaranteed to synchronize to an external clock applied to the PLLIN/SPREAD pin that swings up to at least 2.2 V and down to 0.5 V or less. Note that the LTC7890 can only be synchronized to an external clock frequency within the range of 100 kHz to 3 MHz.

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EFFICIENCY CONSIDERATIONS

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Analyzing individual losses is useful for determining what is limiting the efficiency and which change produces the most improvement. The percent efficiency can be expressed by Equation 25, as follows:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + \ldots) \quad (25)$$

where *L1*, *L2*, *L3*, and so on, are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7890 circuits: IC V_{IN} current, $INTV_{CC}$ regulator current, I^2R losses, and topside FET transition losses.

The V_{IN} current is the dc supply current given in Table 1, which excludes FET driver and control currents. Other than at light loads in Burst Mode operation, V_{IN} current typically results in a small (<0.1%) loss.

The $INTV_{CC}$ current is the sum of the FET driver and control currents. The FET driver current results from switching the gate capacitance of the power FETs. Each time a FET gate is switched from low to high to low again, a packet of charge (dQ) moves from $INTV_{CC}$ to GND. The resulting dQ/time duration (dt) is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, gate charge current ($I_{GATECHG}$) = Frequency (f) x ($Q_T + Q_B$), where Q_T and Q_B are the gate charges of the top and bottom FETs.

Supplying $INTV_{CC}$ from an output derived source through $EXTV_{CC}$ scales the V_{IN} current required for the driver and control circuits by a factor of $V_{OUTx}/(V_{IN} \times \text{efficiency})$. For example, in a 20 V to 5 V application, 10 mA of $INTV_{CC}$ current results in approximately 2.5 mA of V_{IN} current. This result reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

I^2R losses are predicted from the dc resistances of the input fuse (if used), FET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode, the average output current flows through L and R_{SENSE} but is chopped between the top and bottom FETs. If the two FETs have approximately the same $R_{DS(ON)}$, the resistance of one FET can be summed with the resistances of L, R_{SENSE}, and ESR to obtain the I^2R losses.

For example, if each $R_{DS(ON)}$ = 30 mΩ, load resistance (R_L) = 50 mΩ, R_{SENSE} = 10 mΩ, and ESR = 40 mΩ (the sum of both input and output capacitance losses), the total resistance is 130 mΩ. The resulting losses range from 3% to 13% as the output current increases from 1 A to 5 A for a 5 V output or a 4% to 20% loss for a 3.3 V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system.

Transition losses apply only to the top FETs and become significant only when operating at higher input voltages (typically 15 V or greater). Transition losses can be estimated using Equation 26, as follows:

$$Transition\ Loss = 1.7(V_{IN})^2 \times I_{L(MAX)} \times C_{RSS} \times f \quad (26)$$

where C_{RSS} is the reverse transfer capacitance.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional 5% to 10% efficiency degradation in portable systems. It is important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and low ESR at the switching frequency. A 25 W supply typically requires a minimum of 20 µF to 40 µF of capacitance with a maximum of 20 mΩ to 50 mΩ of ESR. Other losses, including inductor core losses, generally account for less than 2% total additional loss.

CHECKING TRANSIENT RESPONSE

To check the regulator loop response, look at the load current transient response. Switching regulators take several cycles to respond to a step in dc (resistive) load current. When a load step occurs, V_{OUTx} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUTx} to its steady state value. During this recovery time, V_{OUTx} can be monitored for excessive overshoot or ringing, which indicates a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITHx pin not only allows optimization of control loop behavior, but it also provides a dc-coupled and ac filtered closed-loop response test point. The dc step, rise time, and settling at this test point reflects the closed-loop response. Assuming a predominantly second-order system, the phase margin and/or damping factor can be estimated using the percentage of overshoot seen at the ITHx pin. The bandwidth can also be estimated by examining the rise time at the ITHx pin. The ITHx external components shown in Figure 52, Figure 54, Figure 56, and Figure 58 provide an adequate starting point for most applications.

The ITHx series compensation resistor (R_C) and capacitor (C_C) filter sets the dominant pole zero loop compensation. The values can be modified slightly (from 0.5 times to 2 times their initial values) to optimize transient response when the final PCB layout is done and the particular output capacitor type and value are determined. The output capacitors must be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of the full load current, with a rise time of 1 µs to 10 µs, produces output voltage and ITHx pin waveforms that give

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a sense of the overall loop stability without breaking the feedback loop.

Placing a power FET directly across from the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop. Therefore, this signal cannot be used to determine phase margin. For this reason, it is better to look at the ITHx pin signal, which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop increases by increasing R_C, and the bandwidth of the loop increases by decreasing C_C. If R_C increases by the same factor that C_C decreases, the zero frequency is kept the same, keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1 µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUTx}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage, if the load switch resistance is low and it is driven quickly. If the ratio of load capacitance (C_{LOAD}) to C_{OUT} is greater than 1:50, the switch rise time must be controlled so that the load rise time is limited to approximately C_{LOAD} × 25 µs/µF. Therefore, a 10 µF capacitor requires a 250 µs rise time, limiting the charging current to about 200 mA.

DESIGN EXAMPLE

As a design example, assume the nominal input voltage ($V_{IN(NOMINAL)}$) = 12 V, $V_{IN(MAX)}$ = 22 V, V_{OUTx} = 3.3 V, I_{OUT} = 20 A, and f = 1 MHz.

Take the following steps to design an application circuit:

1. Set the operating frequency. The frequency is not one of the internal preset values. Therefore, a resistor from the FREQ pin to GND is required, with a value given by Equation 27, as follows:

$$R_{FREQ}\left(\text{in k}\Omega\right) = (37\text{ MHz}/1\text{ MHz}) = 37\text{ k}\Omega \quad (27)$$

2. Determine the inductor value. Initially, select a value based on an inductor ripple current of 30%. To calculate the inductor value, use Equation 28, as follows:

$$L = \frac{V_{OUT}}{f(\Delta I_L)}\left(1 - \frac{V_{OUT}}{V_{IN(NOMINAL)}}\right) = 0.4\ \mu\text{H} \quad (28)$$

The highest value of the ripple current occurs at the maximum input voltage. In this case, the ripple at V_{IN} = 22 V is 35%.

3. Verify that the minimum on time of 40 ns is not violated. The minimum on time occurs at $V_{IN(MAX)}$, as shown in Equation 29:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \times f} = 150\text{ ns} \quad (29)$$

This time is sufficient to satisfy the minimum on-time requirement. If the minimum on time is violated, the LTC7890 skips pulses at high input voltage, resulting in lower frequency operation and higher inductor current ripple than desired. If undesirable, this behavior can be avoided by decreasing the frequency (with the inductor value accordingly adjusted) to avoid operation near the minimum on time.

4. Select the R_{SENSE} resistor value. The peak inductor current is the maximum dc output current plus half of the inductor ripple current, or 20 A × (1 + 0.30/2) = 23 A in this case. The R_{SENSE} resistor value is then calculated based on the minimum value for the maximum current sense threshold (45 mV for ILIM = float), given by Equation 30, as follows:

$$R_{SENSE} \leq (45\text{ mV}/23\text{ A}) \cong 2\text{ m}\Omega \quad (30)$$

To allow for additional margin, a lower value R_{SENSE} can be used (for example, 1.8 mΩ). However, be sure that the inductor saturation current has sufficient margin more than $V_{SENSE(MAX)}$/R_{SENSE}, where the maximum value of 55 mV is used for $V_{SENSE(MAX)}$.

5. Select the feedback resistors. If light load efficiency is required, use high value feedback resistors to minimize the current due to the feedback divider. However, in most applications, a feedback divider current in the range of 10 µA to 100 µA or more is acceptable. For a 50 µA feedback divider current, R_A = 0.8 V/50 µA = 16 kΩ. R_B is then calculated as $R_B = R_A$(3.3 V/0.8 V – 1) = 50 kΩ.

6. Select the FETs. The best way to evaluate FET performance in a particular application is to build and test the circuit on the bench, facilitated by an LTC7890 evaluation board. However, an educated guess about the application is helpful to initially select FETs. Because this is a high current, low voltage application, I^2R losses likely dominate over transition losses for the top FET. Therefore, choose a FET with lower $R_{DS(ON)}$ as opposed to lower gate charge to minimize the combined loss terms. The bottom FET does not experience transition losses, and its power loss is generally dominated by I^2R losses. For this reason, the bottom FET is typically chosen to be of lower $R_{DS(ON)}$ and higher gate charge than the top FET.

   Due to the high current in this application, two FETs may be needed in parallel to more evenly balance the dissipated power and to lower the $R_{DS(ON)}$. When using silicon MOSFETs, be sure to select logic level threshold MOSFETs because the gate drive voltage is limited to 5.5 V ($INTV_{CC}$).

7. Select the input and output capacitors. C_{IN} is chosen for an rms current rating of at least 10 A (I_{OUT}/2, with margin) at temperature. C_{OUT} is chosen with an ESR of 3 mΩ for low output ripple. Multiple capacitors connected in parallel may be required to reduce the ESR to this level. The output ripple in continuous mode is highest at the maximum input voltage. The

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output voltage ripple ($V_{ORIPPLE}$) due to ESR is approximately given by Equation 31, as follows:

$$V_{ORIPPLE} = ESR \times \Delta I_L = 3\ m\Omega \times 6\ A = 18\ mV\ p\text{-}p \qquad (31)$$

On the 3.3 V output, 18 mV p-p is equal to 0.55% of the peak-to-peak voltage ripple.

8. Determine the bias supply components. Because the regulated output is not greater than the $EXTV_{CC}$ switchover threshold, it cannot be used to bias $INTV_{CC}$. However, if another 5 V supply is available, connect that supply to $EXTV_{CC}$ to improve the efficiency. For a 6.7 ms soft start, select a 0.1 µF capacitor for the TRACK/SSx pin. As a first pass estimate for the bias components, select the $INTV_{CC}$ capacitance (C_{INTVCC}) = 4.7 µF and C_B = 0.1 µF.
9. Determine and set application specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread spectrum, or phase-locked frequency is desired. The RUNx pin can control the minimum input voltage for regulator operation, or the RUNx pin can be tied to V_{IN} for always on operation. Use ITHx compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary.

PCB LAYOUT CHECKLIST

Figure 51 shows the current waveforms present in the various branches of the synchronous regulators operating in the continuous mode.

When laying out the PCB, use the following checklist to ensure proper operation of the IC.

1. Place the top N-channel FETs MTOP1 and MTOP2 (shown in the Typical Applications section) within 1 cm of each other with a common drain connection at C_{IN}. Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.
2. Route the BGUPx and BGDNx traces together and connect them as close as possible to the bottom FET gate. If using gate resistors, connect the resistor connections to the FET gate as close as possible to the FET. Connecting BGUPx and BGDNx further away from the bottom FET gate can cause inaccuracies in the dead time control circuit of the LTC7890. Route the TGUPx and TGDNx traces together and connect them as close as possible to the top FET gate.
3. The combined IC GND pin and the GND return of C_{INTVCC} must return to the combined C_{OUT} negative terminals. The path formed by the top N-channel FET and the C_{IN} capacitor must have short leads and PCB trace lengths. Connect the output capacitor negative terminals as close as possible to the negative terminals of the input capacitor by placing the capacitors next to each other and away from the loop.
4. Connect the LTC7890 V_{FBx} pin resistive dividers to the positive terminals of C_{OUT} and the signal GND. Place the divider close to the V_{FBx} pin to minimize noise coupling into the sensitive V_{FBx} node. The feedback resistor connections must not be along the high current input feeds from the input capacitors.
5. Route the $SENSEx^-$ and $SENSEx^+$ leads together with minimum PCB trace spacing. Route these traces away from the high frequency switching nodes on an inner layer, if possible. The filter capacitor between $SENSEx^+$ and $SENSEx^-$ must be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
6. Connect the $INTV_{CC}$ decoupling capacitor close to the IC, between the $INTV_{CC}$ and the power GND pin. This capacitor carries the current peaks of the FET drivers. Place an additional 1 µF ceramic capacitor next to the DRV_{CC} and GND pins to help improve noise performance.
7. Keep the switching nodes (SW1 and SW2), top gate nodes (TGUP1/TGDN1 and TGUP2/TGDN2), and boost nodes (BOOST1 and BOOST2) away from sensitive small signal nodes, especially from the voltage and current sensing feedback pins of the other channel. All of these nodes have large and fast moving signals. Therefore, keep these nodes on the output side of the LTC7890 and ensure they occupy the minimum PCB trace area.
8. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PCB as the input and output capacitors, with tie ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider, and the GND pin of the IC.

APPLICATIONS INFORMATION

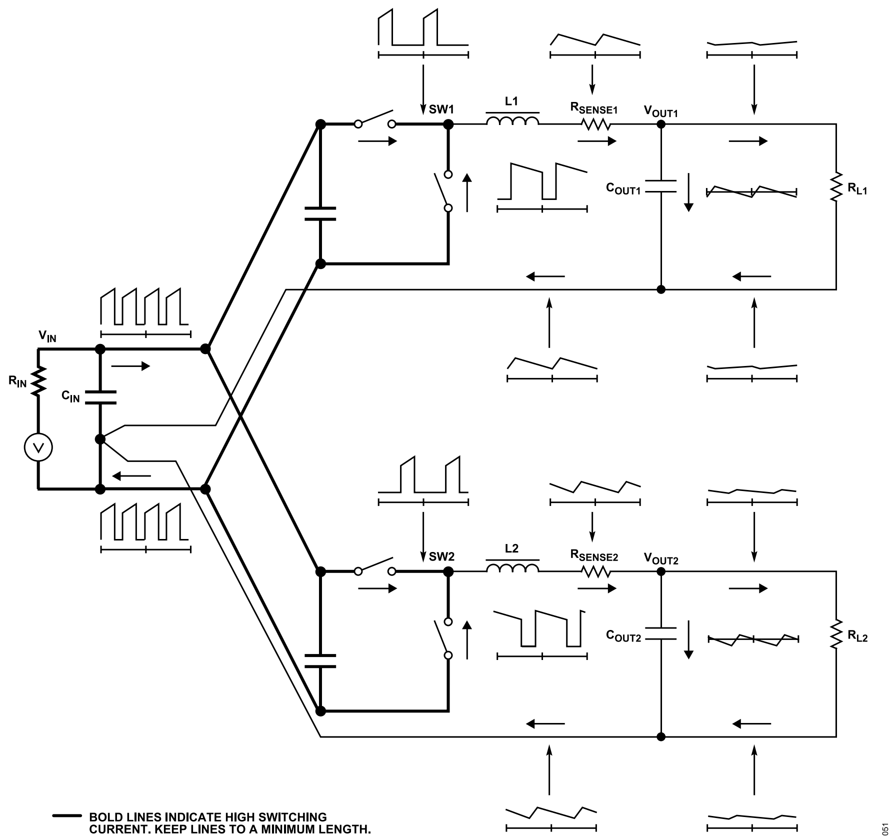

Figure 51. Branch Current Waveform

APPLICATIONS INFORMATION

PCB LAYOUT DEBUGGING

Start with one controller on at a time. Use a dc to 50 MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (the SWx pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation is maintained over the input voltage range down to dropout and until the output load drops to less than the low current operation threshold, typically 25% of the maximum designed current level in Burst Mode operation.

The duty-cycle percentage is maintained from cycle to cycle in a well designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can tame an improper PCB layout if regulator bandwidth optimization is not required. Turn on both controllers at the same time after each controller is checked for its individual performance. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top FET, which occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty-cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the UVLO circuit by further lowering V_{IN} while monitoring the outputs to verify operation. Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOSTx, SWx, TGxxx, and possibly BGxxx connections and the sensitive voltage and current pins. Place the capacitor across the current sensing pins next to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, the top FET, and the bottom FET components to the sensitive current and voltage sensing traces. In addition, investigate the common GND path voltage pickup between these components and the GND pin of the IC.

A problem that may be missed in an otherwise properly working switching regulator results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup is maintained, but the advantages of current mode control are not realized. Compensation of the voltage loop is more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor. The regulator maintains control of the output voltage even during this condition.

APPLICATIONS INFORMATION

TYPICAL APPLICATIONS

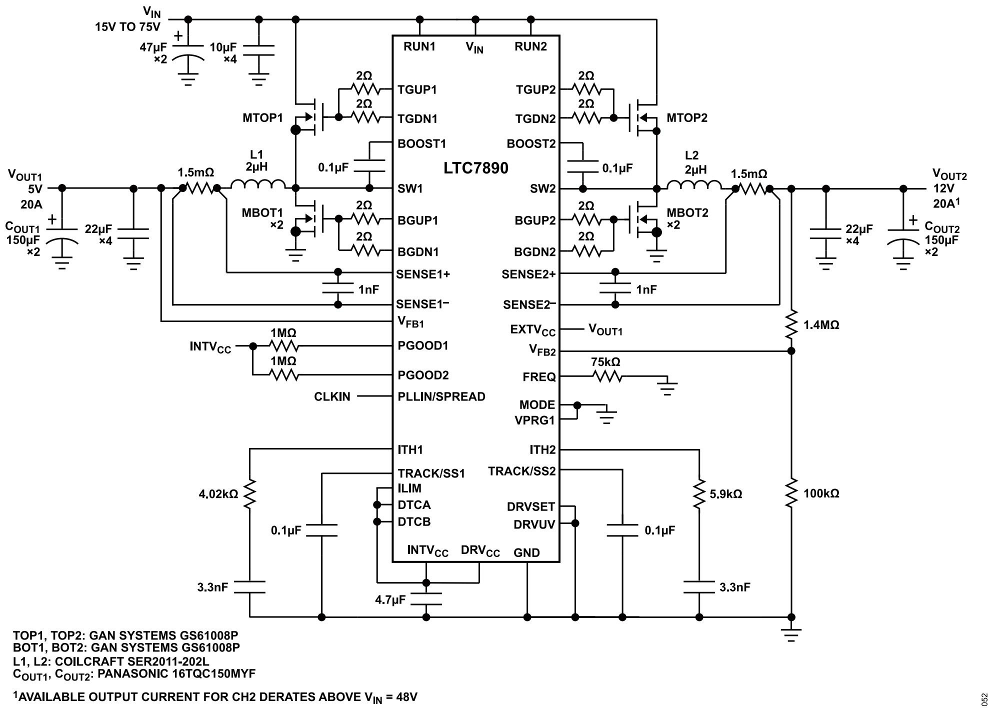

Figure 52. High Efficiency, Dual 5 V/12 V, Step-Down Regulator Using GaN FETs

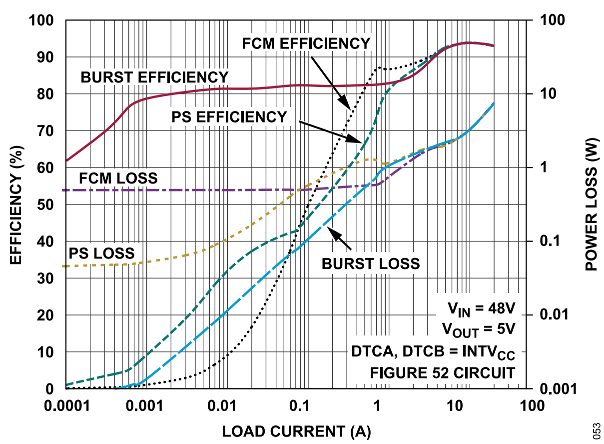

Figure 53. V_{OUT1} Efficiency and Power Loss vs. Load Current for Figure 52

APPLICATIONS INFORMATION

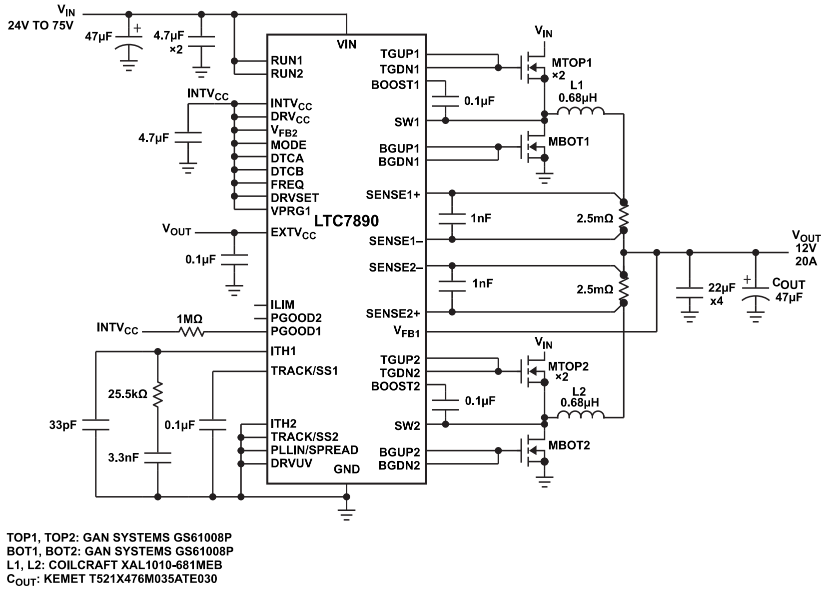

Figure 54. 2-Phase Single Output 12 V_{OUT}, 20 A, 2.25 MHz, Step-Down Regulator Using GaN FETs

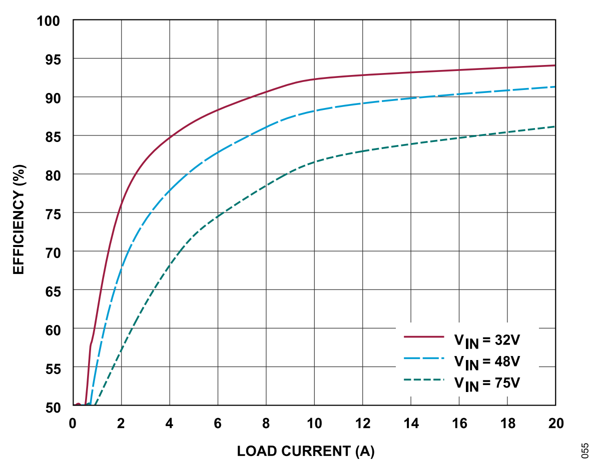

Figure 55. V_{OUT} Efficiency vs. Load Current for Figure 54

APPLICATIONS INFORMATION

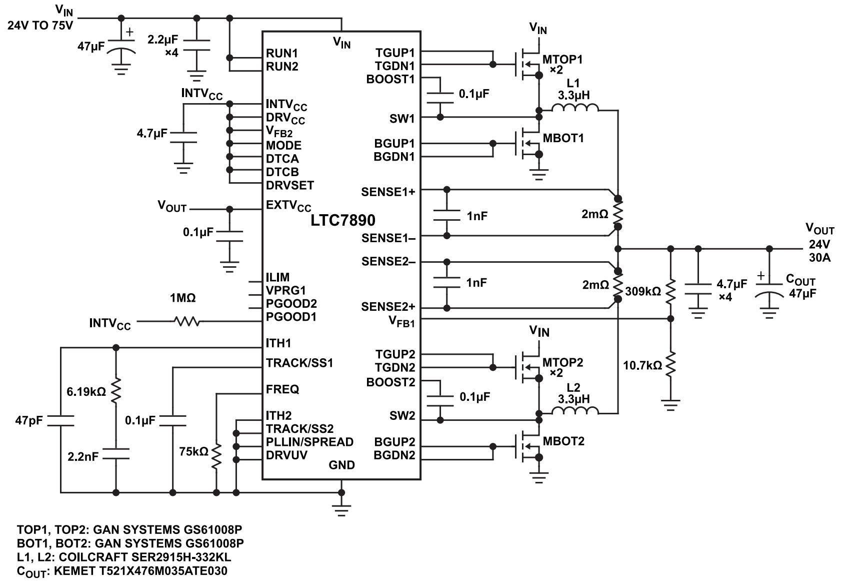

Figure 56. 2-Phase Single Output, 24 V_{OUT}, 500 kHz, Step-Down Regulator Using GaN FETs

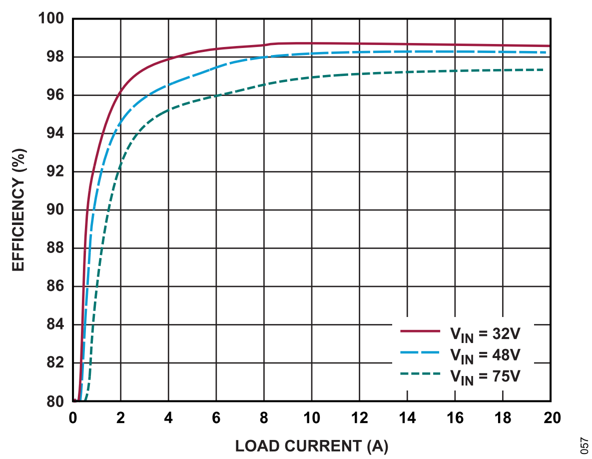

Figure 57. V_{OUT} Efficiency vs. Load Current for Figure 56

APPLICATIONS INFORMATION

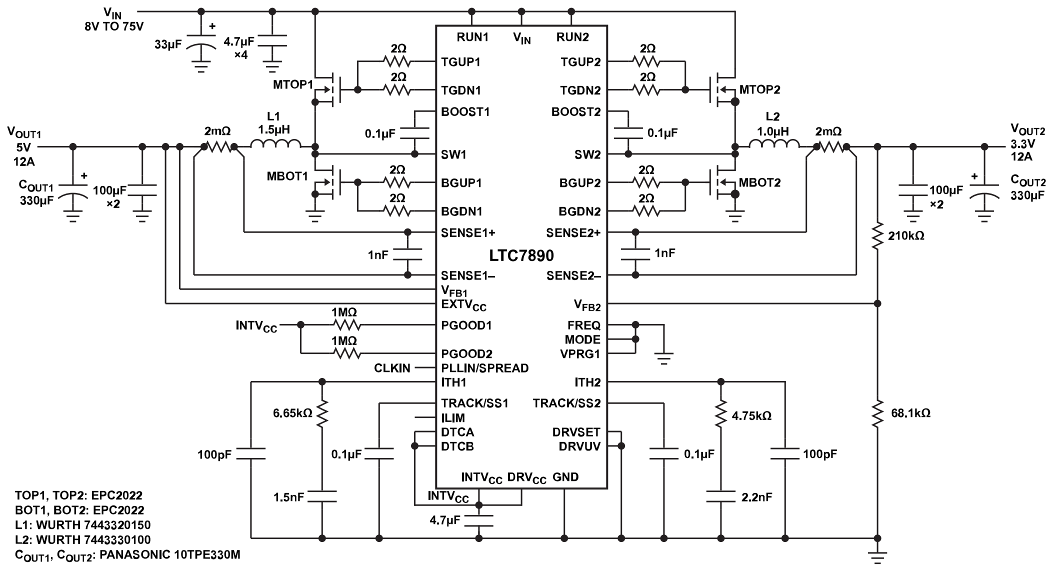

Figure 58. High Efficiency, Dual 5 V/3.3 V, Step-Down Regulator Using GaN FETs

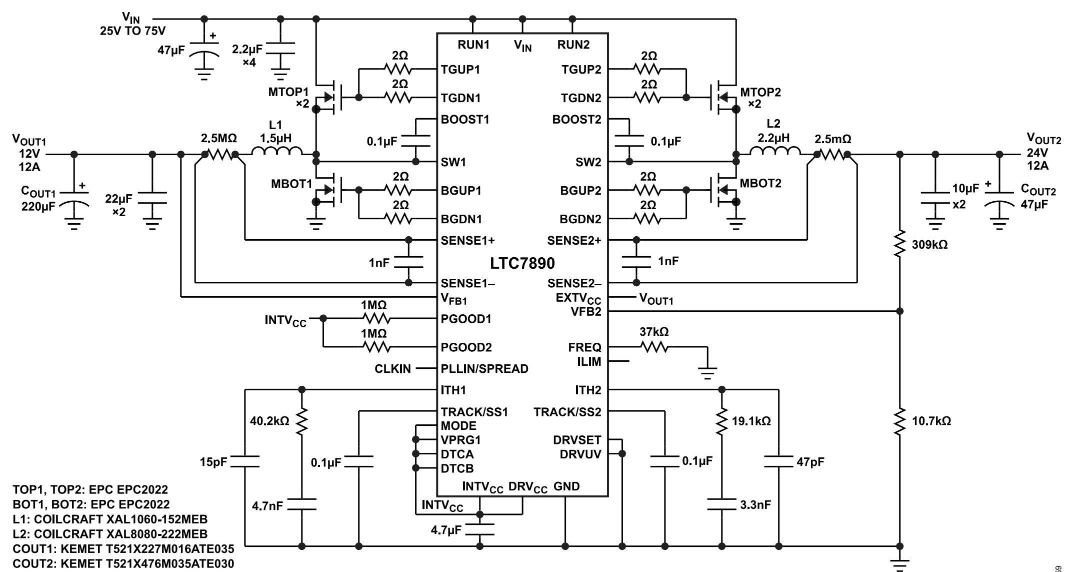

Figure 59. High Efficiency, Dual 12 V/24 V, Step-Down Regulator Using GaN FETs

APPLICATIONS INFORMATION

RELATED PRODUCTS

Table 8. Related Products

Model	Description	Comments
LTC3890	60 V, low I_Q, dual 2-phase step-down controller	PLL fixed frequency of 50 kHz to 900 kHz, 4 V ≤ V_{IN} ≤ 60 V, I_Q = 50 µA, 0.8 V ≤ V_{OUT} ≤ 24 V, 5 mm × 5 mm, 32-lead QFN package
LTC3892	60 V, low I_Q, dual 2-phase step-down controller	PLL fixed frequency of 50 kHz to 900 kHz, 4 V ≤ V_{IN} ≤ 60 V, I_Q = 29 µA, 0.8 V ≤ V_{OUT} ≤ 99% × V_{IN}, 5 mm × 5 mm, 32-lead QFN package
LTC7891	100 V, low I_Q, synchronous step-down controller for GaN FETs	PLL fixed frequency of 100 kHz to 3 MHz, 4 V ≤ V_{IN} ≤ 100 V, I_Q = 5 µA, 0.8 V ≤ V_{OUT} ≤ 60 V, 4 mm × 5 mm, 28-lead QFN package
LTC7800	60 V, low I_Q, high frequency, synchronous step-down controller	4 V ≤ V_{IN} ≤ 60 V, 0.8 V ≤ V_{OUT} ≤ 24 V, I_Q = 50 µA, PLL fixed frequency of 320 kHz to 2.25 MHz, 3 mm × 4 mm, 20-lead QFN package
LTC7802	40 V, dual, low I_Q, 3 MHz, 2-phase, synchronous step-down controller with spread spectrum	4.5 V ≤ V_{IN} ≤ 40 V, V_{OUT} up to 40 V, I_Q = 12 µA, PLL fixed frequency of 100 kHz to 3 MHz, 4 mm × 5 mm, 28-lead QFN package
LTC7803	40 V, low I_Q, 3 MHz, synchronous step-down controller with spread spectrum	PLL fixed frequency of 100 kHz to 3 MHz, 4.5 V ≤ V_{IN} ≤ 40 V, I_Q = 12 µA, 0.8 V ≤ V_{OUT} ≤ 40 V, 3 mm × 3 mm, 16-lead QFN package, 16-lead mini small outline package (MSOP)
LTC7801	150 V, low I_Q, synchronous step-down dc-to-dc controller	4.5 V ≤ V_{IN} ≤ 140 V, 150 V_{PK}, 0.8 V ≤ V_{OUT} ≤ 60 V, I_Q = 40 µA, PLL fixed frequency of 50 kHz to 900 kHz, 4 mm × 5 mm, 24-lead QFN package, 24-lead TSSOP
LTC3895	150 V, low I_Q, synchronous step-down dc-to-dc controller	4.5 V ≤ V_{IN} ≤ 140 V, 150 V_{PK}, 0.8 V ≤ V_{OUT} ≤ 60 V, I_Q = 40 µA, PLL fixed frequency of 50 kHz to 900 kHz, 4 mm × 5 mm, 38-lead TSSOP with high voltage spacing
LTC7818	40 V, low I_Q, 3 MHz, triple output buck/buck/boost synchronous controller	4.5 V ≤ V_{IN} ≤ 40 V, V_{OUT} up to 40 V, I_Q = 14 µA, PLL fixed frequency of 100 kHz to 3 MHz, 6 mm × 6 mm, 40-lead QFN package

OUTLINE DIMENSIONS

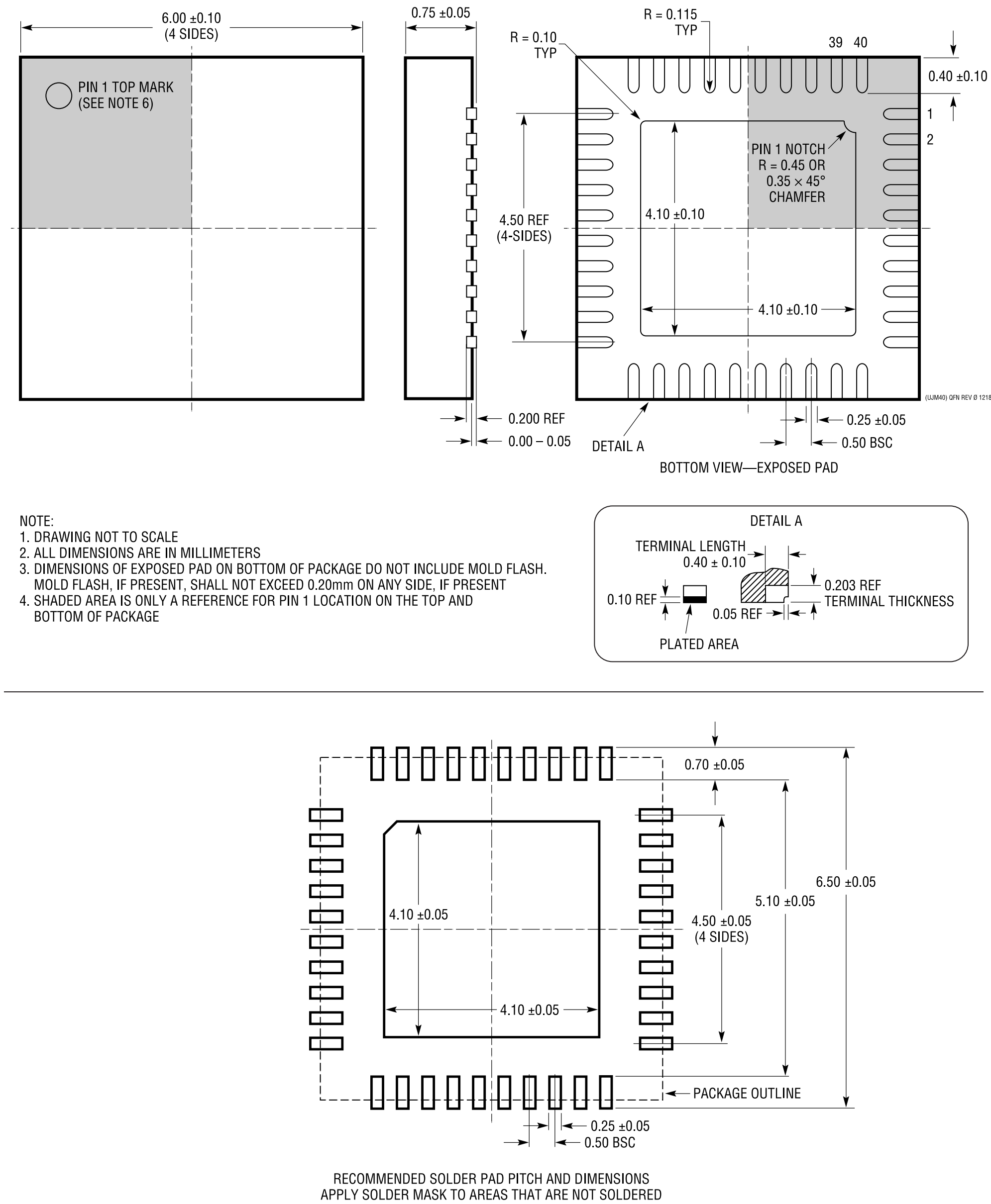

Figure 60. 40-Lead Plastic Side Wettable QFN
6 mm × 6 mm
(05-08-1681)
Dimensions shown in millimeters

Updated: March 16, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC7890RUJM#PBF	–40°C to +150°C	40-Lead QFN (6 mm × 6 mm, Plastic Side Wettable)	Tube, 73	05-08-1681
LTC7890RUJM#TRPBF	–40°C to +150°C	40-Lead QFN (6 mm × 6 mm, Plastic Side Wettable)	Reel, 2500	05-08-1681

1 All models are RoHS compliant parts.

OUTLINE DIMENSIONS

EVALUATION BOARDS

Model[1]	Description
DC2938A	Evaluation Board

1 The DC2938A is an RoHS compliant part.