ASTEC SEMICONDUCTOR

AS384x

Current Mode Controller

PTC

Features

- 2.5 V bandgap reference trimmed to 1.0% and temperature-compensated
- Standard temperature range extended to 105°C
- AS3842/3 oscillations trimmed for precision duty cycle clamp
- AS3844/5 have exact 50% max duty cycle clamp
- Advanced oscillator design simplifies synchronization
- Improved specs on UVLO and hysteresis provide more predictable start-up and shutdown
- Improved 5 V regulator provides better AC noise immunity
- Guaranteed performance with current sense pulled below ground

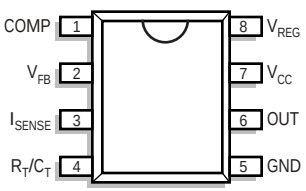
Description

The AS3842 family of control ICs provide pin-for-pin replacement of the industry standard UC3842 series of devices. The devices are redesigned to provide significantly improved tolerances in power supply manufacturing. The 2.5 V reference has been trimmed to 1.0% tolerance. The oscillator discharge current is trimmed to provide guaranteed duty cycle clamping rather than specified discharge current. The circuit is more completely specified to guarantee all parameters impacting power supply manufacturing tolerances.

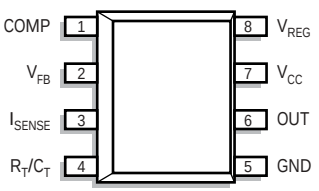
In addition, the oscillator and flip-flop sections have been enhanced to provide additional performance. The R_T/C_T pin now doubles as a synchronization input that can be easily driven from open collector/open drain logic outputs. This sync input is a high impedance input and can easily be used for externally clocked systems. The new flip-flop topology allows the duty cycle on the AS3844/5 to be guaranteed between 49 and 50%. The AS3843/5 requires less than 0.5 mA of start-up current over the full temperature range.

Pin Configuration — Top view

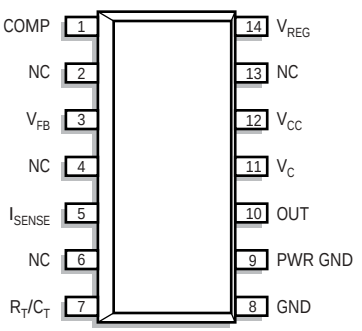
PDIP (N)



8L SOIC (8D)



14L SOIC (14D)



Ordering Information

AS384X 8D N

Circuit Type:
Current Mode Controller (See Table A)

Package Style
8D = 8 Pin Plastic SOIC
14D = 14 Pin Plastic SOIC
N = 8 Pin Plastic DIP

Packaging Option:
N = Tape and Reel (13" Reel Dia)
T = Tube

Table A

Model	$V_{CC(min)}$	$V_{CC(on)}$	Duty Cycle Typ.	I_{CC}
AS3842	10	16	97%	0.5 mA
AS3843	7.6	8.4	97%	0.3 mA
AS3844	10	16	49.5%	0.5 mA
AS3845	7.6	8.4	49.5%	0.3 mA

Functional Block Diagram

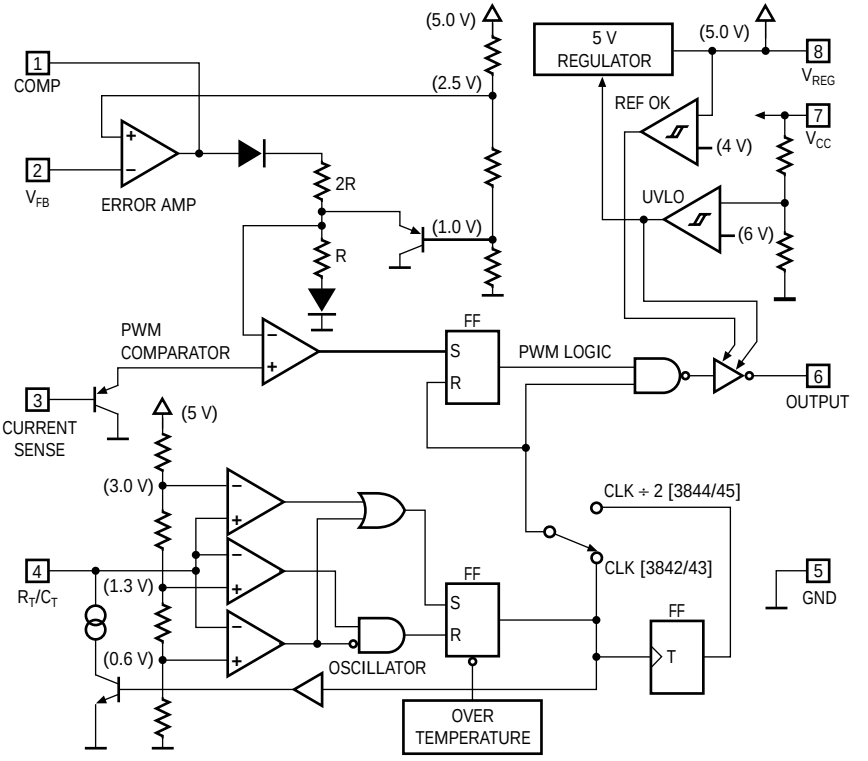


Figure 1. Block Diagram of the AS3842/3/4/5

Pin Function Description

Pin Number	Function	Description
1	COMP	This pin is the error amplifier output. Typically used to provide loop compensation to maintain V_{FB} at 2.5 V.
2	V_{FB}	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V bandgap reference.
3	Current Sense	A voltage proportional to inductor current is connected to the input. The PWM uses this information to terminate the gate drive of the output.
4	R_T/C_T	Oscillator frequency and maximum output duty cycle are set by connecting a resistor (R_T) to V_{REG} and a capacitor (C_T) to ground. Pulling this pin to ground or to V_{REG} will accomplish a synchronization function.
5	GND	Circuit common ground, power ground, and IC substrate.
6	Output	This output is designed to directly drive a power MOSFET switch. This output can sink or source peak currents up to 1A. The output for the AS3844/5 switches at one-half the oscillator frequency.
7	V_{CC}	Positive supply voltage for the IC.
8	V_{REG}	This 5 V regulated output provides charging current for the capacitor C_T through the resistor R_T.

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 105°C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
PWM						
Maximum Duty Cycle	D_{max}	3842/3	94	97	100	%
Minimum Duty Cycle	D_{min}	3842/3			0	%
Maximum Duty Cycle	D_{max}	3844/5	49	49.5	50	%
Minimum Duty Cycle	D_{min}	3844/5			0	%
Supply Current						
Start-up Current	I_{CC}	3842/4, V_{FB} = V_{SENSE} = 0 V, V_{CC} = 14 V		0.5	1.0	mA
		3843/5, V_{FB} = V_{SENSE} = 0 V, V_{CC} = 7 V		0.3	0.5	mA
Operating Supply Current	I_{CC}			9	17	mA
V_{CC} Zener Voltage	V_Z	I_{CC} = 25 mA		30		V

Notes:

1. This parameter is not 100% tested in production.
2. Parameter measured at trip point of PWM latch.
3. Transfer gain is the relationship between current sense input and corresponding error amplifier output at the PWM latch trip point and is mathematically expressed as follows:

$$A = \frac{\Delta I_{COMP}}{\Delta V_{SENSE}}; -0.2 \leq V_{SENSE} \leq 0.8\,V$$

4. At the over-temperature threshold, T_{OT}, the oscillator is disabled. The 5 V reference and the PWM stages, including the PWM latch, remain powered.

Typical Performance Curves

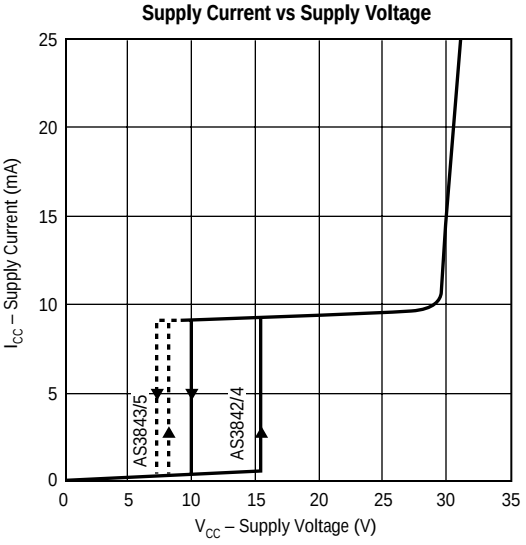


Figure 2

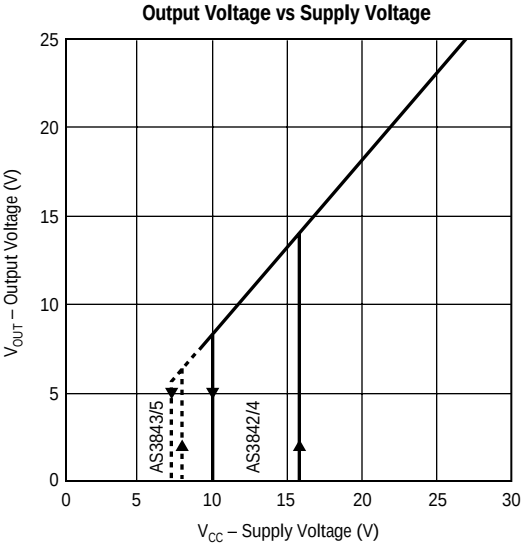


Figure 3

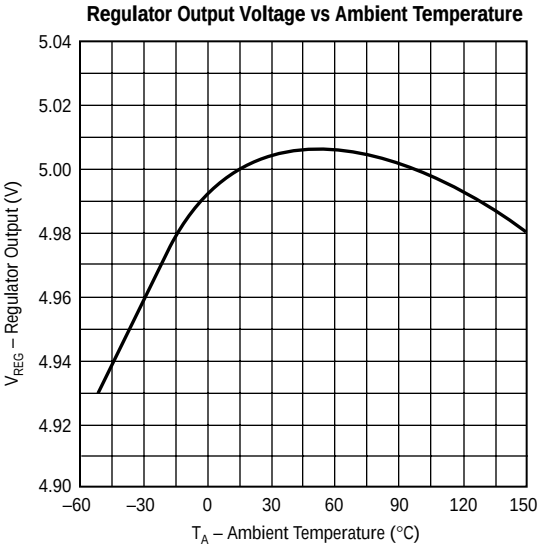


Figure 4

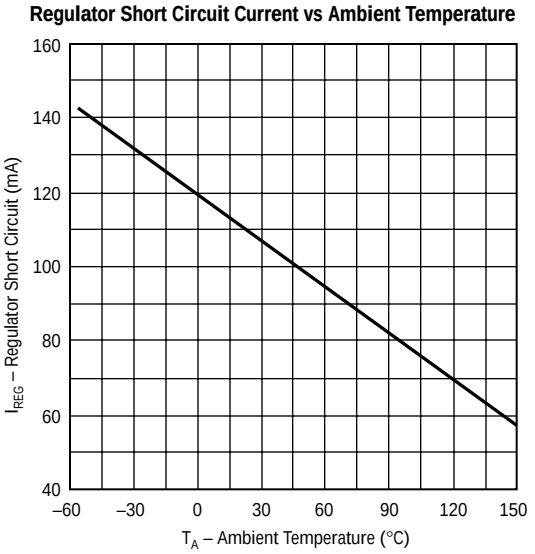


Figure 5

Typical Performance Curves

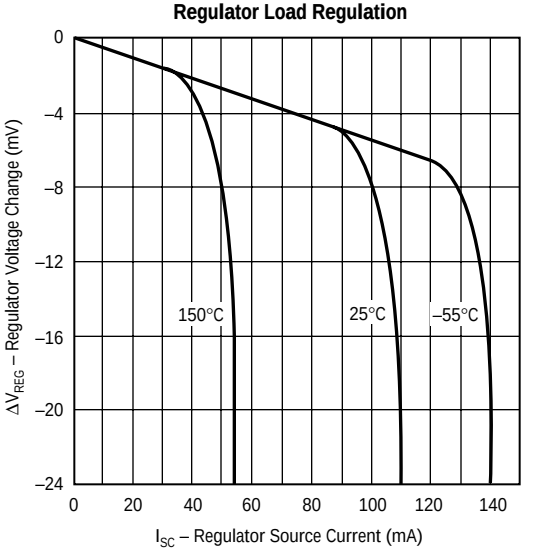


Figure 6

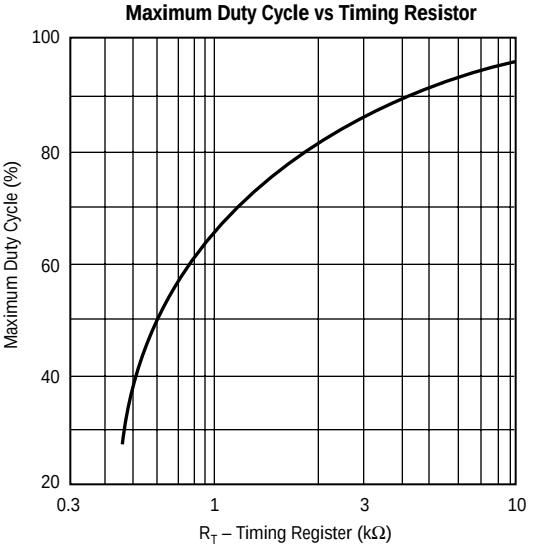


Figure 7

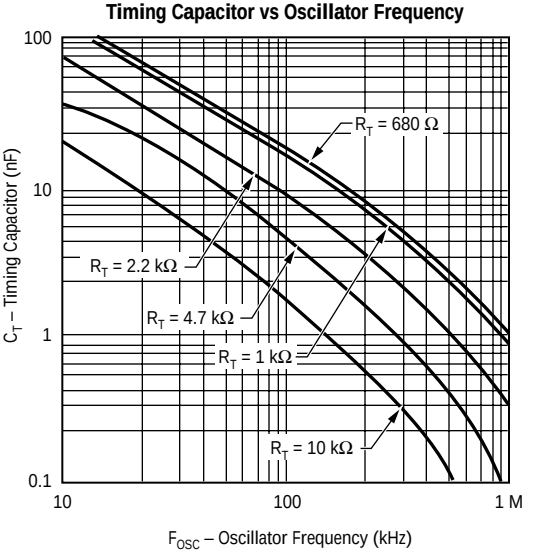


Figure 8

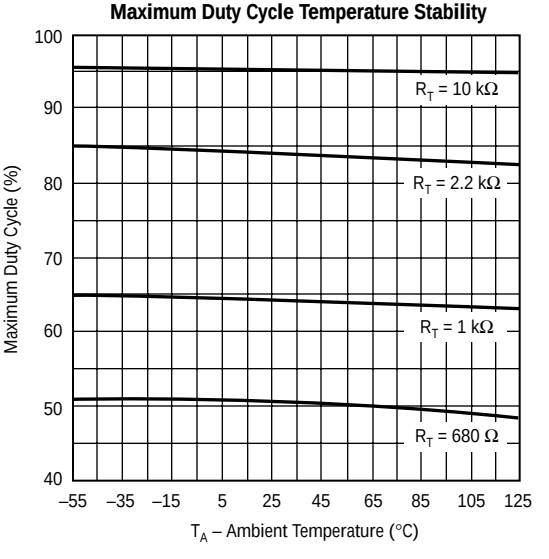


Figure 9

Typical Performance Curves

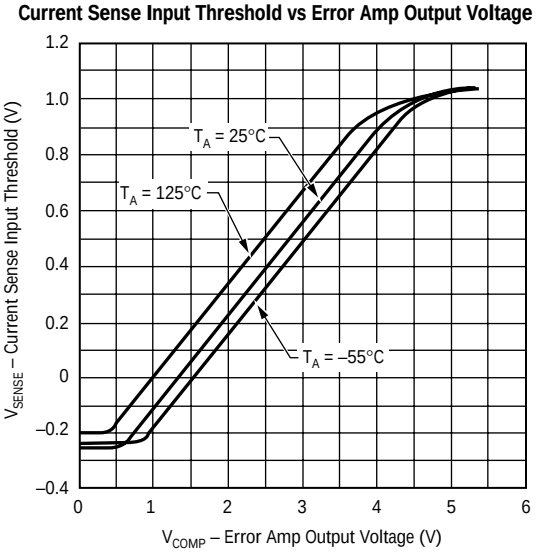


Figure 10

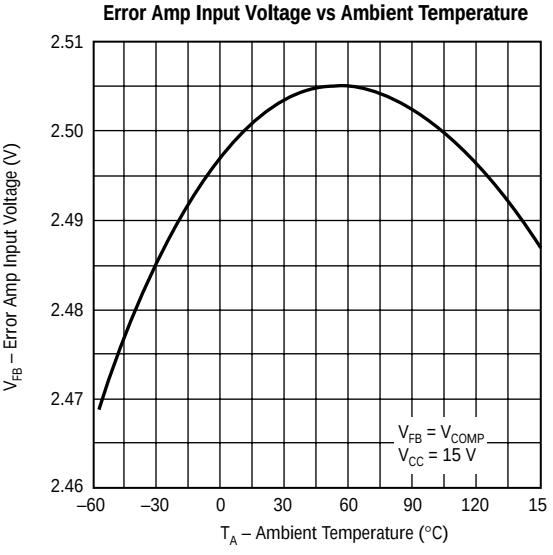


Figure 11

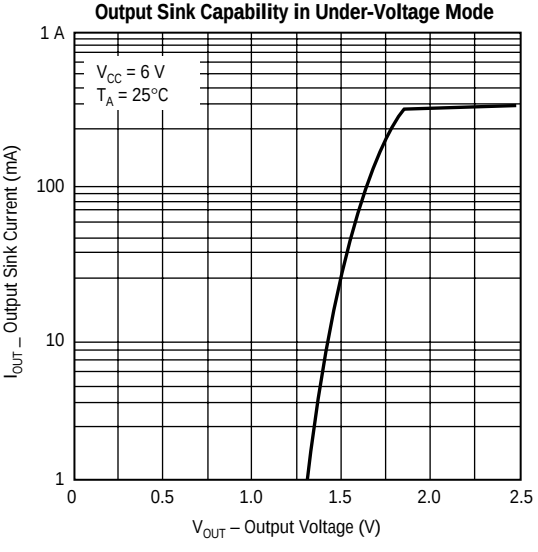


Figure 12

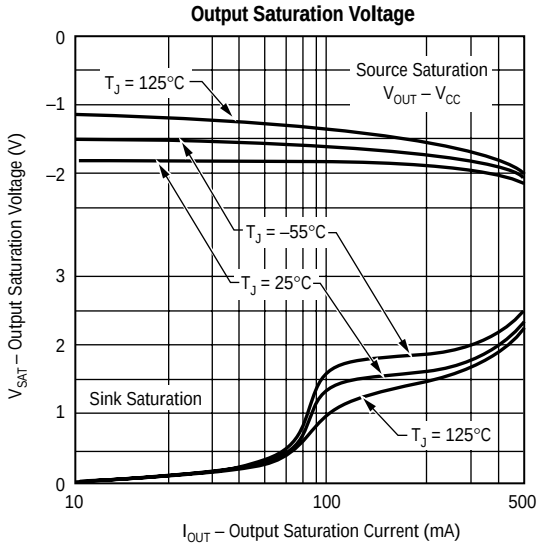


Figure 13

Application Information

The AS3842/3/4/5 family of current-mode control ICs are low cost, high performance controllers which are pin compatible with the industry standard UC3842 series of devices. Suitable for many switch mode power supply applications, these ICs have been optimized for use in high frequency off-line and DC-DC converters. The AS3842 has been enhanced to provide significantly improved performance, resulting in exceptionally better tolerances in power supply manufacturing. In addition, all electrical characteristics are guaranteed over the full 0 to 105°C temperature range. Among the many enhancements are: a precision trimmed 2.5 volt reference (+/– 1% of nominal at the error amplifier input), a significantly reduced propagation delay from current sense input to the IC output, a trimmed oscillator for precise duty-cycle clamping, a modified flip-flop scheme that gives a true 50% duty ratio clamp on 3844/45 types, and an improved 5 V regulator for better AC noise immunity. Furthermore, the AS3842 provides guaranteed performance with current sense input below ground. The advanced oscillator design greatly simplifies synchronization. The device is more completely specified to guarantee all parameters that impact power supply manufacturing tolerances.

Section 1 – Theory of Operation

The functional block diagram of the AS3842 is shown in Figure 1. The IC is comprised of the six basic functions necessary to implement current mode control; the under-voltage lockout; the reference; the oscillator; the error amplifier; the current sense comparator/PWM latch; and the output. The following paragraphs will describe the theory of operation of each of the functional blocks.

1.1 Under-voltage lockout (UVLO)

The under-voltage lockout function of the AS3842 holds the IC in a low quiescent current (≤ 1 mA) “standby” mode until the supply voltage (V_{CC}) exceeds the upper UVLO threshold voltage. This guarantees that all of the IC’s internal circuitry are properly biased and fully functional before the output stage is enabled. Once the IC turns on, the UVLO threshold shifts to a lower level (hysteresis) to prevent V_{CC} oscillations.

The low quiescent current standby mode of the AS3842 allows “bootstrapping”—a technique used in off-line converters to start the IC from the rectified AC line voltage initially, after which power to the IC is provided by an auxiliary winding off the power supply’s main transformer. Figure 14 shows a typical bootstrap circuit where capacitor (C) is

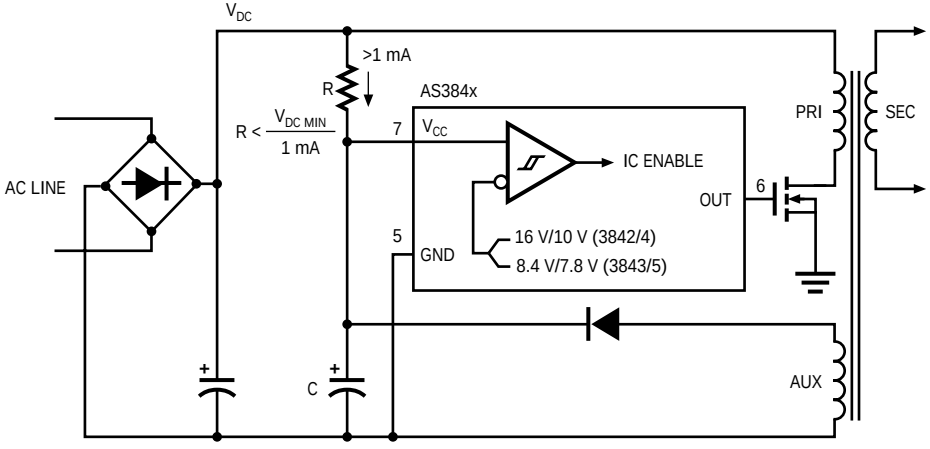


Figure 14. Bootstrap Circuit

the following paragraphs. The basic operation of the oscillator is as follows:

A simple RC network is used to program the frequency and the maximum duty ratio of the AS3842 output. See Figure 15. Timing capacitor (C_T) is charged through timing resistor (R_T) from the fixed 5.0 V at V_{REG}. During the charging time, the OUT (pin 6) is high. Assuming that the output is not terminated by the PWM latch, when the voltage across C_T reaches the upper oscillator trip point (≈3.0 V), an internal current sink from pin 4 to ground is turned on and discharges C_T towards the lower trip point. During this discharge time, an internal clock pulse blanks the output to its low state. When the voltage across C_T reaches the lower trip point (≈1.3 V), the current sink is turned off, the output goes high, and the cycle repeats. Since the output is blanked during the discharge of C_T, it is the discharge time which controls the output deadtime and hence, the maximum duty ratio.

The nature of the AS3842 oscillator circuit is such that, for a given frequency, many combinations of R_T and C_T are possible. However, only one value of R_T will yield the desired maximum duty ratio at a given frequency. Since a precise maximum duty ratio clamp is critical for many power supply designs, the oscillator discharge current is trimmed in a unique manner which provides significantly improved tolerances as explained later in this section. In addition, the AS3844/5 options have an internal flip-flop which effectively blanks every other output pulse (the oscillator runs at twice the output frequency), providing an absolute maximum 50% duty ratio regardless of discharge time.

1.3.1 Selecting timing components R_T and C_T

The values of R_T and C_T can be determined mathematically by the following expressions:

$$C_T = \frac{D}{R_T f_{OSC} \ln\left(\frac{K_L}{K_H}\right)} = \frac{1.63D}{R_T f_{OSC}} \qquad (1)$$

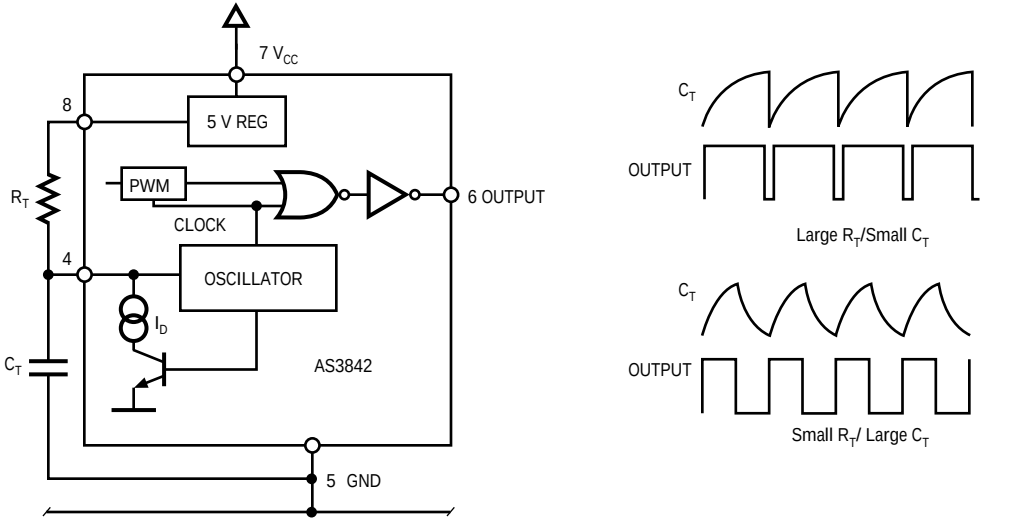


Figure 15. Oscillator Set-up and Waveforms

$$R_T = \frac{V_{REG}}{I_D} \bullet \frac{(K_L)^{\frac{1}{D}} - (K_H)^{\frac{1}{D}}}{(K_L)^{\frac{1-D}{D}} - (K_H)^{\frac{1-D}{D}}} \quad (2)$$

$$= 582 \bullet \frac{(0.736)^{\frac{1}{D}} - (0.432)^{\frac{1}{D}}}{(0.736)^{\frac{1-D}{D}} - (0.432)^{\frac{1-D}{D}}}$$

$$K_L = \frac{V_{REG} - V_L}{V_{REG}} \approx 0.736 \quad (3)$$

$$K_H = \frac{V_{REG} - V_H}{V_H} \approx 0.432 \quad (4)$$

where f_{osc} is the oscillator frequency, D is the maximum duty ratio, V_H is the oscillator's upper trip point, V_L is the lower trip point, V_R is the Reference voltage, I_D is the discharge current.

Table 1 lists some common values of R_T and the corresponding maximum duty ratio. To select the timing components; first, use Table 1 or equation (2) to determine the value of R_T that will yield the desired maximum duty ratio. Then, use equation (1) to calculate the value of C_T. For example, for a switching frequency of 250 kHz and a maximum duty ratio of 50%, the value of R_T, from Table 1, is 683 Ω. Applying this value to equation (1) and solving for C_T gives a value of 4700 pF. In practice, some fine tuning of the initial values may be necessary during design. However, due to the advanced design of the AS3842 oscillator, once the final values are determined, they will yield repeatable results, thus eliminating the need for additional trimming of the timing components during manufacturing.

1.3.2 Oscillator enhancements

The AS3842 oscillator is trimmed to provide guaranteed duty ratio clamping. This means that the discharge current (I_D) is trimmed to a value that compensates for all of the tolerances within the device (such as the tolerances of V_{REG}, propagation delays, the oscillator trip points, etc.) which have an effect on the frequency and maximum duty ratio. For example, if the combined tolerances of a particular device are 0.5% above nominal, then I_D is trimmed to 0.5% above nominal. This method of trimming virtually eliminates the need to trim external oscillator components during power supply manufacturing. Standard 3842 devices specify or trim only for a specific value of discharge current. This makes precise

Table 1. RT vs Maximum Duty Ratio

R_T (Ω)	Dmax
470	22%
560	37%
683	50%
750	54%
820	58%
910	63%
1,000	66%
1,200	72%
1,500	77%
1,800	81%
2,200	85%
2,700	88%
3,300	90%
3,900	91%
4,700	93%
5,600	94%
6,800	95%
8,200	96%
10,000	97%
18,000	98%

and repeatable duty ratio clamping virtually impossible due to other IC tolerances. The AS3844/5 provides true 50% duty ratio clamping by virtue of excluding from its flip-flop scheme, the normal output blanking associated with the discharge of C_T. Standard 3844/5 devices include the output blanking associated with the discharge of C_T, resulting in somewhat less than a 50% duty ratio.

1.3.3 Synchronization

The advanced design of the AS3842 oscillator simplifies synchronizing the frequency of two or more devices to each other or to an external clock. The R_T/C_T doubles as a synchronization input which can easily be driven from any open collector logic output. Figure 16 shows some simple circuits for implementing synchronization.

1.4 Error amplifier (COMP)

The AS3842 error amplifier is a wide bandwidth, internally compensated operational amplifier which provides a high DC open loop gain (90 dB). The input to the amplifier is a PNP differential pair. The non-inverting (+) input is internally connected to the 2.5 V reference, and the inverting (–) input is available at pin 2 (V_{FB}). The output of the error amplifier consists of an active pull-down and a 0.8 mA current source pull-up as shown in Figure 17. This type of output stage allows easy implementation of soft start, latched shutdown and reduced current sense clamp functions. It also permits wire “OR-ing” of the error amplifier outputs of several 3842s, or complete bypass of the error amplifier when its output is forced to remain in its “pull-up” condition.

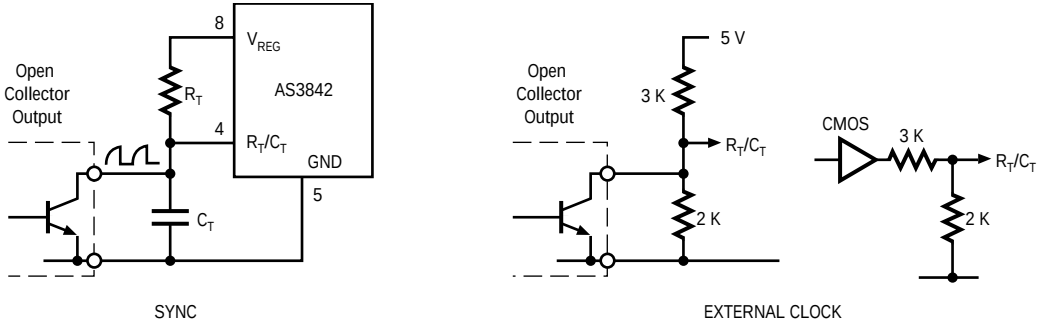


Figure 16. Synchronization

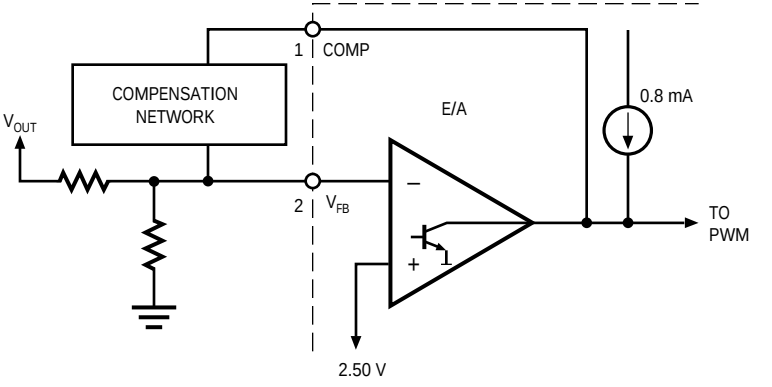


Figure 17. Error Amplifier Compensation

In most typical power supply designs, the converter's output voltage is divided down and monitored at the error amplifier's inverting input, V_{FB}. A simple resistor divider network is used and is scaled such that the voltage at V_{FB} is 2.5 V when the converter's output is at the desired voltage. The voltage at V_{FB} is then compared to the internal 2.5 V reference and any slight difference is amplified by the high gain of the error amplifier. The resulting error amplifier output is level shifted by two diode drops and is then divided by three to provide a 0 to 1 V reference (V_E) to one input of the current sense comparator. The level shifting reduces the input voltage range of the current sense input and prevents the output from going high when the error amplifier output is forced to its low state. An internal clamp limits V_E to 1.0 V. The purpose of the clamp is discussed in Section 1.5.

1.4.1 Loop compensation

Loop compensation of a power supply is necessary to ensure stability and provide good line/load regulation and dynamic response. It is normally provided by a compensation network connected between the error amplifier's output (COMP) and inverting input as shown in Figure 17. The type of network used depends on the converter topology and in particular, the characteristics of the major functional blocks within the supply — i.e. the error amplifier, the modulator/switching circuit, and the output filter. In general, the network is designed such that the converter's overall gain/phase response approaches that of a single pole with a –20 dB/decade rolloff, crossing unity gain at the highest possible frequency (up to $f_{SW}/4$) for good dynamic response, with adequate phase margin (> 45°) to ensure stability.

Figure 18 shows the Gain/Phase response of the error amplifier. The unity gain crossing is at 1.2 MHz with approximately 57°C of phase margin. This information is useful in determining the configuration and characteristics required for the compensation network.

One of the simplest types of compensation networks is shown in Figure 19. An RC network provides a single pole which is normally set to compensate for the zero introduced by the output capacitor's ESR. The frequency of the pole (f_P) is determined by the formula;

$$f_P = \frac{1}{2\pi\ R_f\ C_f} \qquad (5$$

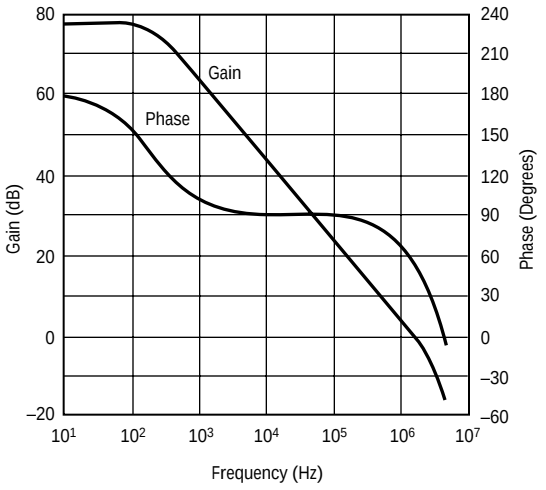


Figure 18. Gain/Phase Response of the AS3842

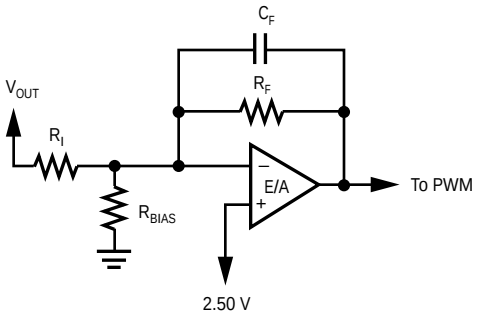


Figure 19. A Typical Compensation Network

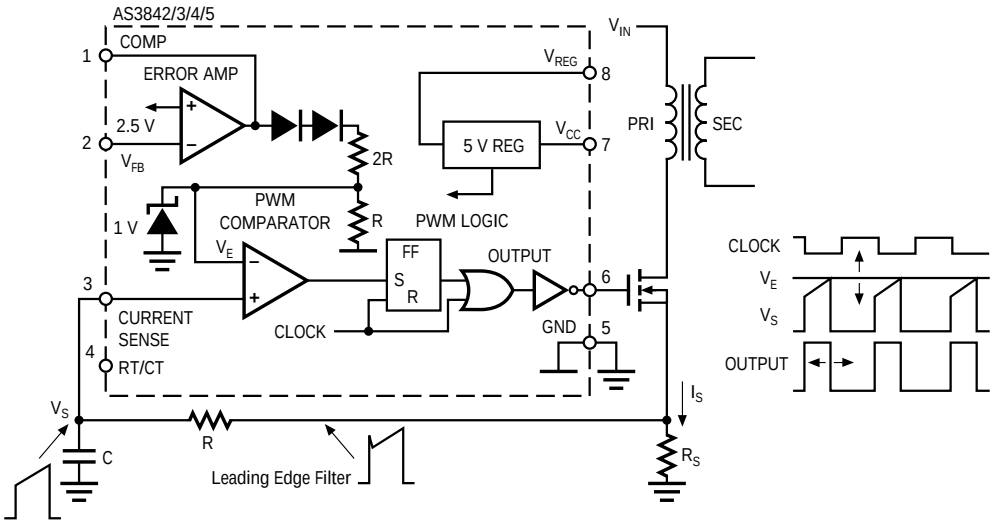


Figure 20. Current Sense/PWM Latch Circuit and Waveforms

The current sense comparator's inverting input is internally clamped to a level of 1.0 V to provide a current limit (or power limit for multiple output supplies) function. The value of R_S is selected to produce 1.0 V at the maximum allowed current. For example, if 1.5 A is the maximum allowed peak inductor current, then R_S is selected to equal 1 V/1.5 A = 0.66 Ω. In high power applications, power dissipation in the current sense resistor may become intolerable. In such a case, a current transformer can be used to step down the current seen by the sense resistor. See Figure 21.

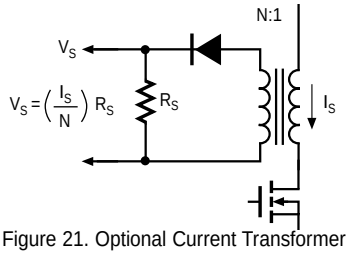


Figure 21. Optional Current Transformer

1.6 Output (OUT)

The output stage of the AS3842 is a high current totem-pole configuration that is well suited for directly driving power MOSFETs. It is capable of sourcing and sinking up to 1 A of peak current. Cross conduction losses in the output stage have been minimized resulting in lower power dissipation in the device. This is particularly important for high frequency operation. During under-voltage shutdown conditions, the output is active low. This eliminates the need for an external pull-down resistor.

1.7 Over-temperature shutdown

The AS3842 has a built-in over-temperature shutdown which will limit the die temperature to 130°C typically. When the over-temperature condition is reached, the oscillator is disabled. All other circuit blocks remain operational. Therefore, when the oscillator stops running, output pulses terminate without losing control of the supply or losing any peripheral functions that may be running off the 5 V regulator. The output may go high during the final cycle, but the PWM

latch is still fully operative, and the normal termination of this cycle by the current sense comparator will latch the output low until the over-temperature condition is rectified. Cycling the power will reset the over-temperature disable mechanism, or the chip will re-start after cooling through a nominal hysteresis band.

Section 2 – Design Considerations

2.1 Leading edge filter

The current sensed by R_S contains a leading edge spike as shown in Figure 20. This spike is caused by parasitic elements within the circuit including the interwinding capacitance of the power transformer and the recovery characteristics of the rectifier diode(s). The spike, if not properly filtered, can cause stability problems by prematurely terminating the output pulse.

A simple RC filter is used to suppress the spike. The time constant should be chosen such that it approximately equals the duration of the spike. A good choice for R_1 is 1 kΩ, as this value is optimum for the filter and at the same time, it simplifies the determination of R_{SLOPE} (Section 2.2). If the duration of the spike is, for example, 100 ns, then C is determined by:

$$C = \frac{\text{Time Constant}}{1\ \text{k}\Omega} \quad (6)$$

$$= \frac{100\ \text{ns}}{1\ \text{k}\Omega}$$

$$= 100\ \text{pF}$$

2.2 Slope compensation

Current-mode controlled converters can experience instabilities or subharmonic oscillations

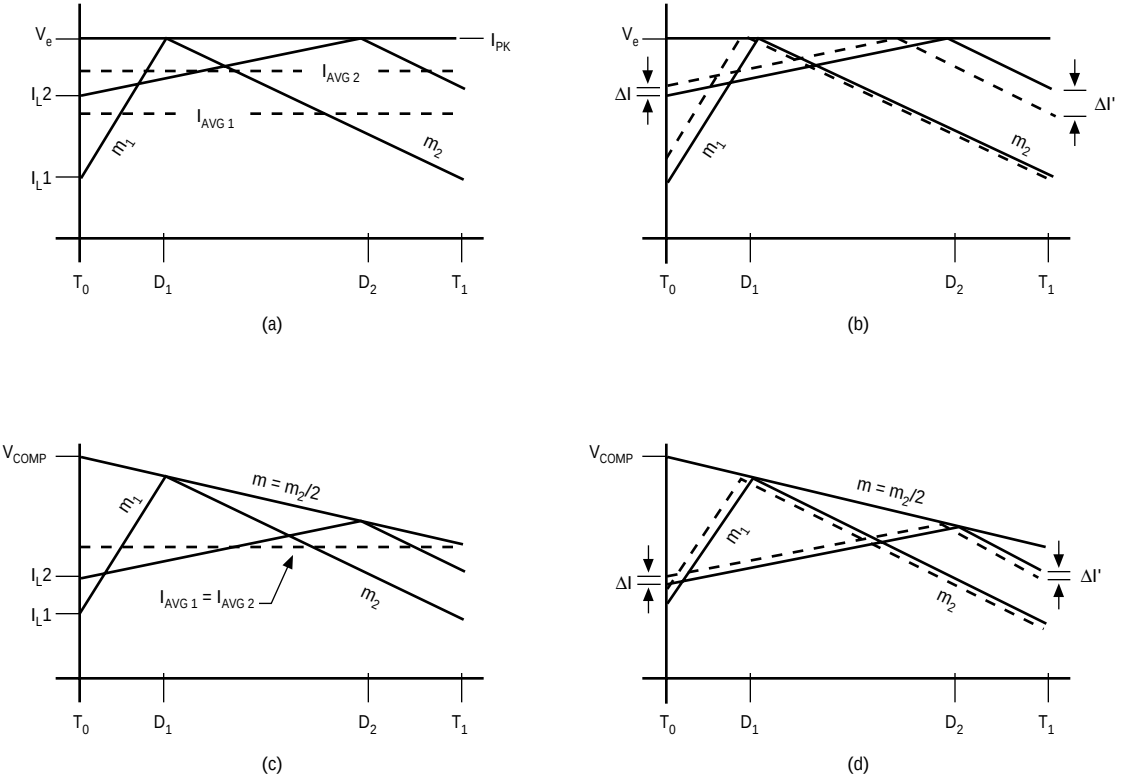


Figure 22. Slope Compensation

when operated at duty ratios greater than 50%. Two different phenomena can occur as shown graphically in Figure 22.

First, current-mode controllers detect and control the peak inductor current, whereas the converter's output corresponds to the average inductor current. Figure 22(a) clearly shows that the average inductor current (I_1 & I_2) changes as the duty ratio (D_1 & D_2) changes. Note that for a fixed control voltage, the peak current is the same for any duty ratio. The difference between the peak and average currents represents an error which causes the converter to deviate from true current-mode control.

Second, Figure 22(b) depicts how a small perturbation of the inductor current (ΔI) can result in an unstable condition. For duty ratios less than 50%, the disturbance will quickly converge to a steady state condition. For duty ratios greater than 50%, ΔI progressively increases on each cycle, causing an unstable condition.

Both of these problems are corrected simultaneously by injecting a compensating ramp into either the control voltage (V_E) as shown in Figure 22(c) & (d), or to the current sense waveform at pin 3. Since V_E is not directly accessible, and, a positive ramp waveform is readily available from the oscillator at pin 4, it is more practical to add the slope compensation to the current waveform. This can be implemented quite simply with the addition of a single resistor, R_{SLOPE}, between pin 4 and pin 3 as shown in Figure 23(a). R_{SLOPE}, in conjunction with the leading edge filter resistor, R_1 (Section 2.1), forms a divider network which determines the amount of slope added to the waveform. The amount of slope added to the current waveform is inversely proportional to the value of R_{SLOPE}. It has been determined that the amount of slope (m) required is equal to or greater than 1/2 the downslope (m_2) of the inductor current. Mathematically stated:

$$m \geq \frac{m_2}{2} \qquad (7)$$

In some cases the required value of R_{SLOPE} may be low enough to affect the oscillator circuit and thus cause the frequency to shift. An emitter follower circuit can be used as a buffer for R_{SLOPE} as depicted in Figure 23(b).

Slope compensation can also be used to improve noise immunity in current mode converters operating at less than 50% duty ratio. Power supplies operating under very light load can experience

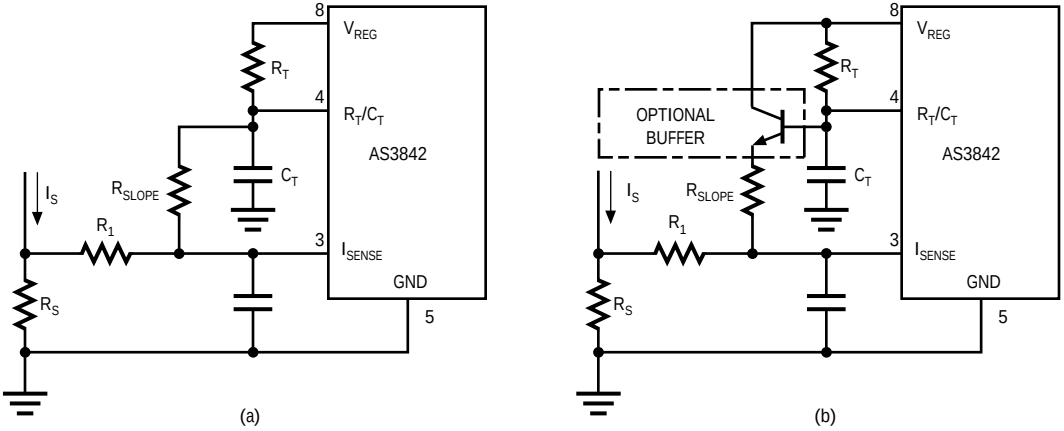


Figure 23. Slope Compensation