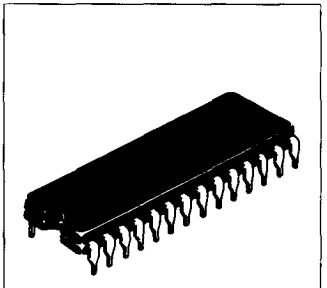
HN58064P-25,HN58064P-30, HN58064P-45

Preliminary

8192-word x 8-bit Electrically Erasable and Programmable ROM

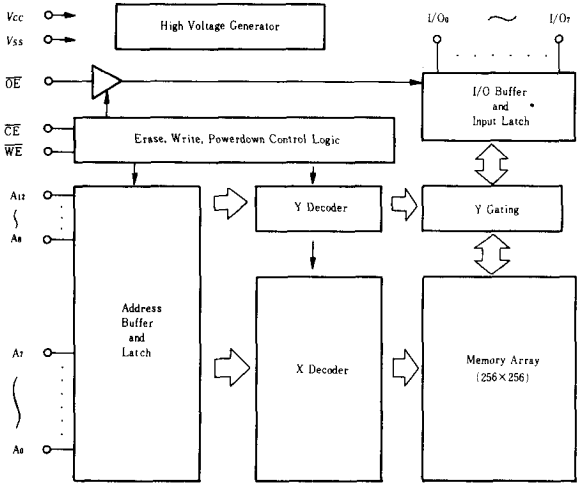
■ FEATURES

- Single 5V Supply
- Address, Data, $\overline{CE}$, $\overline{OE}$ Lathes
- Byte Erase/Byte Write Time . . . . . 10ms typ.
- Chip Erase Time . . . . . 20ms typ.
- Fast Access Time . . . . . 250/300/450ns max.
- Low Power Disispation . . . . . 100mA (max) Active
  40mA (max) Standby
- Comforms to JEDEC Byte-Wide Standard
- Reliable N-channel MNOS Technology
- 10000 Erase/Write Cycles

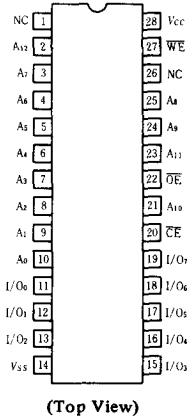


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	D_{out}
Standby	V_{IH}	X	X	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IL}	$D_{in} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{in}
Chip Erase	V_{IL}	V_{IL}	V_{IL}	$D_{in} = V_{IH}$
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z

X: V_{IL} or V_{IH}

$A_0 \sim A_{12}$	Address Input
$I/O_0 \sim I/O_7$	Data in/Data out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	GND
NC	No Connect

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	− 55 to +125	°C

* With Respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.1	–	0.8	V
	V_{IH}	2.0	–	V_{CC}+1	V
Operating Temperature	T_{opr}	0	–	70	°C

■ DC AND OPERATING CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V +10%)

Parameter	Symbol	Test Condition	min	typ	max	unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = 5.5V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V V_{out} = 5.5 ~ 0.4V	–	–	10	μA
V_{CC} Current (Standby)	I_{CC1}		–	20	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	60	100	mA
Input Low Voltage	V_{IL}		−0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	–	–	V

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min	typ	max	unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{in} = 0V	–	–	12	pF

■ AC TEST CONDITIONS

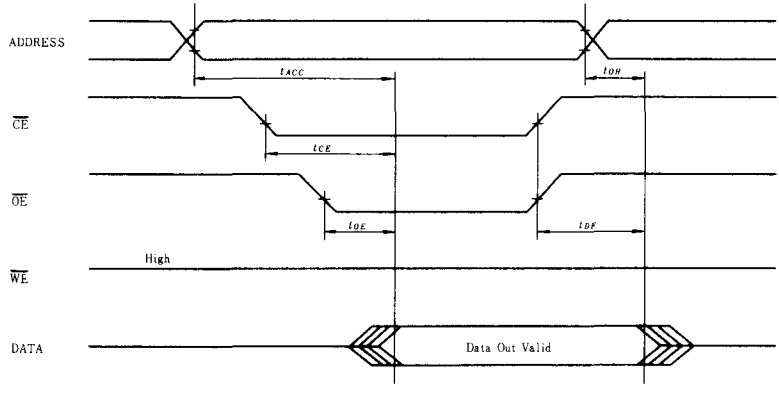
Input Pulse Levels:	0.8V to 2.0V Input
Rise and Fall Time:	≦ 20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V Outputs; 0.8V and 2.0V

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V + 10%)

● READ OPERATION

Parameter	Symbol	Test Condition	HN58064P-25		HN58064P-30		HN58064P-45		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	–	300	–	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	–	300	–	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	100	–	150	–	150	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	–	0	–	0	–	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	90	0	130	0	130	ns

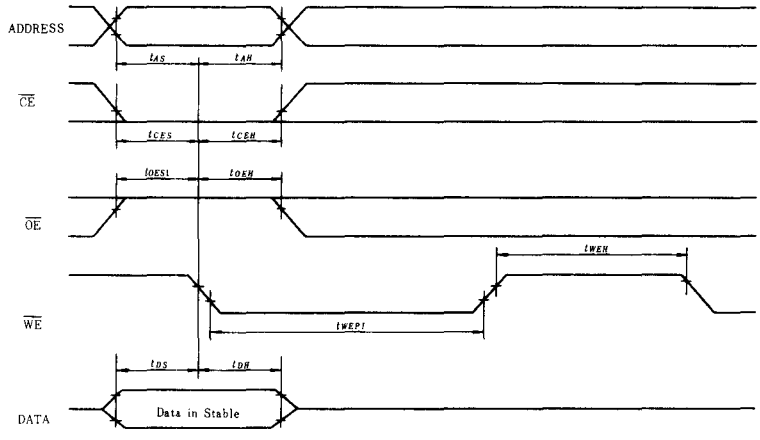
● WAVEFORM ····· READ CYCLE



● BYTE ERASE AND BYTE WRITE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		10	–	–	ns
Address Hold Time	t_{AH}		50	–	–	ns
$\overline{CE}$ Setup Time	t_{CES}		10	–	–	ns
$\overline{CE}$ Hold Time	t_{CEH}		50	–	–	ns
$\overline{OE}$ Setup Time	t_{OES1}		10	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}		50	–	–	ns
$\overline{WE}$ Pulse Width	t_{WEP1}		8	10	15	ms
$\overline{WE}$ High Time	t_{WEH}		500	–	–	ns
Data Setup Time	t_{DS}		10	–	–	ns
Data Hold Time	t_{DH}		50	–	–	ns

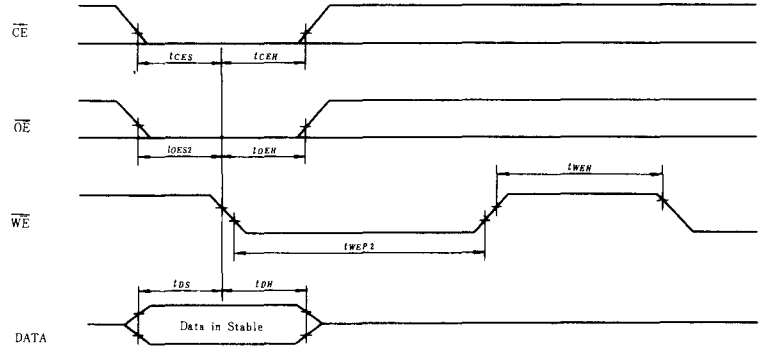
● WAVEFORM ····· ERASE AND WRITE CYCLE



● CHIP ERASE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
$\overline{CE}$ Setup Time	t_{CES}		10	–	–	ns
$\overline{CE}$ Hold Time	t_{CEH}		50	–	–	ns
$\overline{OE}$ Setup Time	t_{OES2}		0	–	50	ns
$\overline{OE}$ Hold Time	t_{OEH}		50	–	–	ns
$\overline{WE}$ Pulse Width	t_{WEP2}		15	20	50	ms
$\overline{WE}$ High Time	t_{WEH}		500	–	–	ns
Data Setup Time	t_{DS}		10	–	–	ns
Data Hold Time	t_{DH}		50	–	–	ns

WAVE FORM ····· CHIP ERASE



● SEQUENCE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
$\overline{WE}$ Setup Time	t_{WES}		150	–	–	ns
$\overline{WE}$ to $\overline{OE}$ Time	t_{WO}		50	–	–	ns
$\overline{WE}$ High Time	t_{WEH}		500	–	–	ns

● WAVE FORM