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INTERSIL

ICL8052/8053 (3½ Digit)
ICL8052A/8053A (4½ Digit)
Precision Chip Pairs for A/D Conversion

FEATURES
- Accuracy high enough for ±40,000 count instruments
- Priced low enough to compete with 3-1/2 digit DPM/DVM pairs
- One basic circuit for an entire family of DVMs
- Auto-Zero; Auto-Polarity
- 5pA typical input current
- Single reference voltage
- True ratiometric (scale factor of 1)

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ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to +70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to +70°C	14 pin ceramic DIP	ICL8052CDD
8052A	0°C to +70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to +70°C	14 pin ceramic DIP	ICL8052ACDD
8053	0°C to +70°C	14 pin plastic DIP	ICL8053CPD
8053	0°C to +70°C	14 pin ceramic DIP	ICL8053CDD
8053A	0°C to +70°C	14 pin plastic DIP	ICL8053ACPD
8053A	0°C to +70°C	14 pin ceramic DIP	ICL8053ACDD

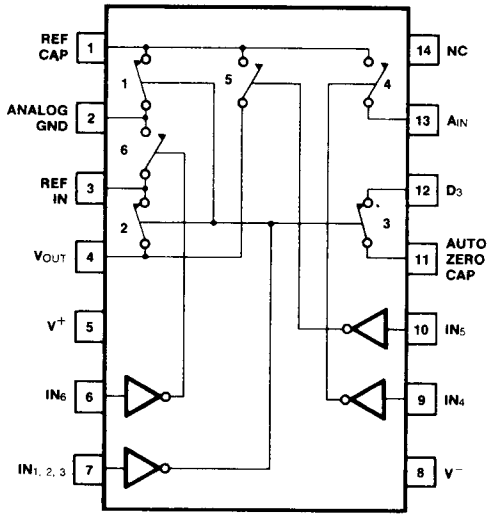
GENERAL DESCRIPTION

The ICL8052/8053 pair has been designed to "lock-in" the accuracy of a DVM and at the same time give the designer the freedom of using any output format his system requires. With reasonable care, the 0.001% linearity capability of the pair can be maintained in production instruments. The system uses time-proven dual-slope integration with all of its advantages: i.e., non-critical components, high rejection of noise and a-c signals, non-critical clock frequency and true ratiometric readings. At the same time it has reduced or eliminated many of the sources of error that have limited dual-slope accuracy. With the ICL8052/8053 pairs, critical board layout is no longer required to give low charge injection by the switches, and elaborate ground planes are not necessary to keep clock pulse transients out of the comparator circuitry. A further feature of these devices is that the DVM/DPM manufacturer can generate an entire family of instruments using only one basic p-c board with 2 or 3 jumper points. The family could include:

±200.0 mV Full Scale
±2.000 Volts
±400.0 mV
±4.000 Volts
±800.0 mV
±2.0000 Volts
±4.0000 Volts
±3.2768 Volts (16 bits in 0.1 mV increments)

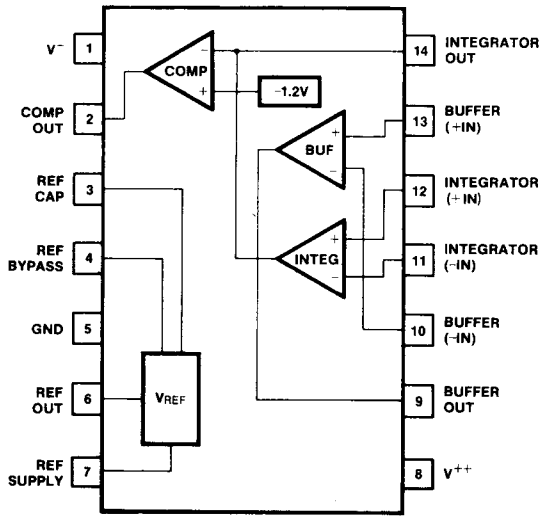
CONNECTION DIAGRAM

8053 Auto Zero Switch Network



(Outline dwg DD, PD)

8052 Analog Signal Conditioner



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ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 500 mW
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C

ICL8052 ONLY

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration,
All Outputs (Note 3) ..... Indefinite

ICL8053 ONLY

Source Current (I_S) ..... 100 mA
Drain Current (I_D) ..... 100 mA
Digital Inputs ..... 5 mA
V^+ to V^- 25V
Digital Input ..... V^- to V^+

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL8053 ELECTRICAL CHARACTERISTICS (V^+ = +5V, V^- = −15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	ICL8053			ICL8053A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
R_{on} Switch 1, 3 (each Switch)	V_7 = +4.5V $V_6 = V_9 = V_{10}$ = +0.5V		1000	2500		1000	2500	Ω
R_{on} Switch 2	Same as Switch 1, 2		2000	5000		2000	5000	Ω
R_{on} Switch 4	V_9 = +4.5V $V_6 = V_7 = V_{10}$ = +0.5V		1000	2500		1000	2500	Ω
R_{on} Switch 5	V_{10} = +4.5V $V_6 = V_7 = V_9$ = +0.5V		1000	2500		1000	2500	Ω
R_{on} Switch 6	V_6 = +4.5V $V_7 = V_9 = V_{10}$ = +0.5V		1000	2500		1000	2500	Ω
Total Leakage Sw 1, 2, 5 & 6 $I_1 + I_3$ @ most positive Voltage	$V_6 = V_7 = V_9 = V_{10}$ = +0.5V V_4 = −4V, V_2 = 0V $V_1 = V_3$ = +4V		10	50		5	20	pA
Total Leakage Sw 1, 2, 5 & 6 $I_1 + I_3$ @ most negative Voltage	$V_6 = V_7 = V_9 = V_{10}$ = +0.5V V_4 = +4V, V_2 = 0V $V_1 = V_3$ = −4V		10	50		5	20	pA
Total Leakage Sw 3 & 4 $I_{12} + I_{13}$ @ most positive Volt.	$V_6 = V_7 = V_9 = V_{10}$ = +0.5V $V_1 = V_{11}$ = −4V $V_{12} = V_{13}$ = +4V		10	50		5	20	pA
Total Leakage Sw 3 & 4 $I_{12} + I_{13}$ @ most negative Volt.	$V_6 = V_7 = V_9 = V_{10}$ = +0.5V $V_1 = V_{11}$ = +4V $V_{12} = V_{13}$ = −4V		10	50		5	20	pA
Supply Current (V^+ or V^-)	$V_{6, 7, 9 \text{ or } 10}$ = 0.5V (each of 4 drivers)		150	300		150	300	μA
	$V_{6, 7, 9 \text{ and } 10}$ = 4.5V (all drivers)		1	10		1	10	μA
Supply Voltage Range V+ V−		4 −12	5 −15	8 −16	4 −12	5 −15	8 −16	V
Switching Time t_{on} t_{off}	See Figure 1 See Figure 1		75 150			75 150		nsec nsec

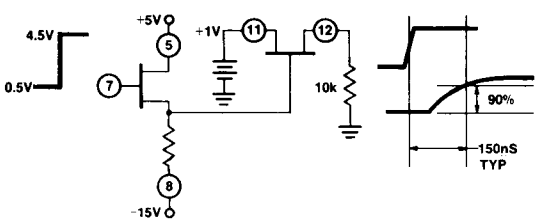
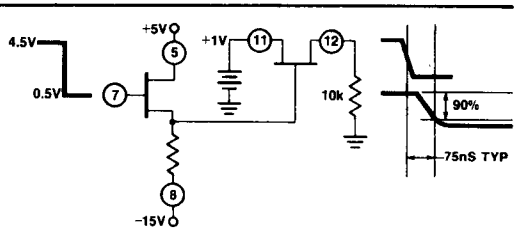


Figure 1: Turn-on Switching Time



Turn-off Switching Time

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8052 ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	CONDITIONS	8052 MIN	8052 TYP	8052 MAX	8052A MIN	8052A TYP	8052A MAX	UNITS
	EACH OPERATIONAL AMPLIFIER								
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	75		20	75	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
A_V	Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			1			1		MHz
I_{SC}	Output Short-Circuit Current			20	100		20	100	mA
	COMPARATOR AMPLIFIER								
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
	VOLTAGE REFERENCE								
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPP}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPP}	Supply Current Total			6	12		6	12	mA

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Note 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA$ Pd where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 2: This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS (V^{++} = +15V, V^{+} +5V, V^{-} = −15V; Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	ICL8052/8053 (3) MIN	ICL8052/8053 (3) TYP	ICL8052/8053 (3) MAX	ICL8052A/8053A (4) MIN	ICL8052A/8053A (4) TYP	ICL8052A/8053A (4) MAX	UNITS
Zero Input Reading	V_{in} = 0.0V	−0.000	±0.000	+0.000	−0.0000	±0.0000	+0.0000	Digital Reading
Ratiometric Reading	$V_{in} = V_{Ref.}$	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \le V_{in} \le +2V$		0.2	1		0.5	1	Digital Count Error
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV		0.2					Digital Count
	Full scale = 2.000V		0.05			0.3		
Leakage Current into Input	V_{in} = 0V		5	30		3	10	pA
Zero Reading Drift	V_{in} = 0V $0° \le T_A \le 70°C$		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0 \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		3	15		2	5	ppm/°C

Notes:

(3) Tested in 3-1/2 digit (2,000 count) circuit shown in Fig. 5; clock frequency 12 kHz.
(4) Tested in 4-1/2 digit (20,000 count) circuit shown in Fig. 5; clock frequency 120 kHz.

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THEORY OF OPERATION

Figure 4 shows a function diagram for an A-D converter using the ICL8052/8053 pair. In this circuit, each measurement cycle is divided into four equal parts by the state F/F. The first part, state 00, is the auto-zero cycle. The switch driver decoder recognizes this state and turns on hex switches number 1, 2, and 3. Switches 1 and 2 impress a voltage equal to V_{REF} across the reference capacitor. Switch 3 closes a loop around the integrator and comparator. The purpose of this loop is to charge up the auto-zero capacitor until the integrator output no longer changes with time. During the second state, 01, switches 1, 2 and 3 are opened and switch 4 is closed. If the input voltage is zero, the buffer, integrator and comparator will see the same voltages that existed in the previous state. Thus, the integrator output will not change but will remain stationary during the entire signal-integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the auto-zero cycle and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this cycle, the sign of the ramp is latched into the polarity F/F. The final cycle, reference integrate, includes states 10 and 11. The switch driver decoder uses the output of the polarity F/F in deciding whether to close switch 5 or 6. If the input signal was positive, switch 6 is closed and a voltage which is V_{REF} more negative than during auto-zero is impressed on the buffer input. If the input signal was negative switch 5 is closed and a voltage which is V_{REF} more positive than during auto-zero is impressed on the buffer input. Thus, the reference capacitor generates the equivalent of a (+) reference of a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to zero. The time, or number of counts, required to do this is proportional to the input voltage. Since the reference cycle can be twice as long as the signal integrate cycle, the input voltage required to give a full scale reading $\equiv 2\ V_{REF}$. The circuit, as described to this point, is not new to this application. It has been used successfully for several years. However, this system makes three major contributions to the accuracy of this circuit. These are: (1) low charge injection, (2) junction FET op amp, and (3) zero-crossing flip-flop.

1. **Low Charge Injection.**

   During auto-zero, there is no problem in charging the capacitors to the correct voltage. The problem is getting the switches off without changing this voltage. As the gate is driven off, the gate-to-drain capacitance of the switch injects a charge on the reference or auto-zero capacitor, changing its voltage. The designer, using discrete components, is forced into critical board layouts where charges of opposite polarity are injected to compensate or neutralize the driver injection. This balance will be upset by any unit-to-unit variation of switch capacitance so at best the final design is a compromise. In the ICL8052/8053 the critical layout has been done on the semiconductor chip and need not concern the user. Also, since a silicon-gate process is used for the switches, the unit-to-unit variation is extremely low. The net result is to give an error due to charge injection that is so low it is difficult to measure; but certainly less than 5μV referred to the input.

2. **Junction FET Op Amps.**

   Both the buffer and integrator use junction FET inputs in a guarded circuit that reduces the voltage across the FET to 3 or 4 volts. At this voltage level, input leakage currents of 2 pA are typical. For typical component values 2 pA leakage contributes less than 2μV of error to the circuit. I theory, MOS FET's would contribute less leakage bu their increased noise would swamp out any improvemen by orders of magnitude.

3. **Zero-Crossing Flip Flop.**

   The problem that the zero-crossing flip-flop is designe to solve is shown in figure 2.

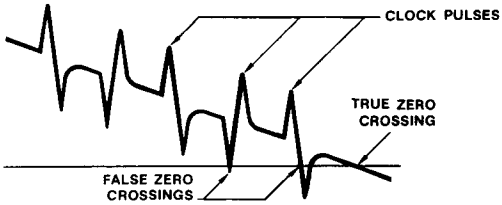

Figure 2: Integrator Output Near Zero-Crossing

The integrator output is approaching the zero-crossing poin where the clock will be stopped and the reading displayed The clock pulse feedthrough superimposed upon this ramp will cause a false reading by stopping the count prematurely For a 40,000 count instrument, the ramp is changing approximately 0.25mV per clock pulse (10 volt max integrator output divided by 40,000 counts). The clock pulses have to be less than 100μV peak to avoid causing significan errors. The circuit layout to achieve this can be time consuming at best and impossible at worst. The suggested circuit gets around this problem by feeding the zero crossing information into a J-K flip-flop instead of using i directly. The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. Any false zero-crossing caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance. If a correction was not made, the display would always be one count too high. The correction is to change the four states of the converter one count early. In othe words, instead of changing states at the beginning of coun 0000, the states are changed at the beginning of count 9999 Since this pulse is always available as "carry" from a synchronous counter, no extra decoding is required. A bonus feature of this circuit is that latching the counte output becomes very simple with no potential race conditior existing. The designer has one complete clock pulse to transfer the counter data to the latches and decouple them before a false reading will occur. The timing diagram for a signal ≈ 0 is shown in figure 3.

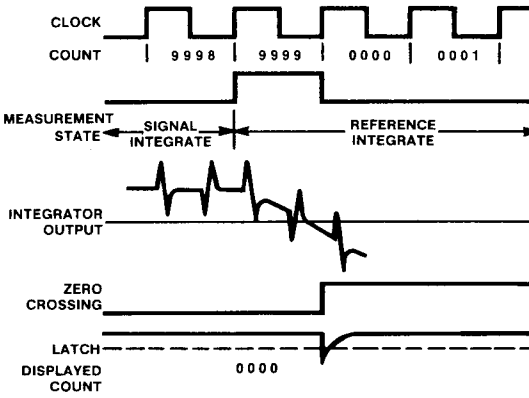

Figure 3

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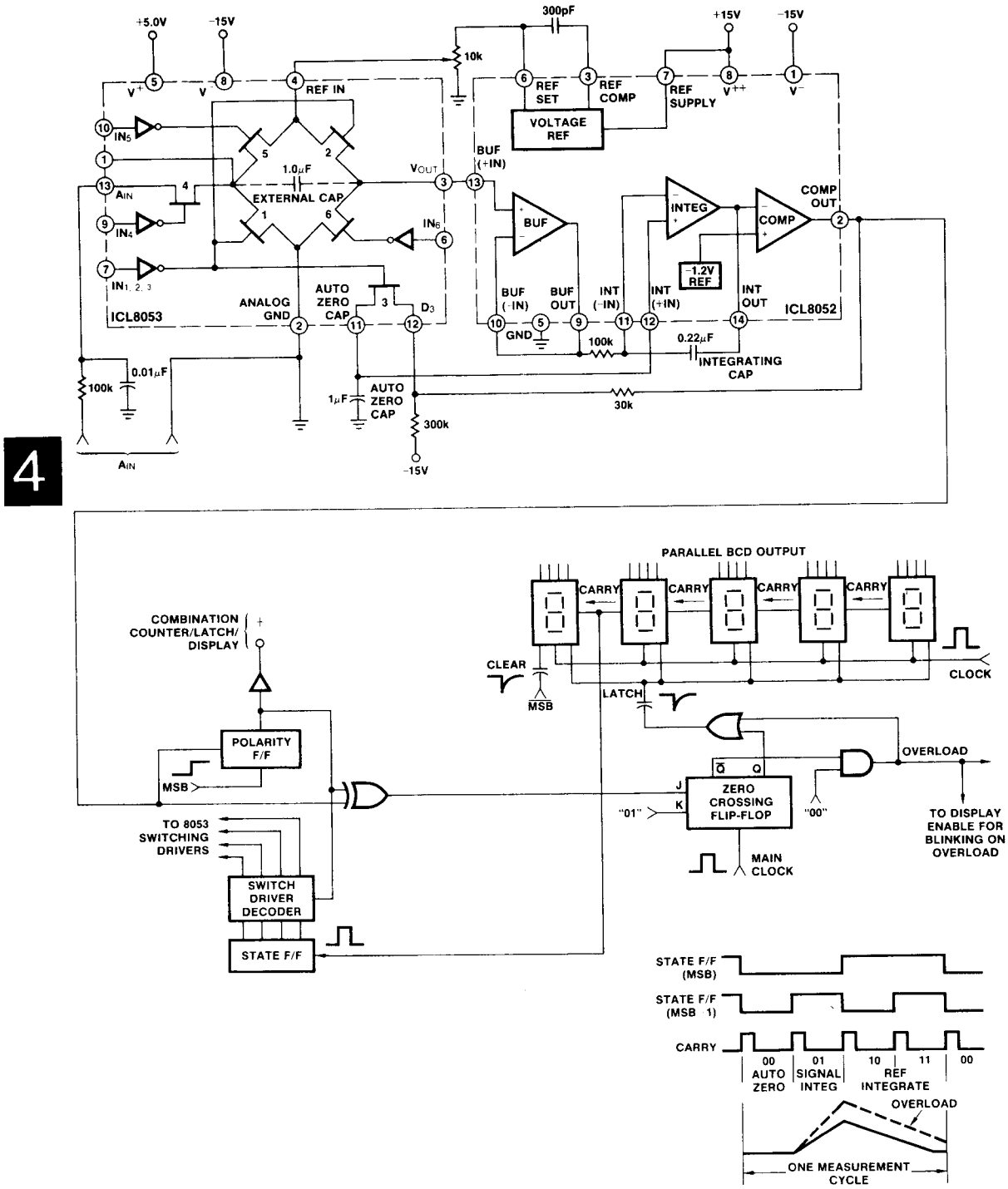

Figure 4: Functional Diagram for A/D Converter

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APPLICATIONS

Specific Circuits Using the ICL8052/8053

Figure 5 shows the complete circuit for a 4-1/2 digit (±2.000V full scale) A-D with LED readout and parallel BCD data lines. In addition to the ICL8052/8053, this circuit uses 6 low-cost CMOS packages for control and 5 TIL 306 as a combination LED readout, synchronous counter, and BCD latch. In this circuit, the clock runs continuously driving the 5 decade counters in the TIL 306's. The carry from the fourth decade is used to trigger the state F-F. Thus, each of the four states lasts for 10,000 counts. At the beginning of state 10, the 5th decade is cleared. None of the other counters need to be cleared since they automatically roll to 0000 at this point. When the zero-crossing F-F detects the end of the measurement, a latch pulse is initiated. The R-C time constant of this pulse is selected long enough (50nsec) to assure the latches turn on, but short enough (3μsec) to assure that the latches are decoupled before the next cloc pulse. Selecting a typical time constant of 400nsec assure proper latching with wide variance in component value.

In order to give a visual indication of overload, the LEI displays are blanked during state 00 if an overload exists. I overloaded, the instrument will blink a reading of 19999. A non-blinking reading 19999 is a valid reading for th instrument.

By tying the clear terminals of the state flip-flop and the fou decade counters to a common bus, the instrument can b synchronized to external events. If the bus is low, th instrument is held in auto-zero with the last measuremen cycle at the beginning of state 00. The data valid puls indicates the end of measurement cycle. For free-runnin condition, the bus is held high at +5 volts.

Generating a Family of A-D Converters

In figure 5, the lines marked (MSB) and (MSB-1) are connected to Q_B and Q_A of the 4-bit state flip-flop respectively. This forces a change in state for each carry pulse (10,000 counts) from the decade counters. If the lines were moved to Q_C and Q_B respectively, two carry pulses (20,000 counts) would be required to change states. Since full-scale is two states long, the max count now becomes 40,000; (actually 39,999). Similarly if Q_D and Q_C are used the max count is now 7,999 (one less decade counter would be used in this case). The ability to easily change max count (full scale) is most useful where the A-D converter is measuring physical constants such as temperature, distances, weight, etc. It allows designer to match the digital reading of the instrument to the analog range of the transducer. Since the analog input required to generate full scale output is $2V_{REF}$ in every case, an almost endless variety of scale factors can be generated easily from one basic design. Table I summarizes how the family of DVM's is generated.

Specific circuits demonstrating this principle are shown in figures 5 and 6. An 800.0mV full scale A-D can be obtained from the 2.0000V instrument shown in figure 5 with the three following modifications:

1. Delete middle LED counter.
2. State decode moved to Q_D and Q_C.
3. Reference voltage adjusted to 0.4000V.

Figure 6 is the specific circuit for a 16-bit binary A-D. Here the decade counters and displays have been replaced by synchronous 4-bit counters and latches. To give a full scal reading of ±3.2768 volts the reference is adjusted to 1.638 volts.

Figure 7 shows the circuit for a 40,000 count instrument. Thi circuit conforms to all of the "family" rules with the exceptio that it uses a −2.0000 volt reference. If a positive referenc was used, pin 3 of the 8053 would have to swing to +6V (+ volt input +2 volt reference). Since this exceeds the +5 vol supply, the switch would forward bias into the substrate. I can easily accommodate the +2 to −6 volt swing required of negative reference. A few changes are required when using negative reference. The drive to pin 6 (+Reference driver) an pin 10 (−Reference driver) must be interchanged, no connec tions are made to pins 3, 6 and 7 of the ICL8052, and the resis tor divider between COMP OUT to AZ switch must be adjusted

Full Scale	V_{REF}	Total Number Of Decade Counters	Connect MSB-1 to	Connect MSB to
±200.0mV	+.1000V	4	Q_A	Q_B
±2.000V	+1.000V	4	Q_A	Q_B
±400.0mV	+.2000V	4	Q_B	Q_C
±4.000V	−2.000V	4	Q_B	Q_C
±800.0mV	+.4000V	4	Q_C	Q_D
±2.0000V	+1.0000V	5	Q_A	Q_B
±4.0000V	−2.0000V	5	Q_B	Q_C
±3.2768V	+1.6384V	4*	Q_C	Q_D

*Number of 4-bit binary counters

Table I

Alternate Circuits

In a 4-1/2 digit (20,000 count) instrument where the family generating capabilities of the four bit counter is not required, a dual D flip-flop can be substituted for this function with some reduction in parts costs. Also a "±1" LED, driven by a dual D flip-flop, can replace the fifth TIL306. Figure 8 shows a circuit with these two substitutions made.

If the Parallel BCD capabilities of the TIL306 are not required, a further reduction in parts cost can be achieved by using the circuit of figure 9. In this circuit the MM74C926 performs the counting, latch and 7 segment decode function of the TIL306 such that it can be used with any LED displays. Some modification of the clock and latch circuit is required since the 74C926 uses a ripple counter with a carry at 0000 instead of a synchronous carry at 9999. When a zero-crossing signal is detected and the latch-enable is initiated, a signal is simultaneously fed to the clock drive circuitry to delay the clock and therefore the count until the previous count can be latched. The latch time-constant is shorter than the clock-delay time-constant to assure that the latch is transferred and disabled before the clock resumes clocking. A 1μs time delay in the output of the clock driver assures that the slight delay (100ns) between the clock pulse and the clock-delay pulse does not clock the counter. Blanking is provided to give a visual indication of overload. However, the display will flash .0000 instead of 1.9999 due to the nature of the ripple counter.

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Component Selection

Except for the Reference Voltage, none of the component values are first-order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance the reference capacitor and auto-zero capacitor are each shown as 1.0μF. These relative large values are selected to give greater immunity to PC board leakage since much smaller capacitors are adequate for charge injection errors or leakage errors from the ICL8052/8053. The ratio of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at ±14 volts) due to tolerance build-up between the resistor, capacitor a and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again the .22 value for integrating cap is selected for PC considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating cap is low dielectric absorption. A polypropylene cap (made by TRW) gave excellent results in the application. In fact a good test for dielectric absorption is to test the subject cap in this circuit with the input tied to reference. This ratiometric condition should read 1.0000 and any deviation is probably due to dielectric absorption. In this test poly-carbonate caps typically read .9992, polystyrene, .9997 and polypropylene, 1.0000. The increased temperature coefficient of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

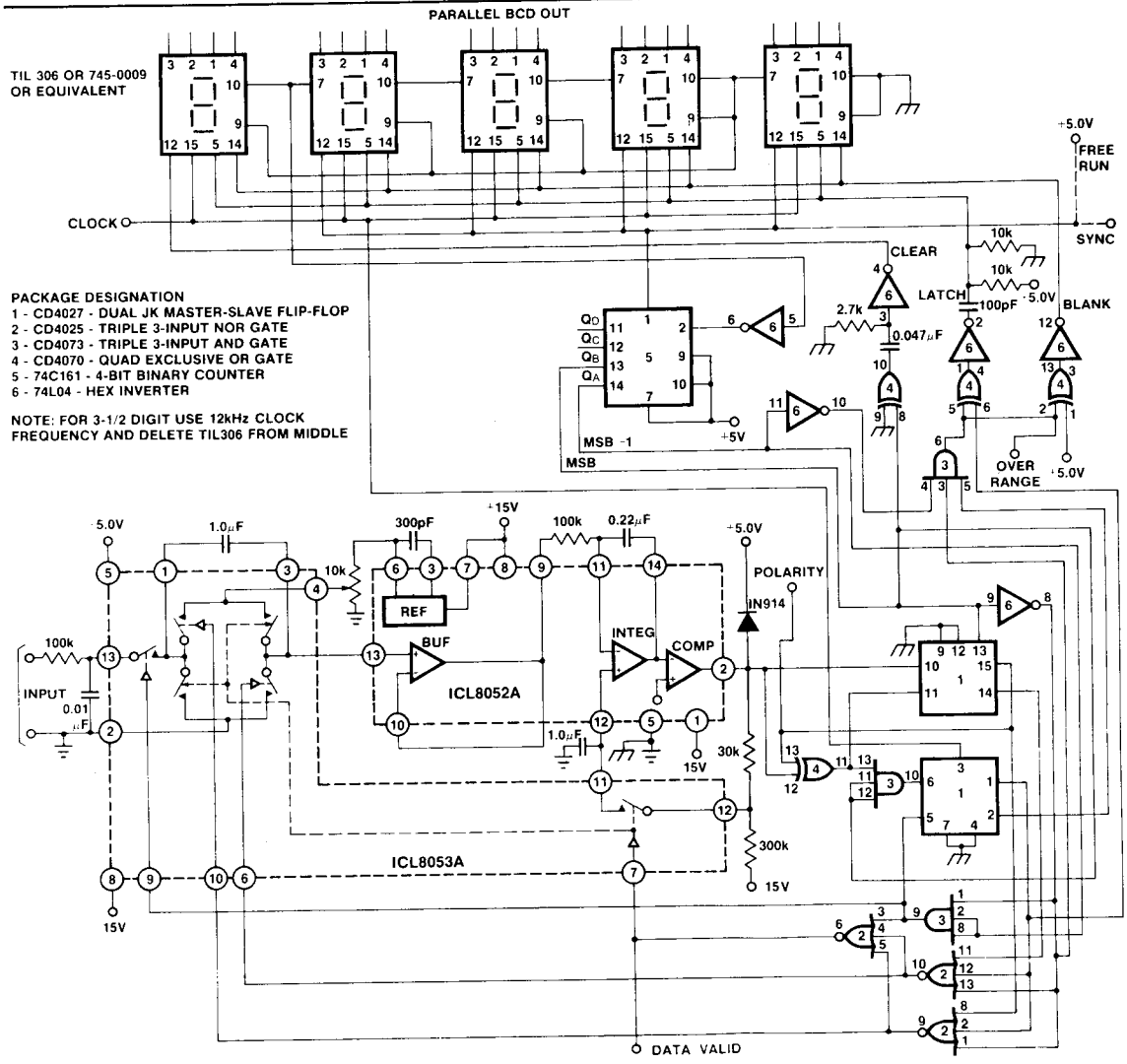

Figure 5: General Circuit for a Family of DVM's.

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The output of the comparator is clamped to the +5 volts supply to prevent the positive swing of the comparator from forward biasing the auto-zero switch to its substrate and injecting minority carriers that would be collected as leakage currents. In addition, a voltage translation network connects the output of the comparator to the auto-zero switch. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the CMOS logic (+2.5V) while the auto-zero cap is being charged to V_{REF} (+1V in the case of 2.0000 instrument). Otherwise even with zero signal in, some reference integrate period would be required to drive the comparator output to the threshold region. This would show up as an equivalent offset error. Once the divider chain has been selected, the unit-to-unit variation should contribute less than a few tenths-of-a-count error in the worse case (40,000 count instrument) and proportionately less in other instruments. For a 3-1/2 digit instrument, the error is unmeasurable.

Finally, the back-to-back diodes are used to lower noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At start-up or recovery from an overload, their impedance is low to large signals so the cap can be charged in one auto-zero cycle.

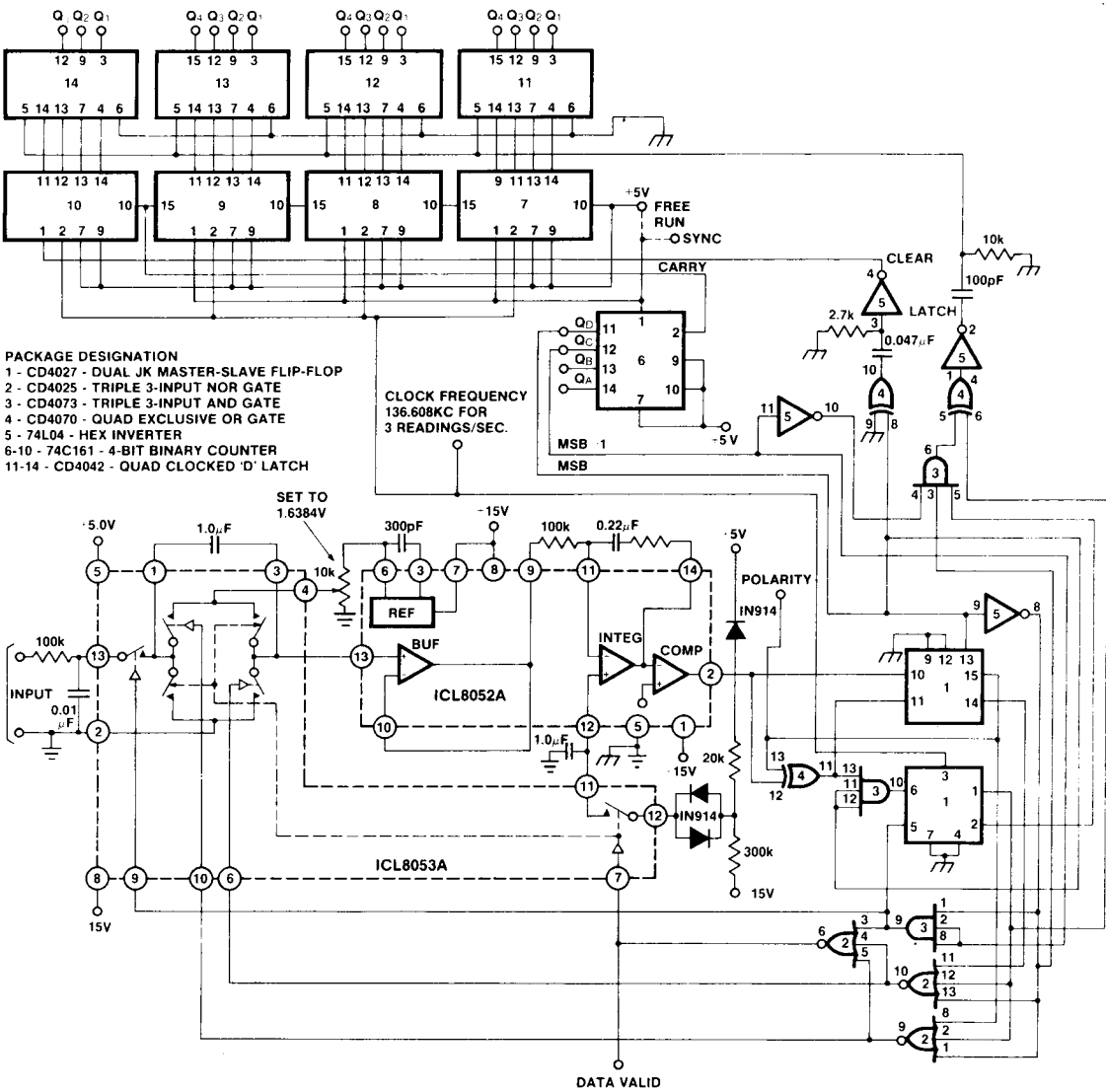

Figure 6: 16-Bit Binary Converter

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Max Clock Frequency

The maximum conversion rate of most dual-slope A-D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open-loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μs delay. At a clock frequency of 160kHz (6μs period) half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash "1" on noise peaks even when the input is shorted.

Some circuits use positive feedback or a latch to solve the delay problem. However, unless the comparator voltage swing, the comparator gain, and the integrator gain are carefully controlled, this circuit can generate *anticipation* errors that greatly exceed the 3μs *delay* error. Also it is very susceptible to noise spikes. A more controlled approach for extending the conversion rate is the use of a small resistor in the integrator feedback loop. This feeds a small pulse to the comparator to get it moving quickly, and partially compensate for its delay.

The minimum clock frequency is established by leakage on the auto-zero and reference cap. With most devices, measurement cycles as long as 10 seconds gave no measurable leakage error.

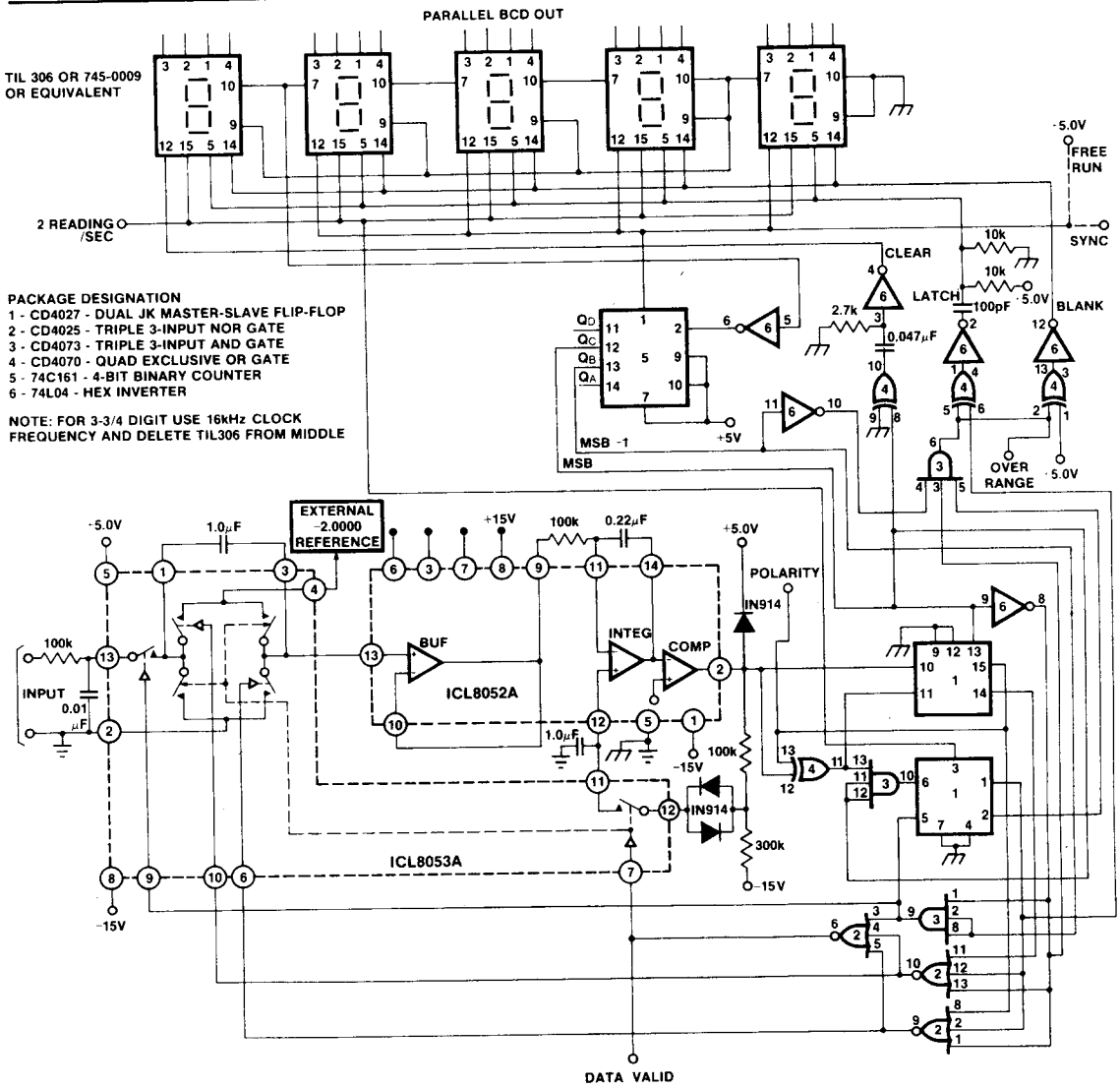

Figure 7: 4-3/4 Digit DVM

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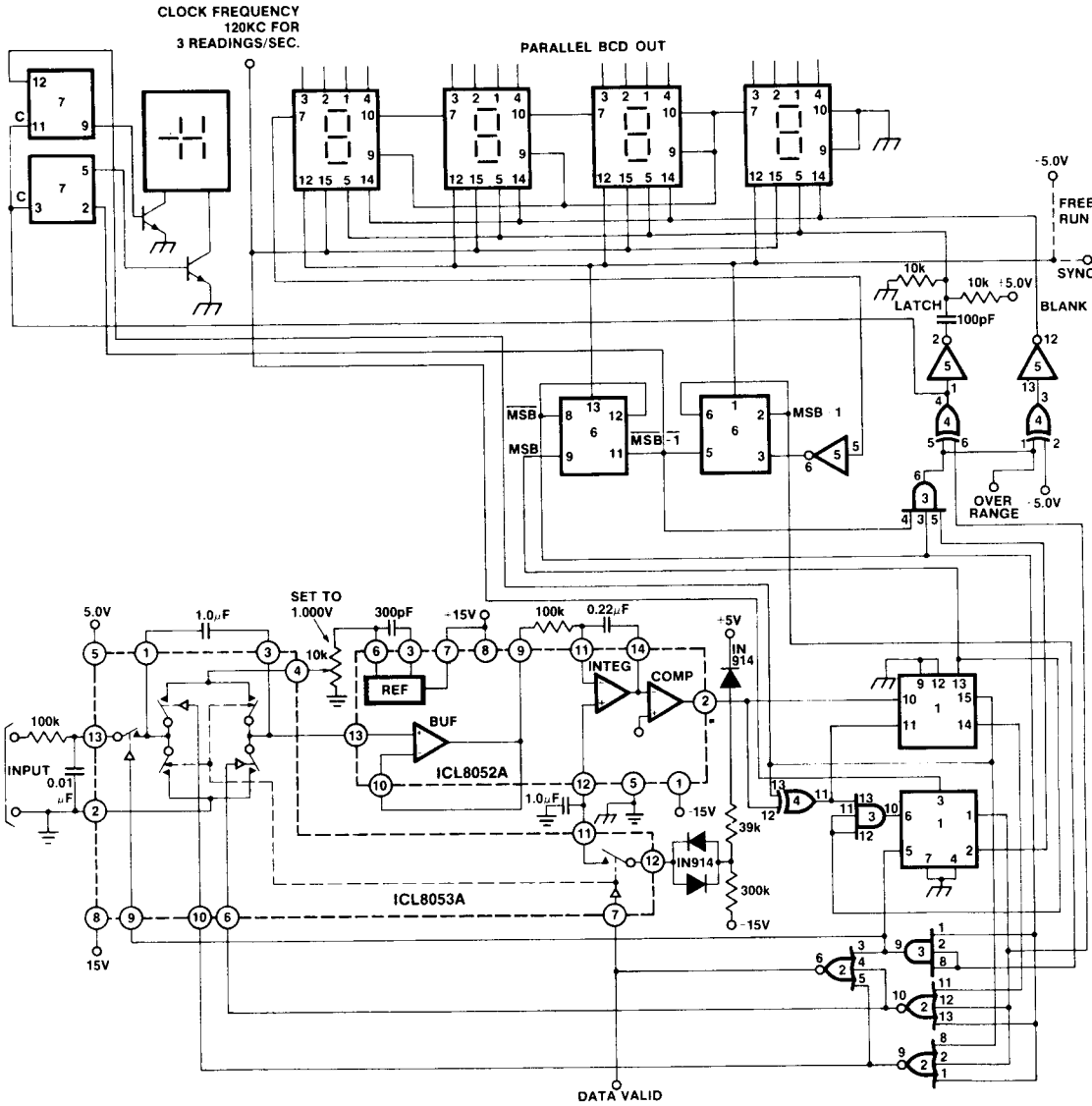

PACKAGE DESIGNATION
1 - CD4027 - DUAL JK MASTER-SLAVE FLIP-FLOP
2 - CD4025 - TRIPLE 3-INPUT NOR GATE
3 - CD4073 - TRIPLE 3-INPUT AND GATE
4 - CD4070 - QUAD EXCLUSIVE OR GATE
5 - 74L04 - HEX INVERTER
6 - 74L74 - DUAL 'D' FLIP-FLOP
7 - 74L74 - DUAL 'D' FLIP-FLOP

NOTE: FOR 3-1/2 DIGIT USE 1/10 CLOCK FREQUENCY AND DELETE TIL306 FROM MIDDLE.

Figure 8: 4-1/2 Digit DVM (Parallel BCD)

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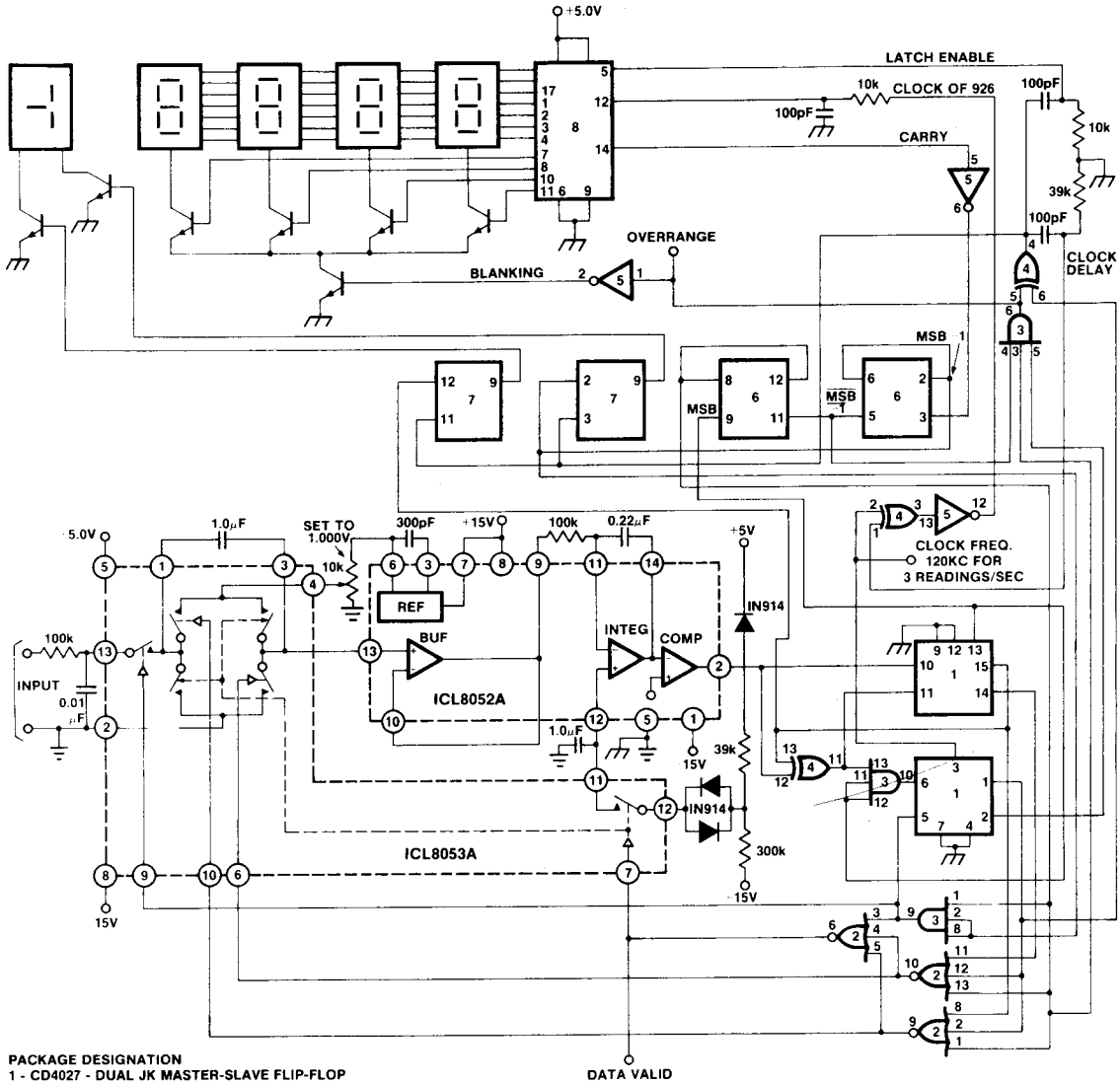

PACKAGE DESIGNATION
1 - CD4027 - DUAL JK MASTER-SLAVE FLIP-FLOP
2 - CD4025 - TRIPLE 3-INPUT NOR GATE
3 - CD4073 - TRIPLE 3-INPUT AND GATE
4 - CD4070 - QUAD EXCLUSIVE OR GATE
5 - 74L04 - HEX INVERTER
6 - 74L74 - DUAL 'D' FLIP-FLOP
7 - 74L74 - DUAL 'D' FLIP-FLOP
8 - MM74C926 - 4 DIGIT COUNTER WITH MULTIPLEXED 7-SEGMENT OUTPUT DRIVERS

NOTE: FOR 3-1/2 DIGIT USE SAME CLOCK FREQUENCY AND DELETE LEAST SIGNIFICANT LED.

Figure 9: 4-1/2 Digit DVM (20,000 Count Multiplexed Display)

ICL8052 vs. ICL8068

An alternative to the 8052 is the 8068.

While the ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances, the ICL8068 has substantially lower noise voltage and will give better performance in systems where noise is a limiting factor, such as low signal level conditions. Specifications may be found in the ICL8068/ICL8052/ICL71C03 and ICL8068/ICL8052/ICL7104 data sheets.