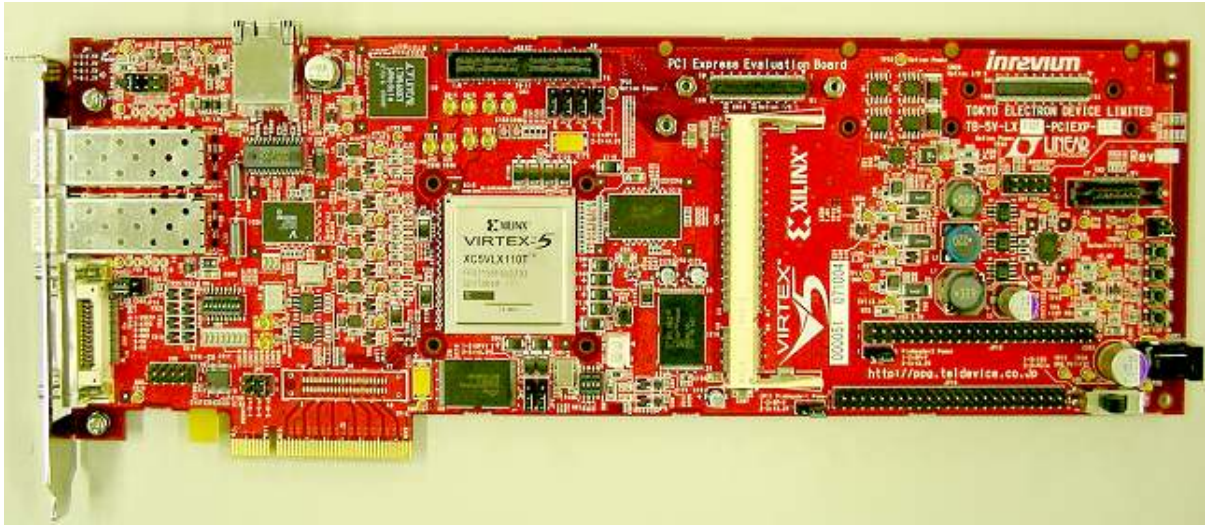

TB-5V-LX50T/110T/SX50T/FX70T-PCIEXP

User's Manual

Rev. 2.02

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Precautions

- Product and information contained in this manual is subject to change without prior notice for improvement.
- Every possible effort has been made to avoid any errors in this document. Should an error or other problems be found, please do not hesitate to contact us.
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- Tokyo Electron Device Limited shall not be liable for any consequences or damages resulting from the uses that are not described in this document.
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- This board has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.
- Repair of the board is carried out by replacing it on a chargeable basis; not repairing the faulty devices.
- Replacement of initial faults carried out by free of charge, however, it is required for the customer to inform us of relevant problem within two weeks after delivery.

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1. Introduction

This document describes the PCI Express Evaluation Board with a high-speed serial transceiver interface "**TB-5V-LX50T/110T/SX50T/FX70T-PCIEXP**".

2. Accessory

- 12V 5A AC adapter
- Screw x 8, Spacer x 4

3. Feature

1. FPGA (Xilinx's XC5VLX50T/110T-1FF1136 or XC5VSX50T-1FF1136 or XC5VFX70T-1FF1136)
2. Xilinx's Virtex-5 series PCI Express (x8) for interfacing with a PC
3. DDR2-SDRAM (on Board) x 1
4. DDR2 SO-DIMM connector x 1
5. 10/100/1000Mbps Ethernet MAC & PHY
6. 4ch high-speed serial transceiver interface
   - SFP optical module port (2ch)
   - MMCX connector port (2ch)
7. Power-switching standalone application

4. Safety Precautions

Before using this board, read these safety precautions carefully to assure correct use.
Failure to do so will damage this board or result in fire or personal injury.
This board is designed and manufactured on the assumption that it is used by personnel who have adequate knowledge and experience regarding electronic circuits.
If the board is used by personnel who do not have such knowledge or experience, be sure to use it under proper supervision.

- Do not use this board for improper purposes.
  This board is designed for use in a generic indoor environment. Do not use it in areas exposed to condensation, metal powder or corrosive, flammable or explosive gases.
- Connecting ICs/LSIs or cables in reverse orientation could damage them or this board. Before connecting them, be sure to check for proper orientation. Do not install or connect/disconnect them with the power switch kept ON or without electrostatic protection.
- Do not connect a device to the PCI slot on the motherboard with the power switch kept ON or without electrostatic protection.
  Do not place this board on the conductor such as steel plate or conductive sponge, otherwise onboard ICs/LSIs could be damaged. Before turning power switch on, be sure to check carefully if there are no flammable dusts or conductive material such as wire chips on the board.
  This board allows two power supply channels, one from the PCI slot and the other from the external power connector. This can be selected by setting onboard jumper pins. Before turning the power switch on, be sure to check if they are correctly set.
- Observe rated supply voltage requirement and be careful about voltage polarity.
- Tokyo Electron Device Limited assumes no responsibility or liability for any losses or damages caused by modification of this board or design/implementation of a sub-board.
- Do not place this board in areas exposed to shock or vibration.
- Be careful about fire since the onboard FPGA, CHIP, DIMM and power regulator can generate heat.
- Be careful when inserting a memory device into the onboard DIMM socket. (Number of connecting/disconnecting to or from the DIMM socket is limited to 25).

5. Board Overview

Board size: 310.0 x 111.15 x 1.6[mm] (Not in compliance with PCI-Express standard)
Board thickness is not included parts width. The board might interfere in PCI Express slot, Please be careful for space with the neighboring PCI Express card.

5-1 External View

- TB-5V-LX110T-PCIEXP

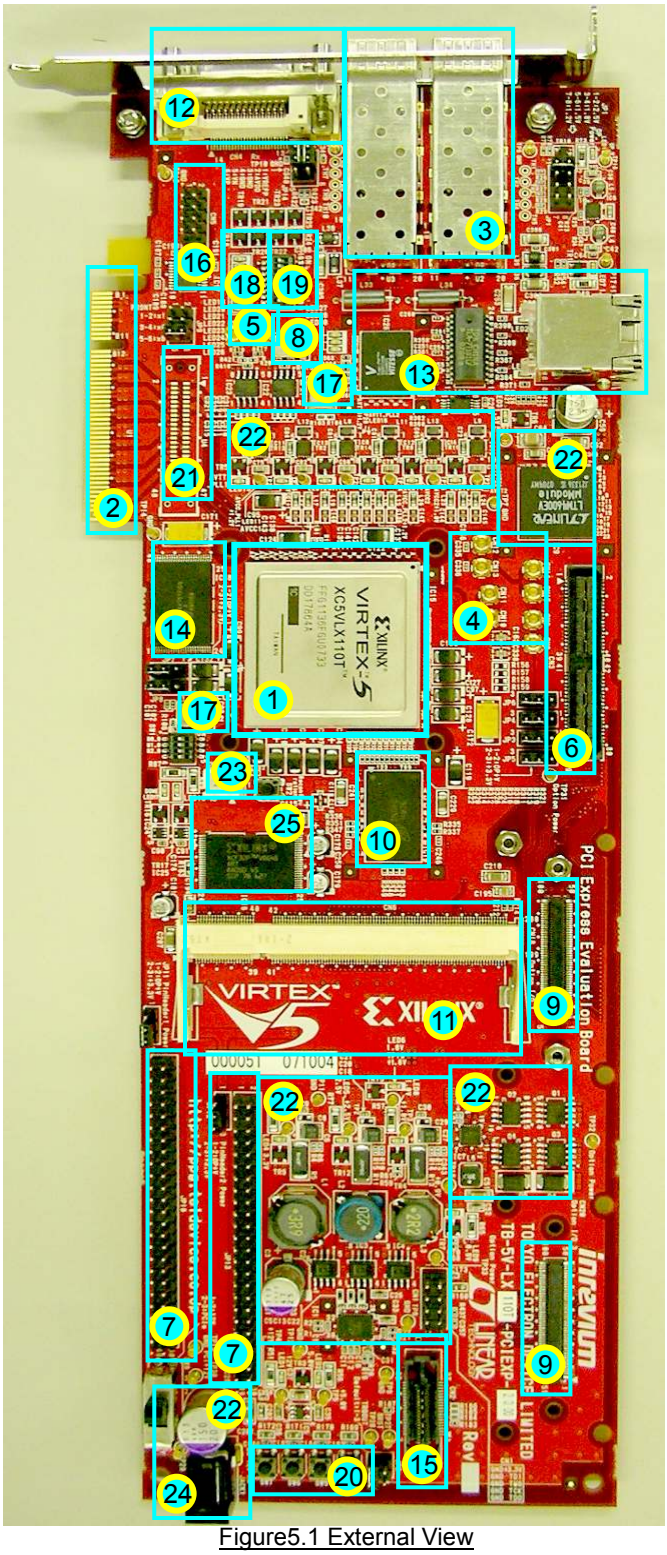


Figure5.1 External View

5-2 Block Diagram

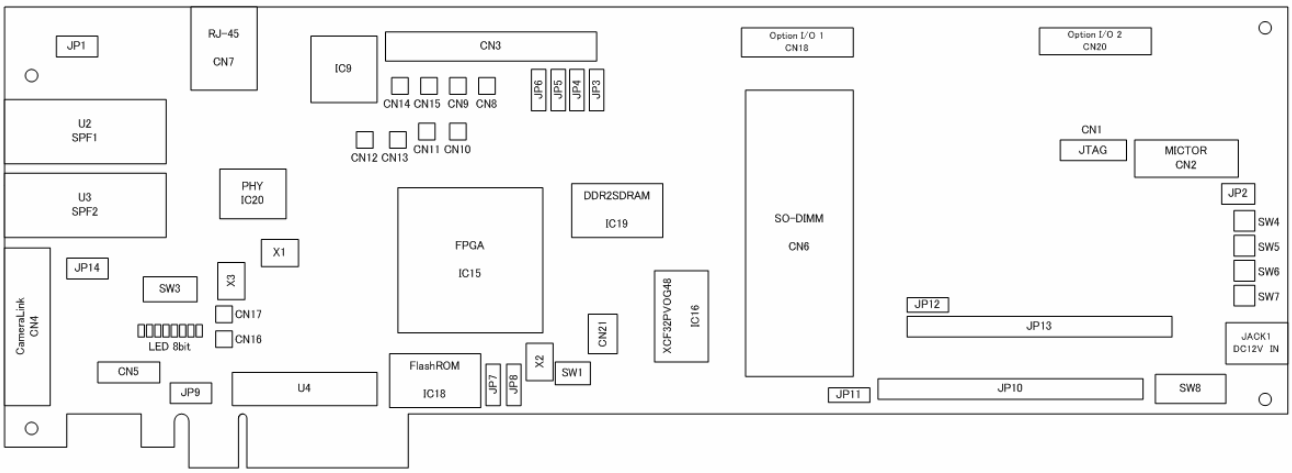
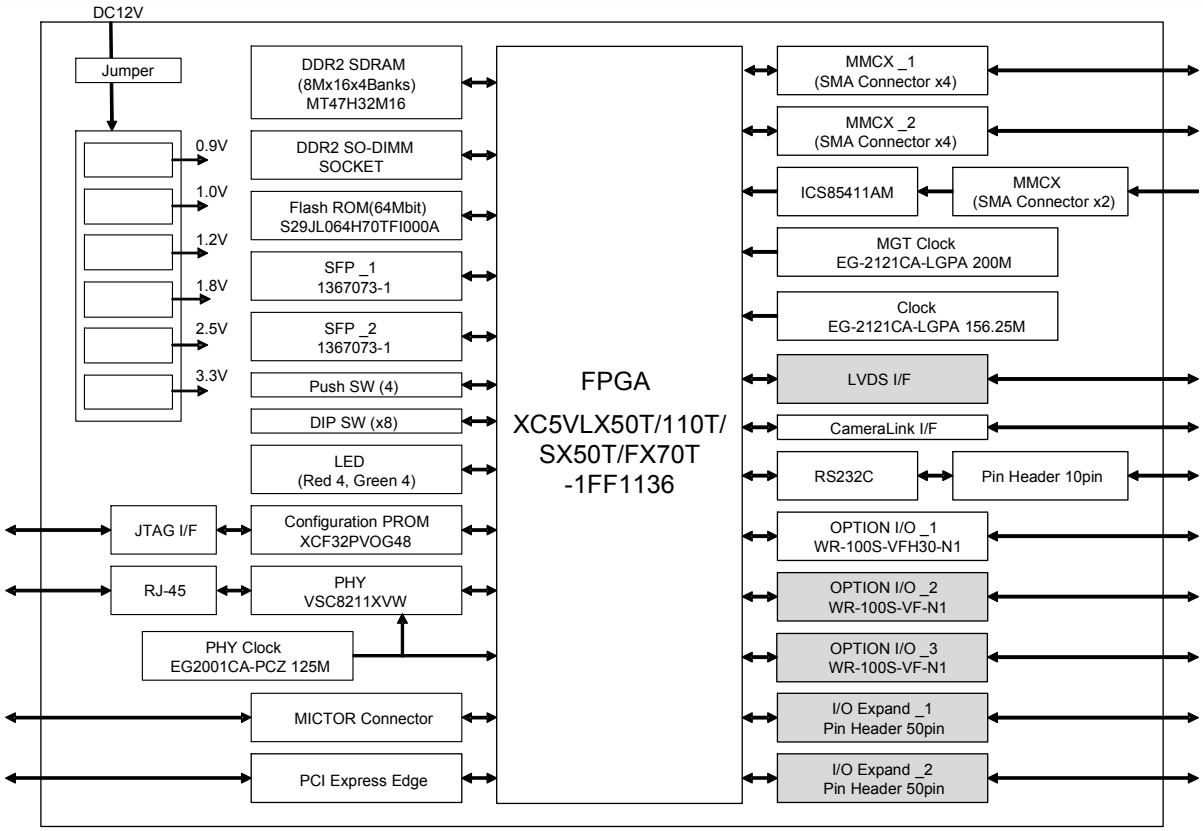


Figure5.2 Board Configuration Diagram



NOTE : Gray Block is available for TB-5V-LX110T/FX70T-PCIEXP only.

Figure5.3 Functional Block Diagram

5-3 Main Components and Functions

5-3-1 XC5VLX50T/110T-1FF1136 , XC5VSX50T-1FF1136 and XC5VFX70T-1FF1136 ①

- Provides interfacing with the PCI Express edge using Xilinx Virtex5LXT/SXT/FXT's PCI Express Block function.
- Provides a high-speed serial transceiver interface to connect the SFP optical module port, MMCX connector port and Option connector .
- Provides connection to the DDR2-SDRAM Chip with 16 data bits and 15 address (including BANK address) bits, Can be possible DDR (Double Data Rate) 400Mbps data transfer.
- Provides connection to the DDR2-SO-DIMM with 64 data bits and 19 address (including BANK address) bits, Can be possible DDR (Double Data Rate) 400Mbps data transfer.

For information about FPGA configuration, refer to Section 7.
- Configuration is implemented using the XCF32PVO48 in Master Parallel Mode.
- The JTAG chain is connected to the XCF32PVO48 and the FPGA.

5-3-2 PCI Express Edge ②

- "x8"(8Lane) connection is allowed.
- Some signals have the P/N polarity of FPGA's high-speed I/O "GTP" and the "PCI Express edge" connected reversely. Because that is easy to keep signal quality and a function to automatically reverse the polarity at the GTP's receiving end is used. Use the LogiCORE PCIExpress Block Plus. Refer to Figure 5.4.

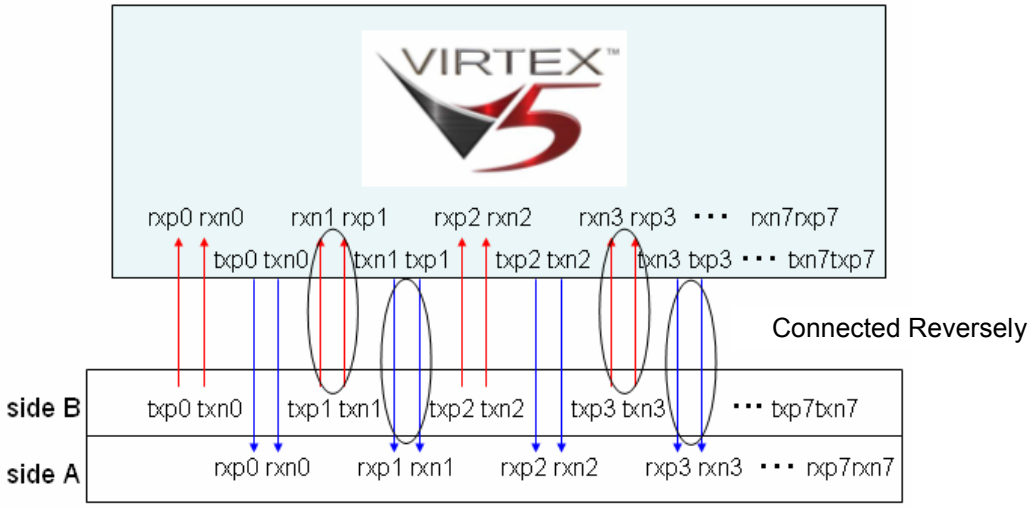


Figure5.4 GTP Signal Connection

Table 5.1 PCI Express GTP Connections

Reference	PCI-Express Edge	FPGA Pin (Pin #)	GTP Tile	GTP Location	
				LX50T or SX50T	LX110T or FX70T
U1	PETp0	RXP(N1)	112	GTP_DUAL_X0Y3	GTP_DUAL_X0Y4
	PETn0	RXN(P1)			
	PERp0	TXP(M2)			
	PERn0	TXN(N2)			
	PETp1	RXN(R1)	112	GTP_DUAL_X0Y3	GTP_DUAL_X0Y4
	PETn1	RXP(T1)			
	PERp1	TXN(T2)			
	PERn1	TXP(U2)			
	PETp2	RXP(W1)	114	GTP_DUAL_X0Y2	GTP_DUAL_X0Y3
	PETn2	RXN(Y1)			
	PERp2	TXP(V2)			
	PERn2	TXN(W2)			
	PETp3	RXN(AA1)	114	GTP_DUAL_X0Y2	GTP_DUAL_X0Y3
	PETn3	RXP(AB1)			
	PERp3	TXN(AB2)			
	PERn3	TXP(AC2)			
	PETp4	RXP(AE1)	118	GTP_DUAL_X0Y1	GTP_DUAL_X0Y2
	PETn4	RXN(AF1)			
	PERp4	TXP(AD2)			
	PERn4	TXN(AE2)			
	PETp5	RXN(AG1)	118	GTP_DUAL_X0Y1	GTP_DUAL_X0Y2
	PETn5	RXP(AH1)			
	PERp5	TXN(AH2)			
	PERn5	TXP(AJ2)			
	PETp6	RXP(AL1)	122	GTP_DUAL_X0Y0	GTP_DUAL_X0Y1
	PETn6	RXN(AM1)			
	PERp6	TXP(AK2)			
	PERn6	TXN(AL2)			
	PETp7	RXN(AP2)	122	GTP_DUAL_X0Y0	GTP_DUAL_X0Y1
	PETn7	RXP(AP3)			
	PERp7	TXN(AN3)			
	PERn7	TXP(AN4)			

* Some signals have the P/N polarity of FPGA's GTP and PCI Express's RX,TX reversely connected on the board. Thus, it is needed to configure the FPGA appropriately.

Table 5.2 PCI Express Edge Terminal Connections (1/2)

A Side	Signal	Pin	B Side	Signal	pin
A1	PCIE_PRSNT1_B	PCIE_PRSNT_B	B1	+12 VOLTS	12V
A2	+12 VOLTS	12V	B2	+12 VOLTS	12V
A3	+12 VOLTS	12V	B3	+12 VOLTS	12V
A4	JTAG_TCK	-	B4	GND	GND
A5	JTAG_TDI	-	B5	SMCLK(2)	-
A6	JTAG_TDI	-	B6	SMDAT(2)	-
A7	JTAG_TDO	-	B7	GND	GND

Table 5.2 PCI Express Edge Terminal Connections (2/2)

A Side	Signal	pin	B Side	Signal	pin
A8	JTAG_TMS	-	B8	3.3 VOLTS	3.3V
A9	+3.3 VOLTS	3.3V	B9	JTAG_TRST_B	-
A10	+3.3 VOLTS	3.3V	B10	3.3 VOLTSAUX	-
A11	PCIE_PERST	AE14	B11	PCIE_WAKE_B	-
A12	GND	GND	B12	RESERVED	-
A13	PCIE_REFCLKP	Y4	B13	GND	GND
A14	PCIE_REFCLKN	Y3	B14	PETP0(4)	RXP(N1)
A15	GND	GND	B15	PETN0(4)	RXN(P1)
A16	PERP0	TXP(M2)	B16	GND	GND
A17	PERN0	TXN(N2)	B17	PCIE_PRSNT2_B	PCIE_PRSNT_x1
A18	GND	GND	B18	GND	GND
A19	RESERVED	-	B19	PETP1	RXN(R1)
A20	GND	GND	B20	PETN1	RXP(T1)
A21	PERP1	TXN(T2)	B21	GND	GND
A22	PERN1	TXP(U2)	B22	GND	GND
A23	GND	GND	B23	PETP2	RXP(W1)
A24	GND	GND	B24	PETN2	RXN(Y1)
A25	PERP2	TXP(V2)	B25	GND	GND
A26	PERN2	TXN(W2)	B26	GND	GND
A27	GND	GND	B27	PETP3	RXN(AA1)
A28	GND	GND	B28	PETN3	RXP(AB1)
A29	PERP3	TXN(AB2)	B29	GND	GND
A30	PERN3	TXP(AC2)	B30	RESERVED	-
A31	GND	GND	B31	PCIE_PRSNT2_B	PCIE_PRSNT_x4
A32	RESERVED	-	B32	GND	GND
A33	RESERVED	-	B33	PETP4	RXP(AE1)
A34	GND	GND	B34	PETN4	RXN(AF1)
A35	PERP4	TXP(AD2)	B35	GND	GND
A36	PERN4	TXN(AE2)	B36	GND	GND
A37	GND	GND	B37	PETP5	RXN(AG1)
A38	GND	GND	B38	PETN5	RXP(AH1)
A39	PERP5	TXN(AH2)	B39	GND	GND
A40	PERN5	TXP(AJ2)	B40	GND	GND
A41	GND	GND	B41	PETP6	RXP(AL1)
A42	GND	GND	B42	PETN6	RXN(AM1)
A43	PERP6	TXP(AK2)	B43	GND	GND
A44	PERN6	TXN(AL2)	B44	GND	GND
A45	GND	GND	B45	PETP7	RXN(AP2)
A46	GND	GND	B46	PETN7	RXP(AP3)
A47	PERP7	TXN(AN3)	B47	GND	GND
A48	PERN7	TXP(AN4)	B48	PCIE_PRSNT2_B	PCIE_PRSNT_x8
A49	GND	GND	B49	GND	GND

5-3-3 SFP Optical Module Port ③

- The SFP optical module is supported.

The control signals to be connected to the SFP optical module is connected to the onboard through-hole (Φ0.8).

Table 5.3 Allocation of SFP Optical Module Pins

Connector Pin #	Pin Name	Connected to	Connector Pin #	Pin Name	Connected to
1	GND		10	GND	
2	TX_FAULT	Through-hole	11	GND	
3	GND		12	RD-	FPGA
4	MOD_DEF2	Through-hole	13	RD+	FPGA
5	MOD_DEF1	Through-hole	14	GND	
6	MOD_DEF0	Through-hole	15	3.3V	
7	NC		16	3.3V	
8	RX_LOS	Through-hole	17	GND	
9	GND		18	TD+	FPGA
10	GND		19	TD-	FPGA

* A loopback evaluation test has been performed using AVAGO's AFBR-57R5APZ optical module. [MAX:3.125Gbps]

Table 5.4 Allocation of SFP Optical Module and FPGA Pins

Reference	Pin Name (FPGA/SFP)	FPGA Pin #	GTP Tile
U2	TXP/TD-	F2	116
	TXN/TD+	G2	
	RXP/RD+	G1	
	RXN/RD-	H1	
U3	TXP/TD-	L2	116
	TXN/TD+	K2	
	RXP/RD+	K1	
	RXN/RD-	J1	

5-3-4 MMCX Connector Port 4

- MMCX connector: Samtec's MMCX-J-P-H-ST-TH1

Table 5.5 MMCX Connector and FPGA Pin Connection

Reference	Signal Name	FPGA Pin #	GTP Tile
CN8	SMA_RXP1	A3	120
CN9	SMA_RXN1	A2	
CN10	SMA_TXP1	B4	
CN11	SMA_TXN1	B3	
CN12	SMA_RXP2	D1	120
CN13	SMA_RXN2	C1	
CN14	SMA_TXP2	E2	
CN15	SMA_TXN2	D2	

5-3-5 MMCX Connector Port for Clock Input 5

- MMCX connector: Samtec's MMCX-J-P-H-ST-TH1
- The clock signals input from the MMCX connector are divided into two channels using the onboard IDT's ICS85411 and supplied to FPGA's GTP clock pins.

Table 5.6 MMCX Connector for Input Clock and FPGA Pin Connection

Reference	Signal Name	FPGA Pin #	GTP Tile
CN16	SMA_MGT_CLKP1	H4	116
	SMA_MGT_CLKN1	H3	
CN17	SMA_MGT_CLKP2	AL7	126
	SMA_MGT_CLKN2	AM7	

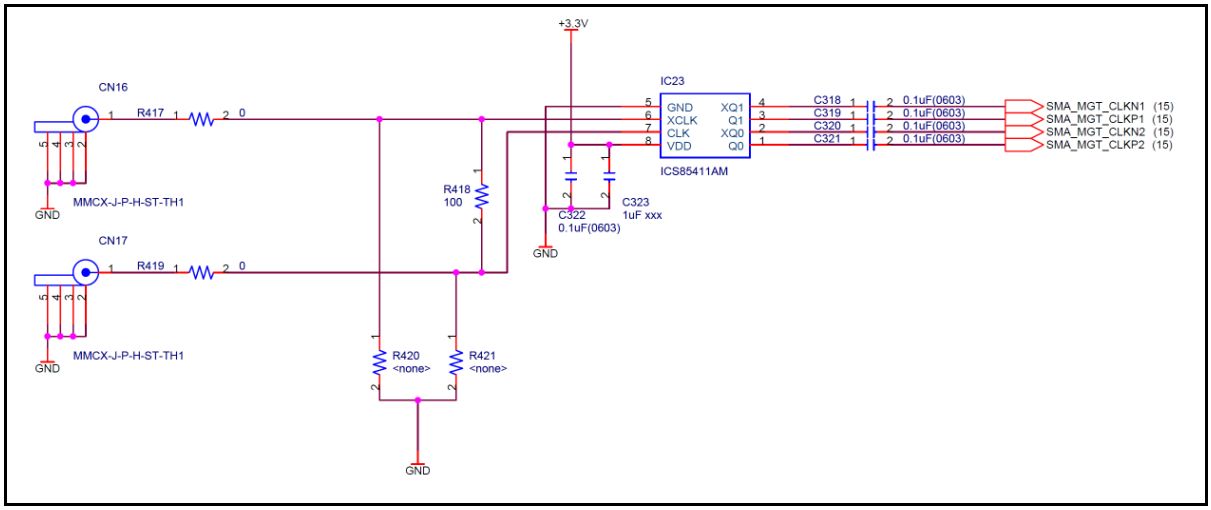


Figure 5.5 Signal Conversion Circuit for the MMCX Connector for Clock Input

5-3-6 High-Speed Serial Interface (GTP) 6

- GTP connector for channel 4 : Samtec's QSE-028-01-F-D-DP-A
- **Used for TB-5V-LX110T/FX70T-PCIEXP only**

Table 5.7 LVDS I/F Connector and FPGA Pin Connection

Connector Pin #	Pin Name		FPGA Pin #	GTP Tile	GTP Tile
1	LVDST0P	<-- connect -->	B5	MGTTXP1_124	124
2	LVDSR0P	<-- connect -->	A6	MGTRXP1_124	
3	LVDST0N	<-- connect -->	B6	MGTTXN1_124	
4	LVDSR0N	<-- connect -->	A7	MGTRXN1_124	
5	GND				
6	GND				
7	LVDST1N	<-- connect -->	B9	MGTTXN0_124	124
8	LVDSR1N	<-- connect -->	A8	MGTRXN0_124	
9	LVDST1P	<-- connect -->	B10	MGTTXP0_124	
10	LVDSR1P	<-- connect -->	A9	MGTRXP0_124	
11	GND				
12	GND				
13	LVDST2P	<-- connect -->	AN5	MGTTXP0_126	126
14	LVDSR2P	<-- connect -->	AP6	MGTRXP0_126	
15	LVDST2N	<-- connect -->	AN6	MGTTXN0_126	
16	LVDSR2N	<-- connect -->	AP7	MGTRXN0_126	
17	GND				
18	GND				
19	LVDST3N	<-- connect -->	AN9	MGTTXN1_126	126
20	LVDSR3N	<-- connect -->	AP8	MGTRXN1_126	
21	LVDST3P	<-- connect -->	AN10	MGTTXP1_126	
22	LVDSR3P	<-- connect -->	AP9	MGTRXP1_126	
23～80	GND				

5-3-7 User Pin Header 7

The board provides two 40-bit I/O pin headers for waveform monitoring by an oscilloscope and signal connection to an external board. **It is applied to only TB-5V-LX110T/FX70T-PCIEXP.**

Table 5.8 Pin Header (JP10) and FPGA Pin Connection (1/2)

Connector Pin #	Pin Name		FPGA Pin #	Pin Description
1	VCC_PH			
2	VCC_PH			
3	GND			
4	GND			
5	PH1_0	<-- connect -->	AK12	IO_L1P_6
6	PH1_1	<-- connect -->	AJ12	IO_L1N_6
7	GND			
8	GND			
9	PH1_2	<-- connect -->	AK13	IO_L3N_6
10	PH1_3	<-- connect -->	AL13	IO_L3P_6
11	PH1_4	<-- connect -->	AJ14	IO_L5P_6
12	PH1_5	<-- connect -->	AJ15	IO_L9N_CC_6
13	PH1_6	<-- connect -->	AL14	IO_L7N_6
14	PH1_7	<-- connect -->	AK14	IO_L5N_6
15	PH1_8	<-- connect -->	AL15	IO_L7P_6
16	PH1_9	<-- connect -->	AL16	IO_L10N_CC_6
17	PH1_10	<-- connect -->	AK16	IO_L10P_CC_6
18	PH1_11	<-- connect -->	AJ16	IO_L9P_CC_6
19	PH1_12	<-- connect -->	AK17	IO_L12P_VRN_6
20	PH1_13	<-- connect -->	AJ17	IO_L12N_VRP_6
21	PH1_14	<-- connect -->	AL18	IO_L14N_VREF_6
22	PH1_15	<-- connect -->	AK18	IO_L14P_6
23	PH1_16	<-- connect -->	AM15	IO_L16P_6
24	PH1_17	<-- connect -->	AP15	IO_L18N_6
25	PH1_18	<-- connect -->	AN15	IO_L18P_6
26	PH1_19	<-- connect -->	AP16	IO_L17P_6
27	PH1_20	<-- connect -->	AM16	IO_L16N_6
28	PH1_21	<-- connect -->	AP17	IO_L17N_6
29	PH1_22	<-- connect -->	AN17	IO_L19N_6
30	PH1_23	<-- connect -->	AM17	IO_L19P_6
31	PH1_24	<-- connect -->	AK19	IO_L15N_6
32	PH1_25	<-- connect -->	AL19	IO_L13P_6
33	PH1_26	<-- connect -->	AJ19	IO_L15P_6
34	PH1_27	<-- connect -->	AJ20	IO_L8N_CC_6
35	PH1_28	<-- connect -->	AL20	IO_L13N_6
36	PH1_29	<-- connect -->	AL21	IO_L11P_CC_6
37	PH1_30	<-- connect -->	AK21	IO_L11N_CC_6
38	PH1_31	<-- connect -->	AJ21	IO_L8P_CC_6
39	PH1_32	<-- connect -->	AK22	IO_L6N_6
40	PH1_33	<-- connect -->	AJ22	IO_L2N_6
41	PH1_34	<-- connect -->	AL23	IO_L4N_VREF_6
42	PH1_35	<-- connect -->	AK23	IO_L6P_6
43	PH1_36	<-- connect -->	AK24	IO_L4P_6
44	PH1_37	<-- connect -->	AJ24	IO_L0N_6

Table 5.8 Pin Header (JP10) and FPGA Pin Connection (2/2)

Connector Pin #	Pin Name		FPGA Pin #	Pin Description
45	PH1_38	<-- connect -->	AH23	IO_L2P_6
46	PH1_39	<-- connect -->	AH24	IO_L0P_6
47	GND			
48	GND			
49	VCC_PH			
50	VCC_PH			

Table 5.9 Pin Header (JP13) and FPGA Pin Connection (1/2)

Connector Pin #	Pin Name		FPGA Pin #	Pin Description
1	VCC_PH			
2	VCC_PH			
3	GND			
4	GND			
5	PH2_0	<-- connect -->	AN24	IO_L12P_VRN_25
6	PH2_1	<-- connect -->	AP24	IO_L12N_VRP_25
7	GND			
8	GND			
9	PH2_2	<-- connect -->	AM23	IO_L14N_VREF_25
10	PH2_3	<-- connect -->	AN23	IO_L14P_25
11	PH2_4	<-- connect -->	AM22	IO_L16N_25
12	PH2_5	<-- connect -->	AN22	IO_L16P_25
13	PH2_6	<-- connect -->	AP22	IO_L18P_25
14	PH2_7	<-- connect -->	AM21	IO_L13P_25
15	PH2_8	<-- connect -->	AP21	IO_L18N_25
16	PH2_9	<-- connect -->	AM20	IO_L13N_25
17	PH2_10	<-- connect -->	AN20	IO_L15P_25
18	PH2_11	<-- connect -->	AP20	IO_L15N_25
19	PH2_12	<-- connect -->	AN19	IO_L19P_25
20	PH2_13	<-- connect -->	AP19	IO_L19N_25
21	PH2_14	<-- connect -->	AM18	IO_L17N_25
22	PH2_15	<-- connect -->	AN18	IO_L17P_25
23	PH2_16	<-- connect -->	AP30	IO_L3P_25
24	PH2_17	<-- connect -->	AN30	IO_L2P_25
25	PH2_18	<-- connect -->	AM30	IO_L2N_25
26	PH2_19	<-- connect -->	AP29	IO_L5P_25
27	PH2_20	<-- connect -->	AN29	IO_L5N_25
28	PH2_21	<-- connect -->	AL29	IO_L0P_25
29	PH2_22	<-- connect -->	AM28	IO_L7N_25
30	PH2_23	<-- connect -->	AL28	IO_L4N_VREF_25
31	PH2_24	<-- connect -->	AL26	IO_L9N_CC_25
32	PH2_25	<-- connect -->	AM26	IO_L9P_CC_25
33	PH2_26	<-- connect -->	AP26	IO_L10P_CC_25
34	PH2_27	<-- connect -->	AL25	IO_L11P_CC_25
35	PH2_28	<-- connect -->	AM25	IO_L8N_CC_25
36	PH2_29	<-- connect -->	AP25	IO_L10N_CC_25

Table 5.9 Pin Header (JP13) and FPGA Pin Connection (2/2)

Connector Pin #	Pin Name		FPGA Pin #	Pin Description
37	PH2_30	<-- connect -->	AN25	IO_L8P_CC_25
38	PH2_31	<-- connect -->	AL24	IO_L11N_CC_25
39	PH2_32	<-- connect -->	AM31	IO_L1P_25
40	PH2_33	<-- connect -->	AP31	IO_L3N_25
41	PH2_34	<-- connect -->	AL31	IO_L1N_25
42	PH2_35	<-- connect -->	AL30	IO_L0N_25
43	PH2_36	<-- connect -->	AN28	IO_L7P_25
44	PH2_37	<-- connect -->	AM27	IO_L4P_25
45	PH2_38	<-- connect -->	AP27	IO_L6P_25
46	PH2_39	<-- connect -->	AN27	IO_L6N_25
47	GND			
48	GND			
49	VCC_PH			
50	VCC_PH			

5-3-8 GTP Clock 8

- The clock signal from the X3 converts into LVDS and connects it to the FPGA's GTP clock pin using an onboard IDT's ICS85411.
- GTP Clock (X3): Epson Toyocom's EG2121CA-LGPA156.25M

Table 5.10 GTP Clock and FPGA Pin Connection

Reference	Signal Name	FPGA Pin #	GTP Tile
X3	MGT_REFCLK1P	E4	120
	MGT_REFCLK1N	D4	
	MGT_REFCLK2P	AL5	122
	MGT_REFCLK2N	AL4	

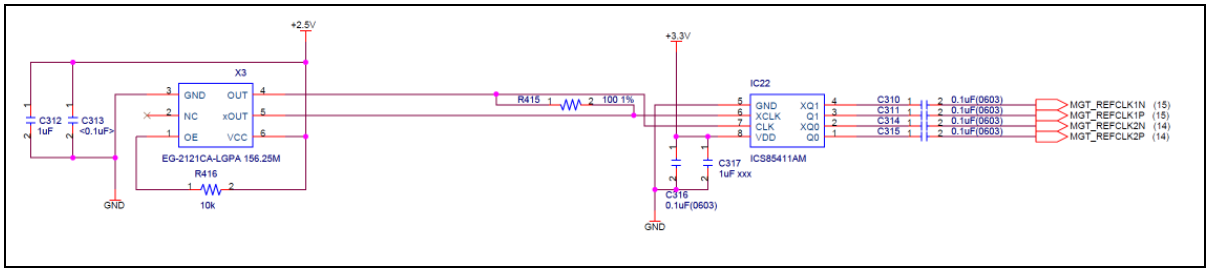


Figure 5.6 Signal Conversion Circuit of an MMCX Connector for Clock Input

5-3-9 Option I/O (9)

- The board provides 3 Option I/Os for connecting the dedicated Option board.
- The Option I/O 1 connects to CN18, Option I/O 2 to CN19 and Option I/O 3 to CN20.

Table 5.11 Option I/O 1's FPGA Pin Connection

FPGA Pin #	FPGA Pin Name	Signal Name
H17	IO_L0P_CC_GC_3	OP1_0
H18	IO_L0N_CC_GC_3	OP1_1
J10	IO_L9P_CC_20	OP1_2
J9	IO_L9N_CC_20	OP1_3
F9	IO_L1P_20	OP1_4
F8	IO_L1N_20	OP1_5
K8	IO_L10P_CC_20	OP1_6
K9	IO_L10N_CC_20	OP1_7
K11	IO_L5P_20	OP1_8
J11	IO_L5N_20	OP1_9
M10	IO_L16P_20	OP1_10
L9	IO_L16N_20	OP1_11
H10	IO_L7P_20	OP1_12
H9	IO_L7N_20	OP1_13
L10	IO_L12P_VRN_20	OP1_14
L11	IO_L12N_VRP_20	OP1_15
D11	IO_L4P_20	OP1_16
D10	IO_L4N_VREF_20	OP1_17
D12	IO_L6P_20	OP1_18
C12	IO_L6N_20	OP1_19
A13	IO_L8P_CC_20	OP1_20
B12	IO_L8N_CC_20	OP1_21
B13	IO_L11P_CC_20	OP1_22
C13	IO_L11N_CC_20	OP1_23
F13	IO_L19P_20	OP1_24
G13	IO_L19N_20	OP1_25
E12	IO_L17P_20	OP1_26
E13	IO_L17N_20	OP1_27
G11	IO_L13P_20	OP1_28
G12	IO_L13N_20	OP1_29
G8	IO_L3P_20	OP1_30
H8	IO_L3N_20	OP1_31
E9	IO_L0P_20	OP1_32
E8	IO_L0N_20	OP1_33
F10	IO_L2P_20	OP1_34
G10	IO_L2N_20	OP1_35
F11	IO_L15P_20	OP1_36
E11	IO_L15N_20	OP1_37
M8	IO_L14P_20	OP1_38
L8	IO_L14N_VREF_20	OP1_39
H14	IO_L6P_GC_3	OP1_40
H15	IO_L6N_GC_3	OP1_41

Table 5.12 Option I/O 2's FPGA Pin Connection

FPGA Pin #	FPGA Pin Name	Signal Name
J14	IO_L8P_GC_3	OP2_0
H13	IO_L8N_GC_3	OP2_1
C14	IO_L3P_5	OP2_2
C15	IO_L3N_5	OP2_3
D14	IO_L9P_CC_5	OP2_4
E14	IO_L9N_CC_5	OP2_5
A15	IO_L1P_5	OP2_6
A14	IO_L1N_5	OP2_7
B16	IO_L0P_5	OP2_8
B15	IO_L0N_5	OP2_9
B17	IO_L2P_5	OP2_10
A16	IO_L2N_5	OP2_11
E19	IO_L4P_5	OP2_12
F19	IO_L4N_VREF_5	OP2_13
F18	IO_L14P_5	OP2_14
G18	IO_L14N_VREF_5	OP2_15
F14	IO_L18P_5	OP2_16
F15	IO_L18N_5	OP2_17
D16	IO_L7P_5	OP2_18
D15	IO_L7N_5	OP2_19
E21	IO_L6P_5	OP2_20
D20	IO_L6N_5	OP2_21
G20	IO_L8P_CC_5	OP2_22
F20	IO_L8N_CC_5	OP2_23
D21	IO_L13P_5	OP2_24
D22	IO_L13N_5	OP2_25
F21	IO_L11P_CC_5	OP2_26
G21	IO_L11N_CC_5	OP2_27
D24	IO_L17P_5	OP2_28
E23	IO_L17N_5	OP2_29
F24	IO_L19P_5	OP2_30
E24	IO_L19N_5	OP2_31
C17	IO_L5P_5	OP2_32
D17	IO_L5N_5	OP2_33
G17	IO_L16P_5	OP2_34
F16	IO_L16N_5	OP2_35
E17	IO_L10P_CC_5	OP2_36
E16	IO_L10N_CC_5	OP2_37
E18	IO_L12P_VRN_5	OP2_38
D19	IO_L12N_VRP_5	OP2_39
J16	IO_L4P_GC_3	OP2_40
J17	IO_L4N_GC_VREF_3	OP2_41

- **Used for TB-5V-LX110T/FX70T-PCIEXP only**

Table 5.13 Option I/O 3's FPGA Pin Connection

FPGA Pin #	FPGA Pin Name	Signal Name
J20	IO_L7P_GC_3	OP3_0
J21	IO_L7N_GC_3	OP3_1
C20	IO_L0P_23	OP3_2
B20	IO_L0N_23	OP3_3
B21	IO_L1P_23	OP3_4
A21	IO_L1N_23	OP3_5
B18	IO_L4P_23	OP3_6
A18	IO_L4N_VREF_23	OP3_7
C19	IO_L2P_23	OP3_8
C18	IO_L2N_23	OP3_9
A19	IO_L6P_23	OP3_10
A20	IO_L6N_23	OP3_11
B27	IO_L10P_CC_23	OP3_12
A26	IO_L10N_CC_23	OP3_13
D26	IO_L13P_23	OP3_14
C27	IO_L13N_23	OP3_15
B25	IO_L11P_CC_23	OP3_16
C25	IO_L11N_CC_23	OP3_17
B26	IO_L9P_CC_23	OP3_18
A25	IO_L9N_CC_23	OP3_19
C24	IO_L8P_CC_23	OP3_20
D25	IO_L8N_CC_23	OP3_21
C23	IO_L5P_23	OP3_22
B23	IO_L5N_23	OP3_23
A23	IO_L7P_23	OP3_24
A24	IO_L7N_23	OP3_25
C22	IO_L3P_23	OP3_26
B22	IO_L3N_23	OP3_27
A30	IO_L19P_23	OP3_28
B30	IO_L19N_23	OP3_29
A29	IO_L14P_23	OP3_30
A28	IO_L14N_VREF_23	OP3_31
C30	IO_L17P_23	OP3_32
D29	IO_L17N_23	OP3_33
B31	IO_L16P_23	OP3_34
A31	IO_L16N_23	OP3_35
C29	IO_L12P_VRN_23	OP3_36
B28	IO_L12N_VRP_23	OP3_37
C28	IO_L15P_23	OP3_38
D27	IO_L15N_23	OP3_39
H19	IO_L9P_GC_3	OP3_40
H20	IO_L9N_GC_3	OP3_41

- **Used for TB-5V-LX110T/FX70T-PCIEXP only**

5-3-10 Memory DDR2-SDRAM (10)

- The board provides a DDR2-SDRAM (MT47H32M16BT-37E).
- Series resistors are installed at the memory side for DQS/DQ signals and at the FPGA side for address/control signals.
  It is assumed that the ODT at the memory side is used for termination. The FPGA side is not terminated.

Table 5.14 DDR2SDRAM (IC19) and FPGA Pin Connection

FPGA			DDR2SDRAM	
Pin #	Pin Name		Pin #	Pin Name
H28	IO_L9P_CC_19	<-- connect -->	R8	A0
L28	IO_L13N_19	<-- connect -->	R3	A1
G28	IO_L9N_CC_19	<-- connect -->	R7	A2
M28	IO_L15P_19	<-- connect -->	T2	A3
H27	IO_L8N_CC_19	<-- connect -->	T8	A4
M25	IO_L3P_19	<-- connect -->	T3	A5
E27	IO_L11N_CC_19	<-- connect -->	T7	A6
N28	IO_L15N_19	<-- connect -->	U2	A7
F28	IO_L10N_CC_19	<-- connect -->	U8	A8
P26	IO_L16P_19	<-- connect -->	U3	A9
K28	IO_L13P_19	<-- connect -->	R2	A10
E26	IO_L11P_CC_19	<-- connect -->	U7	A11
P27	IO_L16N_19	<-- connect -->	V2	A12
T28	IO_L15P_15	<-- connect -->	L2	BA0
U27	IO_L16P_15	<-- connect -->	L3	BA1
R26	IO_L17P_15	<-- connect -->	P7	XCAS
T26	IO_L18N_15	<-- connect -->	N7	XRAS
U25	IO_L19P_15	<-- connect -->	N3	XWE
R27	IO_L17N_15	<-- connect -->	N9	ODT
H29	IO_L2P_15	<-- connect -->	M8	CK
J29	IO_L2N_15	<-- connect -->	N8	XCK
U26	IO_L18P_15	<-- connect -->	N2	CKE
T25	IO_L19N_15	<-- connect -->	P8	XCS
E29	IO_L0P_15	<-- connect -->	J3	LDM
E31	IO_L3N_15	<-- connect -->	E3	UDM
L29	IO_L4P_15	<-- connect -->	G8	DQ0
M30	IO_L7N_15	<-- connect -->	G2	DQ1
F29	IO_L0N_15	<-- connect -->	H7	DQ2
L30	IO_L7P_15	<-- connect -->	H3	DQ3
U28	IO_L16N_15	<-- connect -->	H1	DQ4
G31	IO_L5N_15	<-- connect -->	H9	DQ5
U30	IO_L14P_15	<-- connect -->	F1	DQ6
H30	IO_L5P_15	<-- connect -->	F9	DQ7
J31	IO_L6N_15	<-- connect -->	C8	DQ8
T29	IO_L15N_15	<-- connect -->	C2	DQ9
J30	IO_L6P_15	<-- connect -->	D7	DQ10
R31	IO_L13N_15	<-- connect -->	D3	DQ11
T31	IO_L13P_15	<-- connect -->	D1	DQ12
G30	IO_L1P_15	<-- connect -->	D9	DQ13
F31	IO_L3P_15	<-- connect -->	B1	DQ14
F30	IO_L1N_15	<-- connect -->	B9	DQ15
K31	IO_L9P_CC_15	<-- connect -->	F7	LDQS
L31	IO_L9N_CC_15	<-- connect -->	E8	XLDQS
M31	IO_L11P_CC_15	<-- connect -->	B7	UDQS
N30	IO_L11N_CC_15	<-- connect -->	A8	XUDQS

5-3-11 Memory DDR2-SO-DIMM (11)

- The board provides a 200pin SO-DIMM connector that allows DDR2-SO-DIMM connections.
- Series resisttors are installed at the memory side for DQS/DQ signals and at the FPGA side for address/control signals.

It is assumed that the ODT at the memory side is used for termination. The FPGA side is not terminated.

Table 5.15 DDR2-SO-DIMM(CN6) and FPGA Pin Connection (1/3)

FPGA			DDR2-SO-DIMM(CN6)
Pin #	Pin Name		Pin Name
AD26	IO_L18P_21	<-- connect -->	A0
AB28	IO_L5P_21	<-- connect -->	A1
AF28	IO_L7N_21	<-- connect -->	A2
AB26	IO_L3N_21	<-- connect -->	A3
AG27	IO_L14P_21	<-- connect -->	A4
AC27	IO_L1N_21	<-- connect -->	A5
AG28	IO_L6P_21	<-- connect -->	A6
AH27	IO_L11P_CC_21	<-- connect -->	A7
AC28	IO_L4P_21	<-- connect -->	A8
AE27	IO_L16P_21	<-- connect -->	A9
AB27	IO_L1P_21	<-- connect -->	A10
AH28	IO_L6N_21	<-- connect -->	A11
AE28	IO_L7P_21	<-- connect -->	A12
AB25	IO_L3P_21	<-- connect -->	A13
AJ26	IO_L11N_CC_21	<-- connect -->	A14
AK27	IO_L10N_CC_21	<-- connect -->	A15
AA28	IO_L5N_21	<-- connect -->	BA0
AA26	IO_L0N_21	<-- connect -->	BA1
AE26	IO_L16N_21	<-- connect -->	BA2
V29	IO_L7N_17	<-- connect -->	CASn
V27	IO_L5N_17	<-- connect -->	RASn
W31	IO_L6P_17	<-- connect -->	WEn
V28	IO_L5P_17	<-- connect -->	ODT0
V25	IO_L2P_17	<-- connect -->	ODT1
AC33	IO_L7P_SM2P_13	<-- connect -->	CK0
AB33	IO_L7N_SM2N_13	<-- connect -->	CKn0
B32	IO_L0P_11	<-- connect -->	CK1
A33	IO_L0N_11	<-- connect -->	CKn1
AF26	IO_L15N_21	<-- connect -->	CKE0
AK28	IO_L10P_CC_21	<-- connect -->	CKE1
V30	IO_L4P_17	<-- connect -->	CSn0
W26	IO_L1N_17	<-- connect -->	CSn1
AN34	IO_L18P_13	<-- connect -->	DM0
AH29	IO_L19P_17	<-- connect -->	DM1
AD32	IO_L11P_CC_13	<-- connect -->	DM2
Y31	IO_L6N_17	<-- connect -->	DM3
V32	IO_L0P_SM8P_13	<-- connect -->	DM4
U33	IO_L18P_SM10P_11	<-- connect -->	DM5
U31	IO_L19N_SM9N_11	<-- connect -->	DM6
D32	IO_L2N_11	<-- connect -->	DM7
AK32	IO_L15N_13	<-- connect -->	DQ0
AK33	IO_L13N_13	<-- connect -->	DQ1
AJ32	IO_L15P_13	<-- connect -->	DQ2
AM33	IO_L17P_13	<-- connect -->	DQ3
AP32	IO_L19N_13	<-- connect -->	DQ4
AN32	IO_L19P_13	<-- connect -->	DQ5
AM32	IO_L17N_13	<-- connect -->	DQ6
AL33	IO_L16N_13	<-- connect -->	DQ7
AK31	IO_L16N_17	<-- connect -->	DQ8
AJ30	IO_L18P_17	<-- connect -->	DQ9
AE29	IO_L15P_17	<-- connect -->	DQ10
AD29	IO_L15N_17	<-- connect -->	DQ11
AJ31	IO_L16P_17	<-- connect -->	DQ12
AH30	IO_L18N_17	<-- connect -->	DQ13

Table 5.15 DDR2-SO-DIMM(CN6) and FPGA Pin Connection (2/3)

FPGA			DDR2-SO-DIMM(CN6)
Pin #	Pin Name		Pin Name
AG30	IO_L19N_17	<-- connect -->	DQ14
AF29	IO_L17P_17	<-- connect -->	DQ15
AK34	IO_L13P_13	<-- connect -->	DQ16
AG32	IO_L14P_13	<-- connect -->	DQ17
AL34	IO_L16P_13	<-- connect -->	DQ18
AN33	IO_L18N_13	<-- connect -->	DQ19
AD34	IO_L5N_SM4N_13	<-- connect -->	DQ20
AC32	IO_L6P_SM3P_13	<-- connect -->	DQ21
AC34	IO_L5P_SM4P_13	<-- connect -->	DQ22
AB32	IO_L6N_SM3N_13	<-- connect -->	DQ23
AD30	IO_L13P_17	<-- connect -->	DQ24
AC29	IO_L13N_17	<-- connect -->	DQ25
W29	IO_L7P_17	<-- connect -->	DQ26
W27	IO_L3N_17	<-- connect -->	DQ27
AF31	IO_L14P_17	<-- connect -->	DQ28
AF30	IO_L17N_17	<-- connect -->	DQ29
Y26	IO_L1P_17	<-- connect -->	DQ30
Y27	IO_L3P_17	<-- connect -->	DQ31
Y32	IO_L4P_13	<-- connect -->	DQ32
W34	IO_L1P_SM7P_13	<-- connect -->	DQ33
V34	IO_L1N_SM7N_13	<-- connect -->	DQ34
V33	IO_L0N_SM8N_13	<-- connect -->	DQ35
AA33	IO_L2N_SM6N_13	<-- connect -->	DQ36
AA34	IO_L3P_SM5P_13	<-- connect -->	DQ37
Y33	IO_L2P_SM6P_13	<-- connect -->	DQ38
Y34	IO_L3N_SM5N_13	<-- connect -->	DQ39
M32	IO_L13N_11	<-- connect -->	DQ40
L33	IO_L13P_11	<-- connect -->	DQ41
C33	IO_L1N_11	<-- connect -->	DQ42
T33	IO_L16P_SM12P_11	<-- connect -->	DQ43
N32	IO_L15N_SM13N_11	<-- connect -->	DQ44
U32	IO_L19P_SM9P_11	<-- connect -->	DQ45
T34	IO_L18N_SM10N_11	<-- connect -->	DQ46
R34	IO_L16N_SM12N_11	<-- connect -->	DQ47
G33	IO_L7P_11	<-- connect -->	DQ48
F34	IO_L7N_11	<-- connect -->	DQ49
R33	IO_L17P_SM11P_11	<-- connect -->	DQ50
R32	IO_L17N_SM11N_11	<-- connect -->	DQ51
P34	IO_L14P_11	<-- connect -->	DQ52
K33	IO_L11P_CC_SM14P_11	<-- connect -->	DQ53
C34	IO_L3P_11	<-- connect -->	DQ54
G32	IO_L4P_11	<-- connect -->	DQ55
P32	IO_L15P_SM13P_11	<-- connect -->	DQ56
D34	IO_L3N_11	<-- connect -->	DQ57
C32	IO_L2P_11	<-- connect -->	DQ58
B33	IO_L1P_11	<-- connect -->	DQ59
F33	IO_L5P_11	<-- connect -->	DQ60
E34	IO_L5N_11	<-- connect -->	DQ61
E33	IO_L6N_11	<-- connect -->	DQ62
E32	IO_L6P_11	<-- connect -->	DQ63
AH34	IO_L10P_CC_13	<-- connect -->	DQS0
AJ34	IO_L10N_CC_13	<-- connect -->	DQSn0
AB31	IO_L9P_CC_17	<-- connect -->	DQS1
AA31	IO_L9N_CC_17	<-- connect -->	DQSn1
AF33	IO_L8P_CC_SM1P_13	<-- connect -->	DQS2
AE33	IO_L8N_CC_SM1N_13	<-- connect -->	DQSn2
AA29	IO_L11P_CC_17	<-- connect -->	DQS3
AA30	IO_L11N_CC_17	<-- connect -->	DQSn3
AF34	IO_L9P_CC_SM0P_13	<-- connect -->	DQS4
AE34	IO_L9N_CC_SM0N_13	<-- connect -->	DQSn4

Table 5.15 DDR2-SO-DIMM(CN6) and FPGA Pin Connection (3/3)

FPGA			DDR2-SO-DIMM(CN6)
Pin #	Pin Name		Pin Name
L34	IO_L10P_CC_SM15P_11	<-- connect -->	DQS5
K34	IO_L10N_CC_SM15N_11	<-- connect -->	DQSn5
H34	IO_L9P_CC_11	<-- connect -->	DQS6
J34	IO_L9N_CC_11	<-- connect -->	DQSn6
J32	IO_L8P_CC_11	<-- connect -->	DQS7
H33	IO_L8N_CC_11	<-- connect -->	DQSn7

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- CameraLink MDR Connector (CN4): 3M's 10226-1A10PE

Table 5.16 CameraLink FPGA Pin Connection

FPGA Pin #	FPGA Pin Name	Pin Name
AC4	IO_L0P_18	CMR_X0P
AC5	IO_L0N_18	CMR_X0N
AC7	IO_L3P_18	CMR_X1P
AD7	IO_L3N_18	CMR_X1N
AD6	IO_L7P_18	CMR_X2P
AE6	IO_L7N_18	CMR_X2N
AB6	IO_L1P_18	CMR_X3P
AB7	IO_L1N_18	CMR_X3N
AG5	IO_L10P_CC_18	CMR_CC1P
AF5	IO_L10N_CC_18	CMR_CC1N
AH7	IO_L14P_18	CMR_CC2P
AG7	IO_L14N_VREF_18	CMR_CC2N
AD4	IO_L5P_18	CMR_CC3P
AD5	IO_L5N_18	CMR_CC3N
AE7	IO_L9P_CC_18	CMR_CC4P
AF6	IO_L9N_CC_18	CMR_CC4N
AH5	IO_L12P_VRN_18	CMR_SERTCP
AG6	IO_L12N_VRP_18	CMR_SERTCN
AA5	IO_L2P_18	CMR_SERTFGP
AB5	IO_L2N_18	CMR_SERTFGN
AH12	IO_L1P_GC_D13_4	CMR_XCLKP
AG13	IO_L1N_GC_D12_4	CMR_XCLKN

5-3-13 Ethernet MAC & PHY 13

- The board uses a VITESSE's chip as PHY to enable10/100/1000M Ethernet connections via a RJ-45 connector (CN7).
- PHY Chip (IC20): VITESSE

■ Due to the NDA contract with parts makers, we are not allowed to disclose technical information on the circuits around Ethernet on this board.

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- FlashROM (IC18): Spansion's S29JL064H70TFI000A

Table 5.17 PHY Chip and FPGA Pin Connection

FPGA			S29JL064H70TFI000A(IC18)
Pin #	Pin Name		Signal Name
AB10	IO_L1P_22	<-- connect -->	A0
AA10	IO_L1N_22	<-- connect -->	A1
AA9	IO_L3N_22	<-- connect -->	A2
AA8	IO_L3P_22	<-- connect -->	A3
AC8	IO_L5P_22	<-- connect -->	A4
AB8	IO_L5N_22	<-- connect -->	A5
AC10	IO_L7P_22	<-- connect -->	A6
AC9	IO_L7N_22	<-- connect -->	A7
AD9	IO_L9N_CC_22	<-- connect -->	A8
AE8	IO_L9P_CC_22	<-- connect -->	A9
AD11	IO_L10N_CC_22	<-- connect -->	A10
AD10	IO_L10P_CC_22	<-- connect -->	A11
AE9	IO_L12N_VRP_22	<-- connect -->	A12
AF8	IO_L12P_VRN_22	<-- connect -->	A13
AF10	IO_L14N_VREF_22	<-- connect -->	A14
AF9	IO_L14P_22	<-- connect -->	A15
AF11	IO_L16P_22	<-- connect -->	A16
AE11	IO_L16N_22	<-- connect -->	A17
AH8	IO_L18N_22	<-- connect -->	A18
AG8	IO_L18P_22	<-- connect -->	A19
AG11	IO_L19N_22	<-- connect -->	A20
AG10	IO_L19P_22	<-- connect -->	A21
AH9	IO_L17P_22	<-- connect -->	CE
AN14	IO_L0P_22	<-- connect -->	D0
AP14	IO_L0N_22	<-- connect -->	D1
AM13	IO_L2N_22	<-- connect -->	D2
AN13	IO_L2P_22	<-- connect -->	D3
AL11	IO_L8P_CC_22	<-- connect -->	D4
AL10	IO_L8N_CC_22	<-- connect -->	D5
AJ11	IO_L11N_CC_22	<-- connect -->	D6
AK11	IO_L11P_CC_22	<-- connect -->	D7
AN12	IO_L4N_VREF_22	<-- connect -->	D8
AP12	IO_L4P_22	<-- connect -->	D9
AM11	IO_L6N_22	<-- connect -->	D10
AM12	IO_L6P_22	<-- connect -->	D11
AK9	IO_L13N_22	<-- connect -->	D12
AK8	IO_L13P_22	<-- connect -->	D13
AJ10	IO_L15N_22	<-- connect -->	D14
AJ9	IO_L15P_22	<-- connect -->	D15
AH10	IO_L17N_22	<-- connect -->	OE
AF14	IO_L4N_VREF_FOE_B_MOSI_2	<-- connect -->	BYTE
AF13	IO_L2P_A23_2	<-- connect -->	RESET
AE13	IO_L0P_CC_RS1_2	<-- connect -->	RY/BY
AG12	IO_L2N_A22_2	<-- connect -->	WE
AE12	IO_L0N_CC_RS0_2	<-- connect -->	WP/ACC

5-3-15 MICTOR Connector 15

- MICTOR Connector: AMP's 2-5767004-2
- JTAG-ICE can be connected through the MICTRO Connector.

* To connect an ICE, set SW1 and JP2 according to the ICE manual. (ICE : Computex's F-sight)

Table 5.18 MICTOR Connector Pin Connection

Connector Pin #	Pin Name	Connect to	Connector Pin #	Pin Name	Connect to
1	NC		2	NC	
3	NC		4	NC	
5	NC		6	ANTZCLK	G23
7	NC		8	NC	
9	SRST	TESTPIN(TP27)	10	TRGOUT	TESTPIN(TP28)
11	TDO	FPGA(AD14)	12	Vtref	3.3V
13	NC		14	NC	
15	TCK	FPGA(AB15)	16	NC	
17	TMS	FPGA(AC14)	18	NC	
19	TDI	F_TDI	20	NC	
21	NC		22	NC	
23	CH15	FPGA(H22)	24	CH7	FPGA(K23)
25	CH14	FPGA(G22)	26	CH6	FPGA(K22)
27	CH13	FPGA(J22)	28	CH5	FPGA(L21)
29	CH12	FPGA(K21)	30	CH4	FPGA(L20)
31	CH11	FPGA(K16)	32	CH3	FPGA(L16)
33	CH10	FPGA(J15)	34	CH2	FPGA(L15)
35	CH9	FPGA(J12)	36	CH1	FPGA(K13)
37	CH8	FPGA(H12)	38	CH0	FPGA(K12)

5-3-16 RS232C 16

- The board uses an RS232C driver to enable serial connections via a pin header (CN5).
- RS232C Driver IC (IC17): MAXIM's MAX3380ECUP

Table 5.19 MAX3380ECUP and FPGA Pin Connection

FPGA			MAX3380ECUP	
Pin #	Signal Name		Pin #	Pin Name
AJ7	MAX_TxD	<-- connect -->	8	T1IN
AJ6	MAX_RxD	<-- connect -->	11	R1OUT
AK7	MAX_RTS	<-- connect -->	9	T2IN
AK6	MAX_CTS	<-- connect -->	10	R2OUT

Table 5.20 CN5 Pin Assignment

Pin #	Pin Name	Pin #	Pin Name
1	NC	2	NC
3	RxD	4	RTS
5	TxD	6	CTS
7	NC	8	NC
9	GND	10	NC

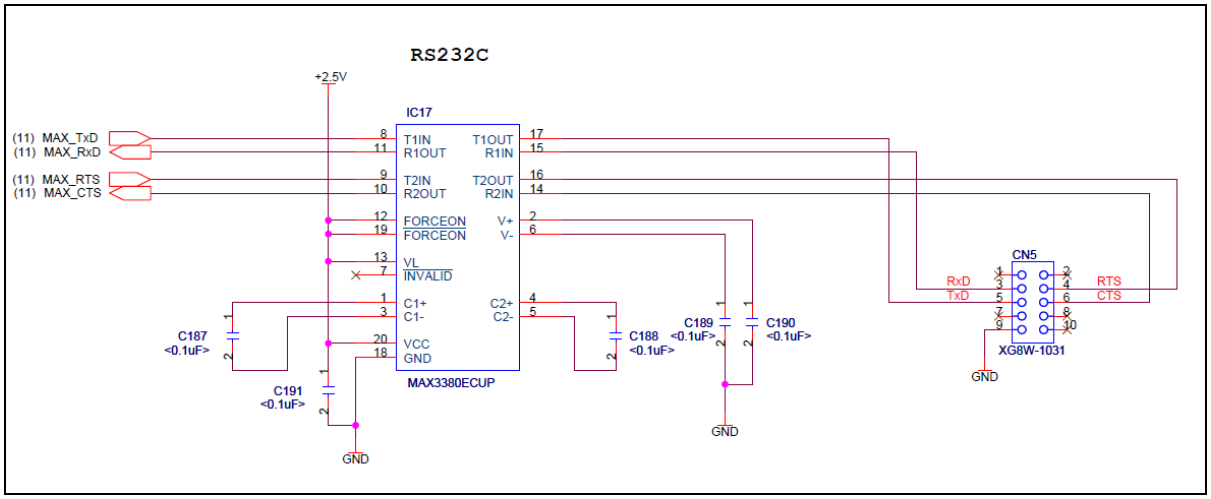


Figure 5.7 RS232C Driver Circuit

5-3-17 Universal Clock 17

- The board provides a 200MHz low-jitter crystal oscillator for high speed I/O operation.
  It also provides 125MHz low-jitter crystal oscillator for PHY.

Table 5.21 Universal Clock and FPGA Pin Connection

Reference	FPGA Pin #	FPGA I/O Bank
X2	AF18	4
	AE18	4
X1	AH15	4

5-3-18 User LED 18

- The board provides four red LEDs (LED 19-22) and four green LEDs (LED 23-26).
- All these LEDs will light on in Active High.

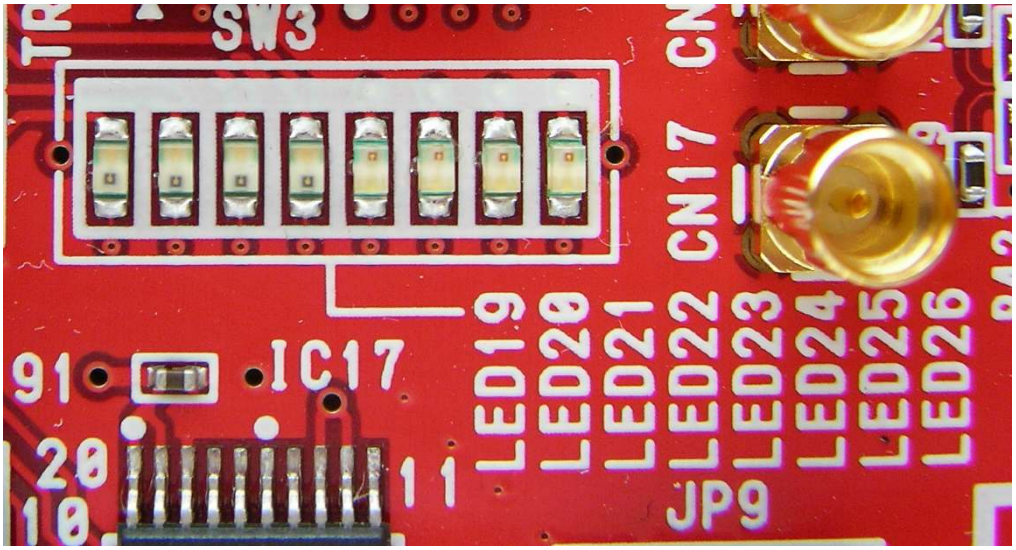


Figure 5.8 USER LED

Table 5.22 USER LED and FPGA Pin Connection

BD Silk		Reference	FPGA Pin #	FPGA Bank
LED	19	USER LED1	W6	18
	20	USER LED2	Y6	
	21	USER LED3	V7	
	22	USER LED4	W7	
	23	USER LED5	Y7	
	24	USER LED6	AA6	
	25	USER LED7	Y8	
	26	USER LED8	Y9	

5-3-19 User Dip Switch 19

- The board provides an 8bit Dip Switch. The side of the Dip Switch labeled “ON” is Low Level.

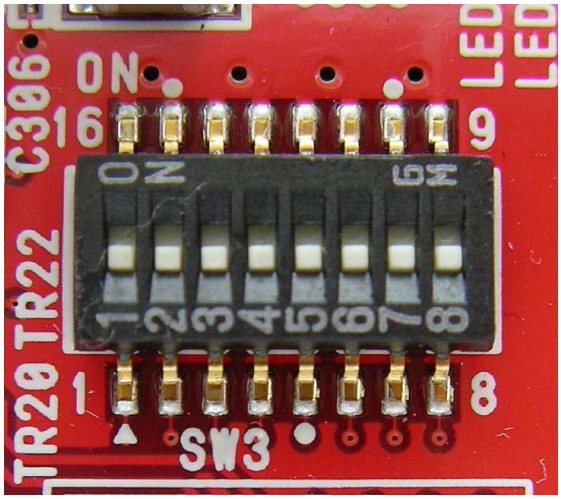


Figure 5.9 User Dip Switch

Table 5.23 UserDipSwitch and FPGA Pin Connection

Component Silk	Reference	FPGA Pin #	FPGA Bank
1	SW3	U7	12
2		T8	
3		P10	
4		R11	
5		T10	
6		T11	
7		T9	
8		U10	

5-3-20 User Push Switch 20

- The board provides four Push switches.
- Each switch provides a Low signal while it is kept pressed.

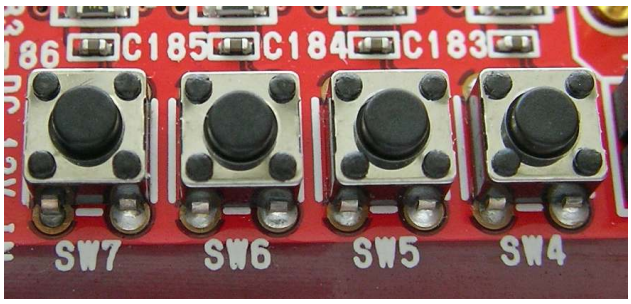


Figure 5.10 User Push Switch

Table5.24 User Push Switch and FPGA Pin Connection

Reference	FPGA Pin #	FPGA Bank
SW4	AF23	2
SW5	AG23	
SW6	AE22	
SW7	AE23	

5-3-21 PCI Express MidBUS Probe 21

- The board can connect a MidBUS probe for PCI Express.

Table 5.25 MidBUS Probe (U4) Pin Assignment

Connector Pin #	Pin Name	Signal Name	PCI_Edge Connected to	Connector Pin #	Pin Name	Signal Name	PCI_Edge Connected to
1	C0p-Upstream	RXP0	PETp0	2	GND		
3	C0n-Upstream	RXN0	PETn0	4	C0p-Downstream	TXP0	PERp0
5	GND			6	C0n-Downstream	TXN0	PERn0
7	C1p-Upstream	RXN1	PETp1	8	GND		
9	C1n-Upstream	RXP1	PETn1	10	C1p-Downstream	TXN1	PERp1
11	GND			12	C1n-Downstream	TXP1	PERn1
13	C2p-Upstream	RXP2	PETp2	14	GND		
15	C2n-Upstream	RXN2	PETn2	16	C2p-Downstream	TXP2	PERp2
17	GND			18	C2n-Downstream	TXN2	PERn2
19	C3p-Upstream	RXN3	PETp3	20	GND		
21	C3n-Upstream	RXP3	PETn3	22	C3p-Downstream	TXN3	PERp3
23	GND			24	C3n-Downstream	TXP3	PERn3
25	C4p-Upstream	RXP4	PETp4	26	GND		
27	C4n-Upstream	RXN4	PETn4	28	C4p-Downstream	TXP4	PERp4
29	GND			30	C4n-Downstream	TXN4	PERn4
31	C5p-Upstream	RXN5	PETp5	32	GND		
33	C5n-Upstream	RXP5	PETn5	34	C5p-Downstream	TXN5	PERp5
35	GND			36	C5n-Downstream	TXP5	PERn5
37	C6p-Upstream	RXP6	PETp6	38	GND		
39	C6n-Upstream	RXN6	PETn6	40	C6p-Downstream	TXP6	PERp6
41	GND			42	C6n-Downstream	TXN6	PERn6
43	C7p-Upstream	RXN7	PETp7	44	GND		
45	C7n-Upstream	RXP7	PETn7	46	C7p-Downstream	TXN7	PERp7
47	GND			48	C7n-Downstream	TXP7	PERn7

5-3-22 External Power Connector + Power Module 22

- The power supply can be switched either to the PCI Express edge or the external power connector using the power selection switch.
- The board generates a variety of different voltage from the 12V using LINEAR TECHNOLOGY's on board power chip.

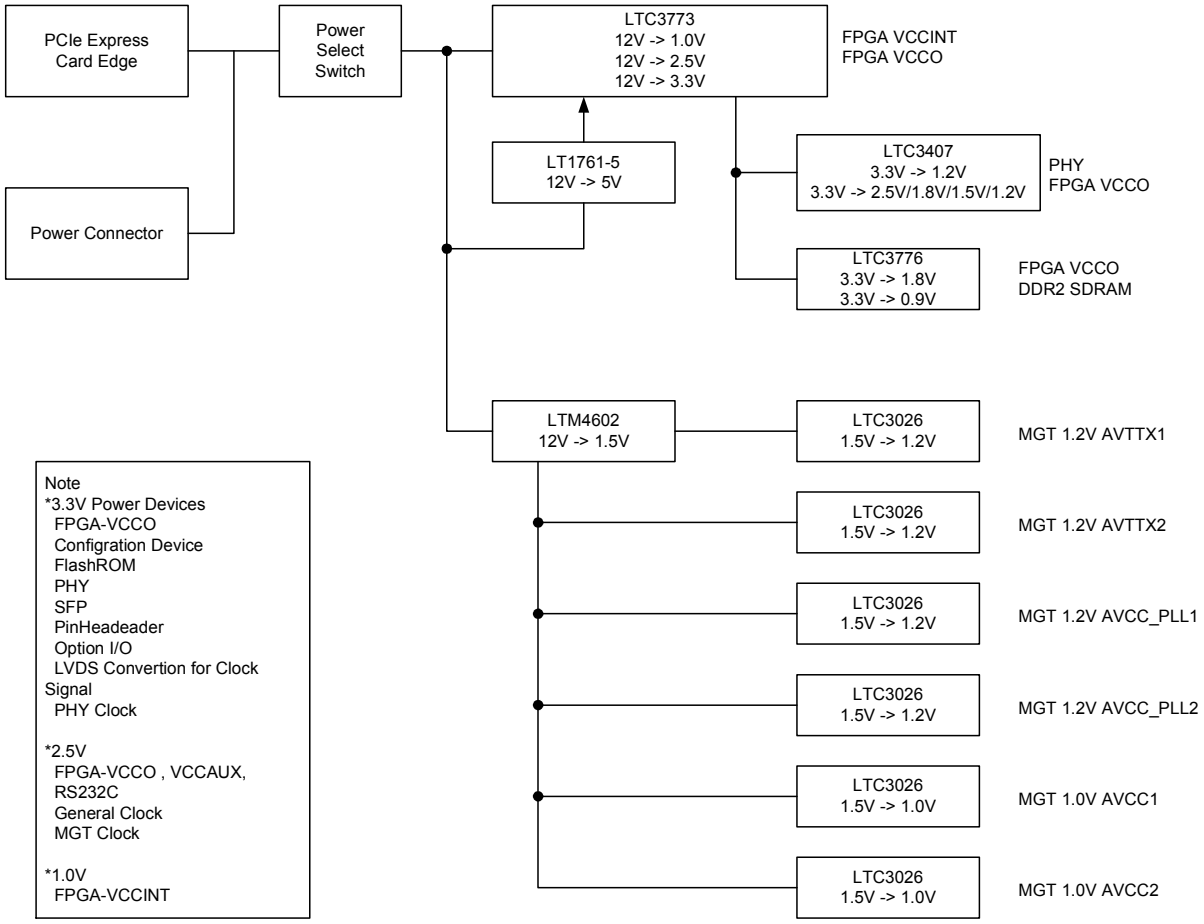


Figure5.11 Power Supply Diagram

5-3-23 Power Connector for Air-Cooling Fan 23

- The board provides a 12V power supply for air-cooling fan. A fan is not provided.
- Connector: JST's B2B-XH-Ag

Table 5.26 CN21 Pin Assignment

Reference	Terminal #	Function
CN21	1	12V
	2	GND

6. Jumper Pin Setting

6-1 Jumper Pin Setting

Table6.1 Jumper Pin Setting

Reference	# of Pins	Function	Default	Remarks
JP1	8	Power voltage selection (OP_V)	Open	1-2 2.5V 3-4 1.8V 5-6 1.5V 7-8 1.2V
JP2	4	Configuration selection	1-3Short	1-3 IC16 Open CN2
JP3	3	VCCO variable function for Bank3	2-3Short	1-2 OP_V 2-3 3.3V
JP4	3	VCCO variable function for Bank5 Only available for TB-LX110T/FX70T-PCIEX	2-3Short	1-2 OP_V 2-3 3.3V
JP5	3	VCCO variable function for Bank23 Only available for TB-LX110T/FX70T-PCIEX	2-3Short	1-2 OP_V 2-3 3.3V
JP6	3	VCCO variable function for Bank20	2-3Short	1-2 OP_V 2-3 3.3V
JP7	3	VCCO variable function for Bank6 Only available for TB-LX110T/FX70T-PCIEX	2-3Short	1-2 OP_V 2-3 3.3V
JP8	3	VCCO variable function for Bank25 Only available for TB-LX110T/FX70T-PCIEX	2-3Short	1-2 OP_V 2-3 3.3V
JP9	9	PCI Express edge PRSNT signal selection	1-2Short	1-2 x1 3-4 x4 5-6 x8
JP11	3	Variable function for pin header 1 (JP10) power Only available for TB-LX110T/FX70T -PCIEX	1-2Short	1-2 OP_V 2-3 3.3V
JP12	3	Variable function for pin header 2 (JP13) power Only available for TB-LX110T/FX70T -PCIEX	1-2Short	1-2 OP_V 2-3 3.3V

NOTE : Gray Block is available for TB-5V-LX110T/FX70T-PCIEXP only.

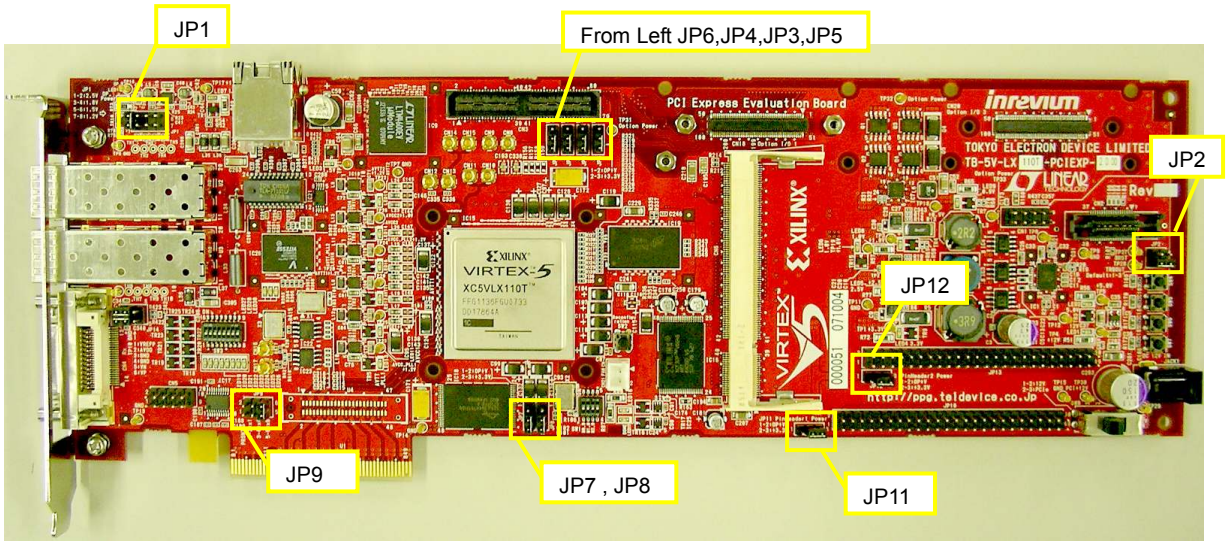


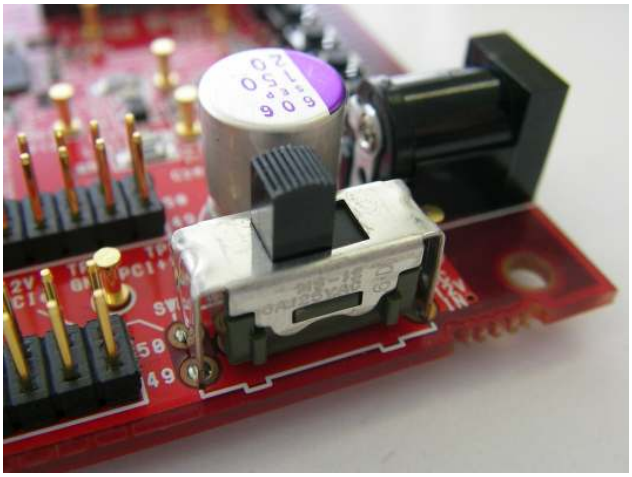
Figure 6.1 Jumper Pin Setting

6-2 External Power Connector and Power Selection Switch 24

- The SW8 allows power selection of either the PCI Express edge or the external power jack (JACK1).
  To connect the external power to JACK1, select the +12V.

Table 6.2 Power Selection Switch

Reference	# of Pins	Function	At factory	Remarks
SW8	2	Power selection 1PIN-side: External 3PIN-side: PCI Express edge	1PIN-side	



* In the above picture the power is supplied from the PCI Express edge.

Figure 6.2 External Power Jack and Power Selection Switch

7. FPGA Configuration 25

- Let's perform FPGA configuration from the XCF32PVO48(IC16).
  Connect a JTAG cable to the 10-pin header(CN1) and download the PROM file created by the Xilinx's iMPACT tool. Then, turn the power switch on again to configuration FPGA from XCF32PVO48. If the configuration is successfully, the green-colored LED18 "DONE_LED" will light up.
  To implement the re-configuration, press the SW2.

* When downloading a file to the XCF32PVO48, make sure that the "Parallel mode" checkbox is checked on the Xilinx's iMPACT tool window.

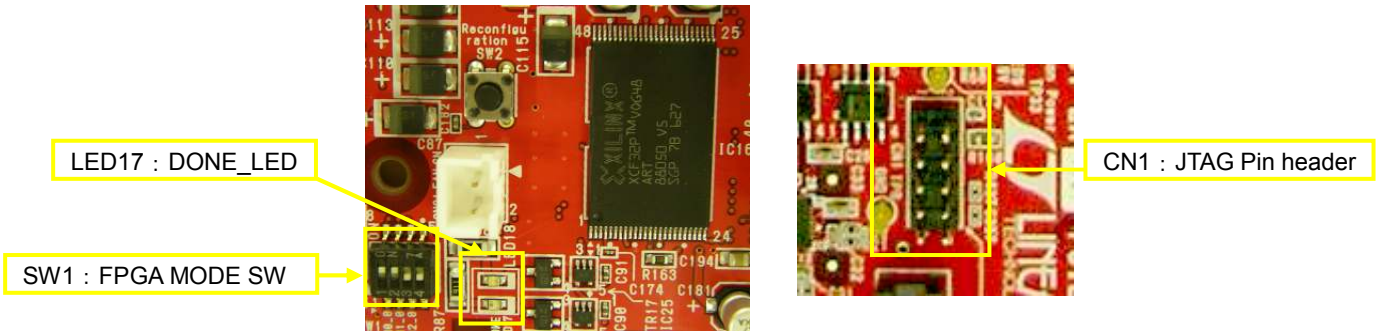


Figure 7.1 Configuration

Table 7.1 J12: JTAG Pin Header Terminals

Reference	Terminal #	Function
CN1	1	GND
	2	3.3V
	3	GND
	4	TDI
	5	GND
	6	TMS
	7	GND
	8	TCK
	9	GND
	10	TDO

Table 7.2 SW1: FPGA MODE Pin Terminals

Reference	Terminal #	Function
SW1	1	M0
	2	M1
	3	M2
	4	NONE

(The side labeled as "ON" will set Low)

<<Revision History>>

Revision	Date	Description
Rev.1.00	2007/10/1	Initial release
Rev.1.01	2007/11/12	Add New devise lineup XC5VSX50T-1FF1136. 4. Board Overview 4-3-2. PCI Express signal connection 4-3-22. External Power Connector + Power Module 6. FPGA Configuration
Rev2.00	2008/9/30	FXT series addition Head office address
Rev2.01	2008/10/15	Table 5.1 is changed
Rev2.02	2009/06/04	Table 7.2 is changed

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