

SC14428 Baseband Processor for FP & PP DECT and WDCT

1.0 General description

The SC14428 is a CMOS IC optimized to handle all the audio, signal and data processing needed within a DECT (1.9 GHz) or 2.4GHz ISM digital band base stations and handsets.

A four channel ADPCM transcoder, a very low power 16 bit Codec and Analog Frontend are integrated. Direct connections towards PSTN or ISDN line interface are possible.

The SC14428 has a programmable Generic DSP optimized for telecom applications.

The SC14428 is designed to fit to any radio interface. A dedicated TDMA controller handles all physical layer slot formats and radio control.

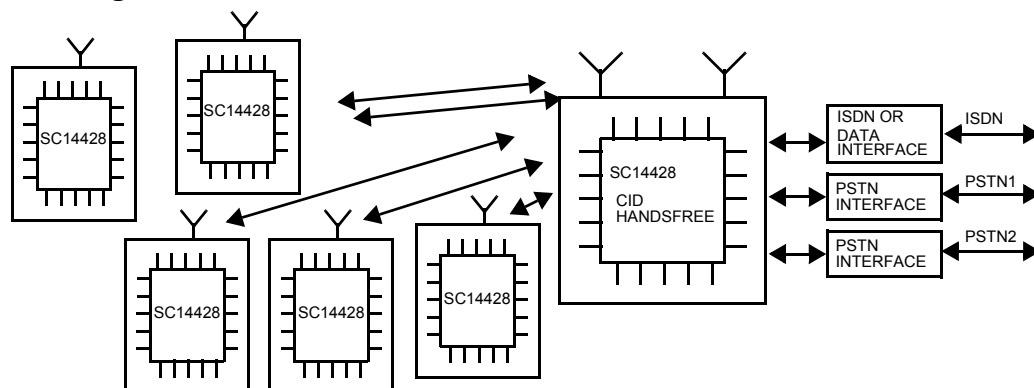
National Semiconductor's standard CompactRISC™ CR16C microprocessor takes care of all the higher protocol stack.

2.0 Features

- Complies with DECT ETS 300 175-2,3 & 8 SWAP-CA V1.3 Rev 1.3 20000616
- 1.8Volt operating voltage with 2.65V (typ) IO pads.
- Two chip low drop voltage regulators
- 16 bit CompactRISC™ CR16C Microprocessor with programmable clock speeds up to 20.736 MHz.
- Four channel DMA controller.
- Serial Debug interface, Nexus Class-1 compliant.
- 16kbyte shared, 6kbyte non shared RAM
- 4kbyte shared RAM for TAM DSP
- Versions with ROM, FLASH and data FLASH

- Programmable 16 bits system bus interface with bus master and slave operation.
- User programmable GENERIC DSP with fixed telecom processing routines.
- Four full duplex 32 kbits/sec ADPCM transcoder.
- On-chip Dedicated Instruction Processor (DiP) for all TDMA based events, which supports DCT 1.152MHz, 0.576MHz and 0.288MHz data rates.
- ISM band and DECT with 9.216, 10.368 and 13.824 MHz xtals.
- Protected and unprotected full and double slot B-fields
- Flexible 1.152 Mbit/sec three wire interface to radio front synthesizer.
- One 16-bit linear CODEC
- Selectable Fast Antenna Diversity operation or RSSI measurement with peak hold ADC.
- Three input general purpose 8 bit ADC
- Two general purpose timers and watch dog timer.
- Two Capture timers for frequency measurement for e.g. metering, ringing and call progress tone detection.
- Three general purpose I/O ports with two edge/level programmable interrupts
- Full duplex UART and MICROWIRE™ interface.
- SPI™ interface (Master/Slave).
- Flexible 8 kHz synchronous Serial interface to external codecs and ISDN interface circuits.
- Three programmable chip selects
- Integrated opamp for caller-id
- (80 pin PFQP and 80,)128,160 pins TQFP packages.

3.0 System Diagram



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3.0 System Diagram (Continued)

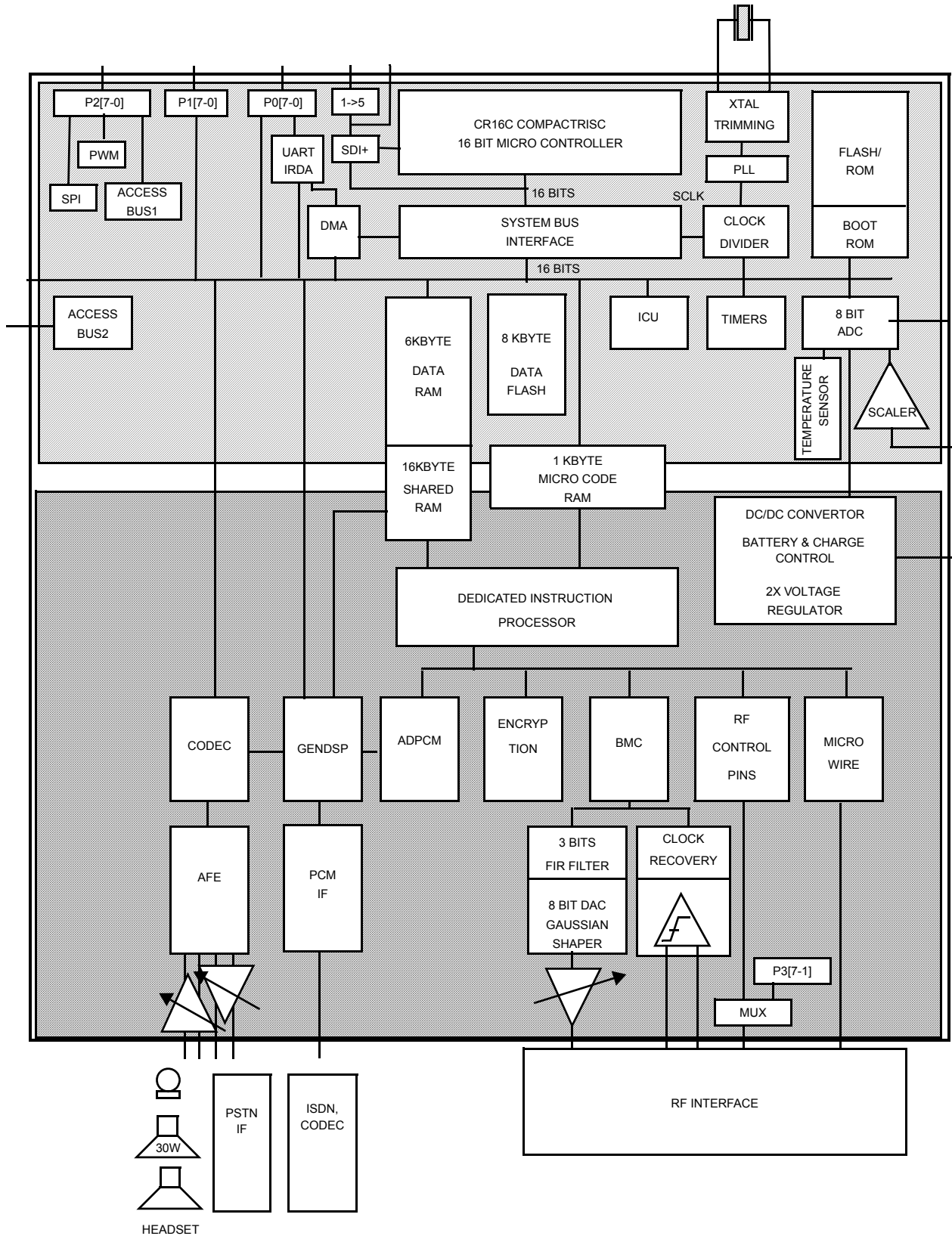


Figure 1. SC14428 Block diagram

4.0 Specifications

All min/max specification limits are guaranteed by design, or production test, or statistical methods.

Table 1. ABSOLUTE MAXIMUM RATINGS¹

Parameter	Description	Conditions	Min	Max	Units
Vbat1_max	Max Battery supply voltage VBAT1			5.5	V
Vbat2_max	Max Battery supply voltage VBAT2			5.5	V
Ibat1_max	Max negative current into VBAT1			300	mA
Ibat2_max	Max negative current into VBAT2			300	mA
Ivddiotot_max	Max total current into VDDIOs			90	mA
Ivddio_max	Max current through I/O pins			20	mA
Vdd_max	Max Core supply voltage (VDD-VSS / AVD-AVS / AVD2-AVS / VDDRF-VSSRF)			2.0	V
Vddiof_max	Max I/O Supply voltage for devices with FLASH (VDDIO-VSS)	Note ²		3.0	V
Vddio_max	Max I/O supply voltage for devices without FLASH (VDDIO-VSS)	Note ³		3.6	V
Vldo1_ctrl_max	Max voltage on pin LDO1_CTRL	Note ⁴	VSS-0.3	5.25	V
Vldo2_ctrl_max	Max voltage on pin LDO2_CTRL	Note ⁴	VSS-0.3	5.25	V
Vpon_max	Max voltage on pin PON		VSS-0.3	2.85	V
Vcharge_max	Max voltage on pin CHARGE		VSS-0.3	2.85	V
Vbat3_max	Max voltage on pin VBAT3		VSS-0.3	2.85	V
Vadc1_max	Max voltage on pin ADC1		VSS-0.3	2.85	V
Vrdidig_max	Max voltage on pin RDI digital mode (max 3.6V)		VSS-0.3	VDDIO+0.3	V
Vrdiana_max	Max voltage on pin RDI analog mode		VSS-0.3	2.0	V
Vdig_max	Max voltage on digital Input pins (max 3.6V)		VSS-0.3	VDDIO+0.3	V
Vana_max	Max voltage on any other input (incl analog pads)		VSS-0.3	2.0	V
Iprot_max	Max current through prot. diodes on any pin to VDDIO			100	mA
Iprotcid_max	Max current through prot. diode pins CID+/- to AGND			1.0	mA
Iprotmic_max	Current through prot. diode pin MIC+/- to AGND			2.4	mA
Iprotpon_max	Max current through prot. circuit of PON pin.	Note ⁵		0.6	mA
Iprotcharge_max	Max current through prot. circuit of CHARGE pin.	Note ⁵		0.6	mA
Iprotvat3_max	Max current through prot. circuit of VBAT3 pin.	Note ⁵		0.6	mA
Iprotadc1_max	Max current through prot. circuit of ADC1 pin.			0.6	mA
Tstorage	Storage temperature		-65	+150	°C
Ppackage	Package power dissipation @ 25 °C			500	mW
Ilu	Latch-up current all pins according JEDEC 78	TA = 65 °C		100	mA
Ilu_rdi_25	Latch-up current RDI pin	TA = 25 °C		100	mA
Ilu_rdi_60	Latch-up current RDI pin	TA = 65 °C		50	mA
Vesd_mm	ESD voltage according to man machine model			100	V
Vesd_hbm	ESD voltage according to human body model			1000	V

1. Absolute maximum ratings are those values that may be applied for maximum 50 hours.

Beyond these values, damage to the device may occur.

2. A voltage between 2.8V and 3.0V may applied for a maximum time of 1 hour in order to guarantee the device specifications.
3. A voltage between 3.3V and 3.6V may applied for a maximum time of 50 hours in order to guarantee the device specifications.
4. For LDO1_CTRL, LDO2_CTRL, with 5V input protection, VDD must be between 1.75V and 2.0V or Vbat 1 >2.0V or Vbat2 >2.8V.

4.0 Specifications (Continued)

5. The protection current can be calculated as follows:

In case P1[6]/PON, P1[7]/CHARGE, VBAT3, P2[3]/ADC1 is input, $I_{protxxx_max} = (V_{ext} - 2.55)/(500 + R_{ext})$

R_{ext} is an external resistor which is needed if the external voltage V_{ext} exceeds the 2.8V.

(A lower protection current value of e.g. 100 μ A is recommended in case power saving is important)

In case P1[6]/PON, P1[7]/CHARGE, P2[3]/ADC1 is output, $I_{protxxx_max} = (V_{DDIO} - 2.55)/(500)$

Table 2. OPERATING CONDITIONS ¹

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vbat1	Battery supply voltage VBAT1-AVS		2.0		5.0	V
Vbat2	Battery supply voltage VBAT2-AVS		2.8		5.0	V
Vdd	Digital core supply voltage VDD-VSS	Note ²	1.75	1.8	1.98	V
Avd	Analog core supply voltage AVD-AVS	Note ²	1.75	1.8	1.98	V
Avd2	Analog core supply voltage AVD2-AVS	Note ²	1.75	1.8	1.98	V
Vddrf	Analog xtal and RFCLK supply voltage VDDRF-VSSRF	Note ²	1.75	1.8	1.98	V
Vddiof	Digital I/O supply voltage VDDIO-VSS for devices with FLASH		2.5	2.65	2.8	V
Vddio	Digital I/O supply voltage VDDIO-VSS for devices without FLASH		1.75		3.3	V
Vdcs	Voltage on DC_Sense pin				2.0	V
Vpon	Voltage on PON	All states ³			2.8	V
Vcharge	Voltage on CHARGE	All states ³			2.8	V
Vbat3	Voltage on VBAT3	Note ³			2.8	V
Vadc1	Voltage on ADC1	Note ³			2.8	V
Vprot_mic	Voltage on pins MICn, CIDp/n if protection enabled	Note ⁴	0.4		1.4	V
Iprotpon	Current through protection circuit of PON pin.	Note ³			0.5	mA
Iprotcharge	Current through protection circuit of CHARGE pin.	Note ³			0.5	mA
Iprotvbat3	Current through protection circuit of VBAT3/RINGING pin.	Note ³			0.5	mA
Iprotadc1	Current through protection circuit of ADC1 pin.	Note ³			0.5	mA
Vldo1_ctrl	Voltage on LDO1_CTRL				5.0	V
Vldo2_ctrl	Maximum voltage on LDO2_CTRL				5.0	V
Fpll_range	PLL operating range		28		48	MHz
TA	Ambient temperature	Note ⁵	-10		60	°C

1. Within the specified limits, a life time of 10 years is guaranteed.

2. Full operating mode; the differences between AVD, VDD may never be more than 300mV; during a short period of time e.g. during power up more than 300mV difference is allowed. Analog performance is only guaranteed from 1.75-1.98V

3. The protection current can be calculated as follows:

In case P1[6]/PON, P1[7]/CHARGE, VBAT3, P2[3]/ADC1 is input,

$$I_{protxxx_max} = (V_{ext} - 2.55) / (500 + R_{ext})$$

R_{ext} is an external resistor which is needed if the external voltage V_{ext} exceeds the 2.8V.

(A lower protection current value of e.g. 100 uA is recommended in case power saving is important)

In case P1[6]/PON, P1[7]/CHARGE, P2[3]/ADC1 is output, $I_{protxxx_max} = (V_{DDIO} - 2.55) / (500)$

4. For pads with the protection circuit enabled, the protection current **must** be limited with external source resistor R_{ext} if the input voltage exceeds 0.4V resp 1.4V. R_{ext} can be calculated as follows:

$$R_{ext} > (V_{ext} - 1.4) / I_{protxxx}$$

5. Within this temperature range full operation is guaranteed. Upto +70 degrees Celsius analog performance is not guaranteed.

5.0 Product Status Definitions

Datasheet Status	Product Status	Definition
Advance Information	Formative or in Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data. Supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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7.0 Package information inches (millimeters) unless otherwise noted

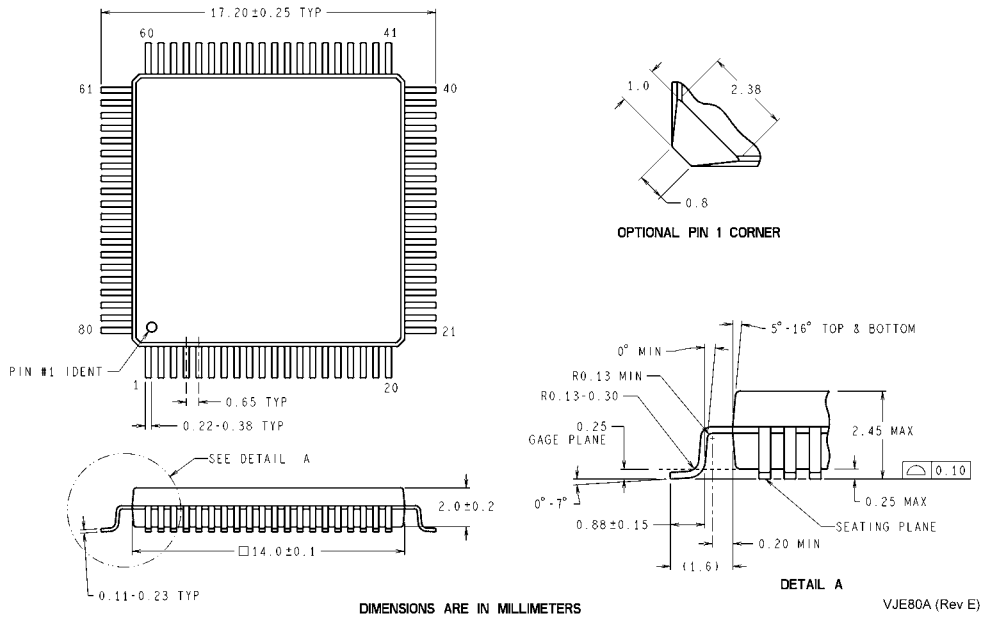


Figure 2. 80 Pins PQFP. NS Package number: VJE80A

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