

74F373 Octal Transparent Latch with 3-STATE Outputs

General Description

The 74F373 consists of eight latches with 3-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

Features

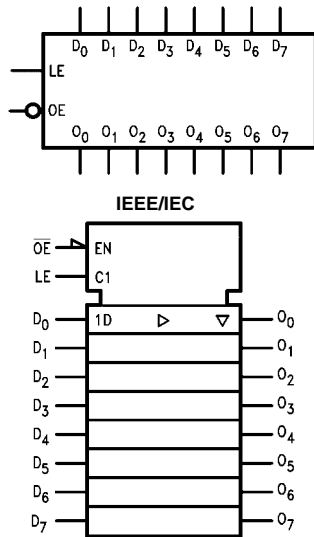
- Eight latches in a single package
- 3-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

Ordering Code:

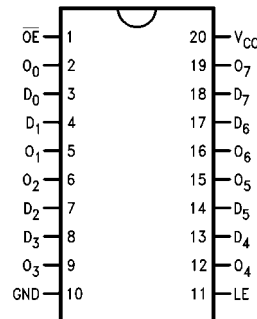
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74F373SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74F373SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F373MSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide |
| 74F373PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
|-----------------|----------------------------------|------------------|---|
| D_0 – D_7 | Data Inputs | 1.0/1.0 | 20 μ A/–0.6 mA |
| LE | Latch Enable Input (Active HIGH) | 1.0/1.0 | 20 μ A/–0.6 mA |
| \overline{OE} | Output Enable Input (Active LOW) | 1.0/1.0 | 20 μ A/–0.6 mA |
| O_0 – O_7 | 3-STATE Latch Outputs | 150/40 (33.3) | –3 mA/24 mA (20 mA) |

Functional Description

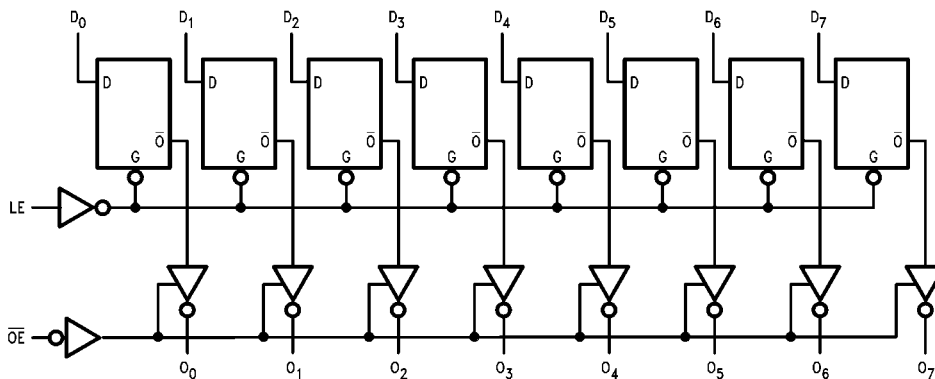
The 74F373 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

| Inputs | | | Output |
|--------|-----------------|-------|-------------------|
| LE | \overline{OE} | D_n | O_n |
| H | L | H | H |
| H | L | L | L |
| L | L | X | O_n (no change) |
| X | H | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance State

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

| | |
|--|--------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|---------------------|-----|-------------------------|-------|-----------------|--|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 10% V _{CC} | 2.5 | | V | Min | I _{OH} = -1 mA |
| | | 10% V _{CC} | 2.4 | I _{OH} = -3 mA | | | |
| | | 5% V _{CC} | 2.7 | I _{OH} = -1 mA | | | |
| | | 5% V _{CC} | 2.7 | I _{OH} = -3 mA | | | |
| V _{OL} | Output LOW Voltage | 10% V _{CC} | | 0.5 | V | Min | I _{OL} = 24 mA |
| I _{IH} | Input HIGH Current | | | 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BV1} | Input HIGH Current Breakdown Test | | | 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEx} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | -0.6 | mA | Max | V _{IN} = 0.5V |
| I _{OZH} | Output Leakage Current | | | 50 | μA | Max | V _{OUT} = 2.7V |
| I _{OZL} | Output Leakage Current | | | -50 | μA | Max | V _{OUT} = 0.5V |
| I _{OS} | Output Short-Circuit Current | -60 | | -150 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | | 500 | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCZ} | Power Supply Current | | 38 | 55 | mA | Max | V _O = HIGH Z |

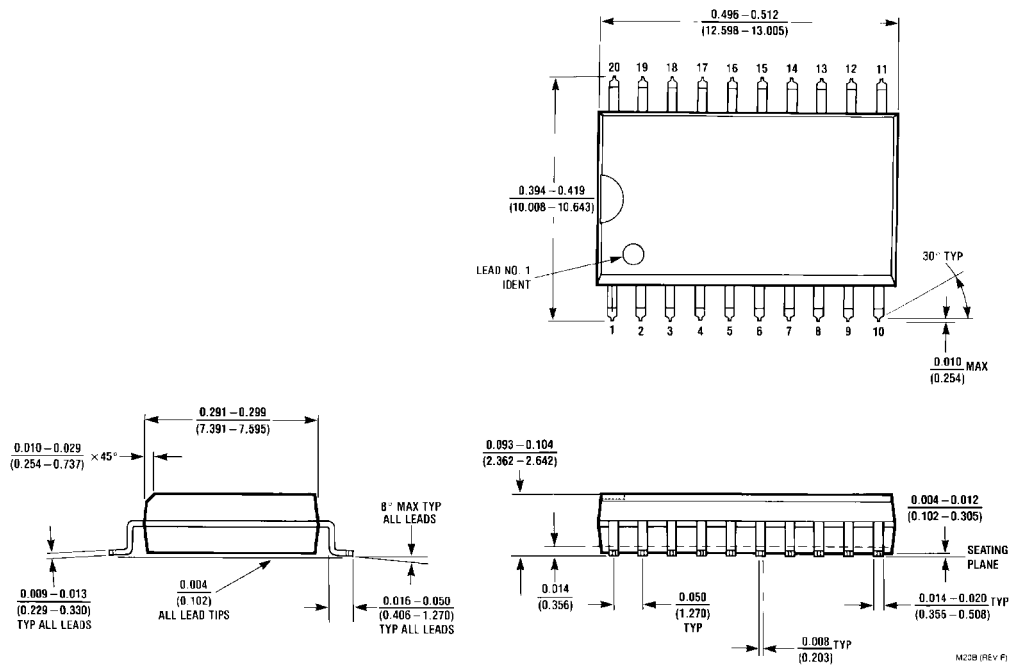
AC Electrical Characteristics

| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
|------------------|----------------------------------|---|-----|------|---|------|--|------|-------|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 3.0 | 5.3 | 7.0 | 3.0 | 8.5 | 3.0 | 8.0 | ns |
| t _{PHL} | D _n to O _n | 2.0 | 3.7 | 5.0 | 2.0 | 7.0 | 2.0 | 6.0 | |
| t _{PLH} | Propagation Delay | 5.0 | 9.0 | 11.5 | 5.0 | 15.0 | 5.0 | 13.0 | ns |
| t _{PHL} | LE to O _n | 3.0 | 5.2 | 7.0 | 3.0 | 8.5 | 3.0 | 8.0 | |
| t _{PZH} | Output Enable Time | 2.0 | 5.0 | 11.0 | 2.0 | 13.5 | 2.0 | 12.0 | ns |
| t _{PZL} | | 2.0 | 5.6 | 7.5 | 2.0 | 10.0 | 2.0 | 8.5 | |
| t _{PHZ} | Output Disable Time | 1.5 | 4.5 | 6.5 | 1.5 | 10.0 | 1.5 | 7.5 | ns |
| t _{PLZ} | | 1.5 | 3.8 | 5.0 | 1.5 | 7.0 | 1.5 | 6.0 | |

AC Operating Requirements

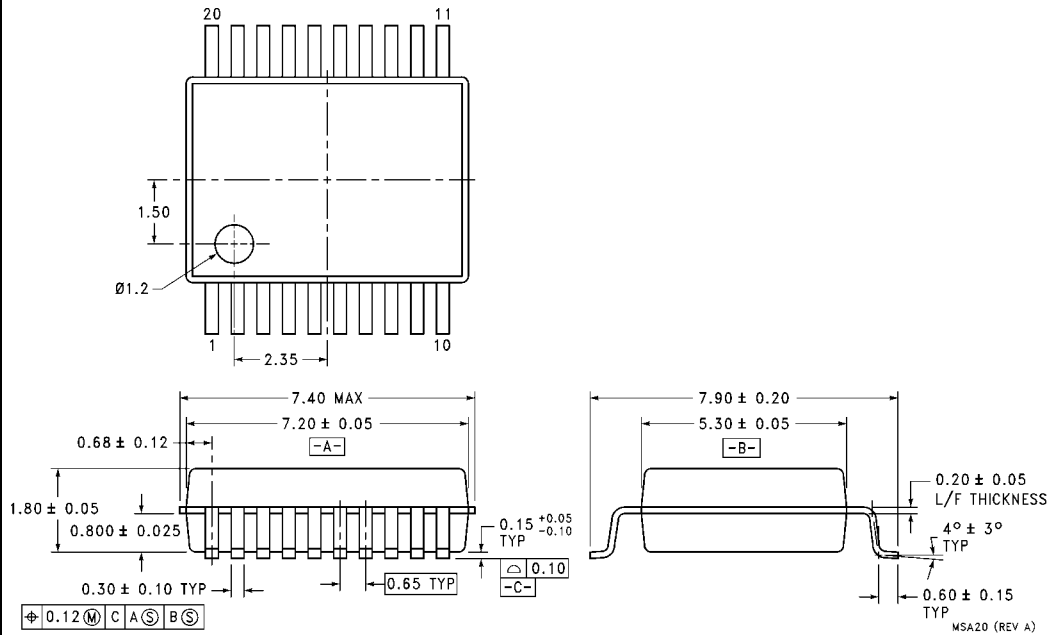
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V | | T _A = -55°C to +125°C V _{CC} = +5.0V | | T _A = 0°C to +70°C V _{CC} = +5.0V | | Units |
|--------------------|-------------------------|---|-----|---|-----|--|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| t _S (H) | Setup Time, HIGH or LOW | 2.0 | | 2.0 | | 2.0 | | ns |
| t _S (L) | D _n to LE | 2.0 | | 2.0 | | 2.0 | | |
| t _H (H) | Hold Time, HIGH or LOW | 3.0 | | 3.0 | | 3.0 | | ns |
| t _H (L) | D _n to LE | 3.0 | | 4.0 | | 3.0 | | |
| t _W (H) | LE Pulse Width, HIGH | 6.0 | | 6.0 | | 6.0 | | ns |

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20**

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