

DAVICOM Semiconductor, Inc.

DM8203

**10/100 Mbps 3-port Ethernet Switch Controller
with MII / RMII Interface**

DATASHEET

***Preliminary Datasheet
Version: DM8203-DS-P08
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1. General Description

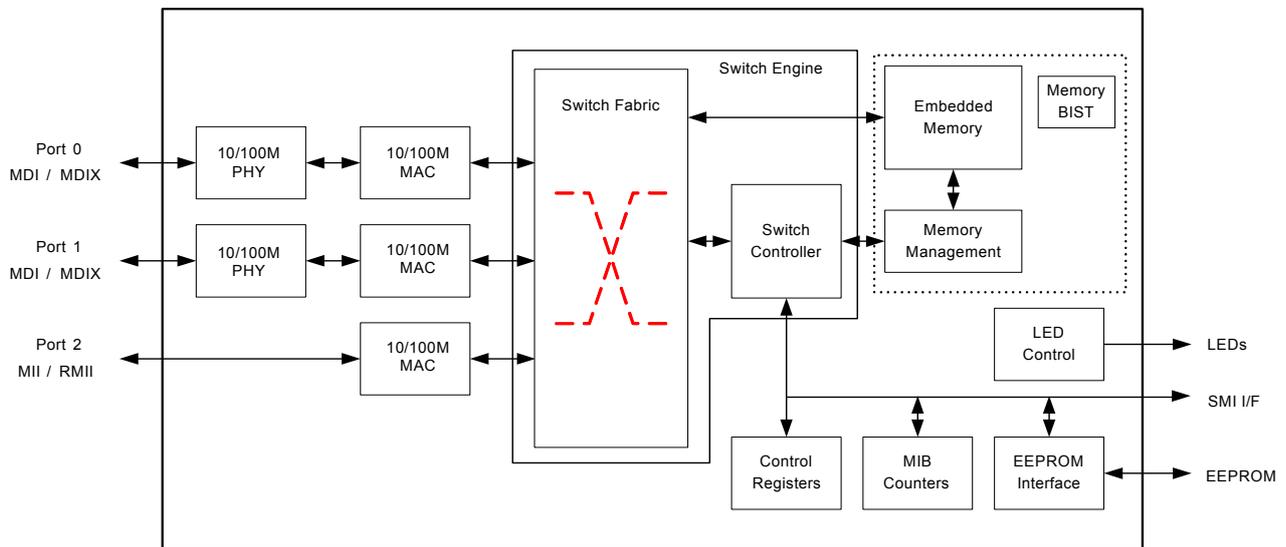
The DM8203 is Davicom’s new fully integrated three-port 10M/100Mbps Fast Ethernet Controller. As a fast Ethernet switch, the DM8203 consists of two PHY ports with 100M Fiber (PECL) interface and a third port with either MII or RMIi interface. As the DM8203 was designed with our customers’ requirements in mind, the switch is optimized for high performance while being highly cost-effective.

The two PHY ports on the DM8203 are IEEE 802.3u standards compliant. Aside for the first two PHY ports and in an effort for maximum application flexibility, the third port on the DM8203 offers the options to either connect with an MII, reversed MII, or RMIi. The reversed MII configuration is used to connect with SoC’s with a MII interface. The RMIi interface is the alternative interface configuration in case of the need to connect a lower pin count Ethernet PHY or SoC.

To maximize the performance of each port, the DM8203 was designed with a number of features. For proper bandwidth, each port also supports ingress and/or egress rate control. In support of efficient packet forwarding, the DM8203 has port-based VLAN with tag/un-tag functions for up to 16 groups of 802.1Q. Each port includes MIB counters, loop-back capability, built in memory self test (BIST) for the system, and board level diagnostic.

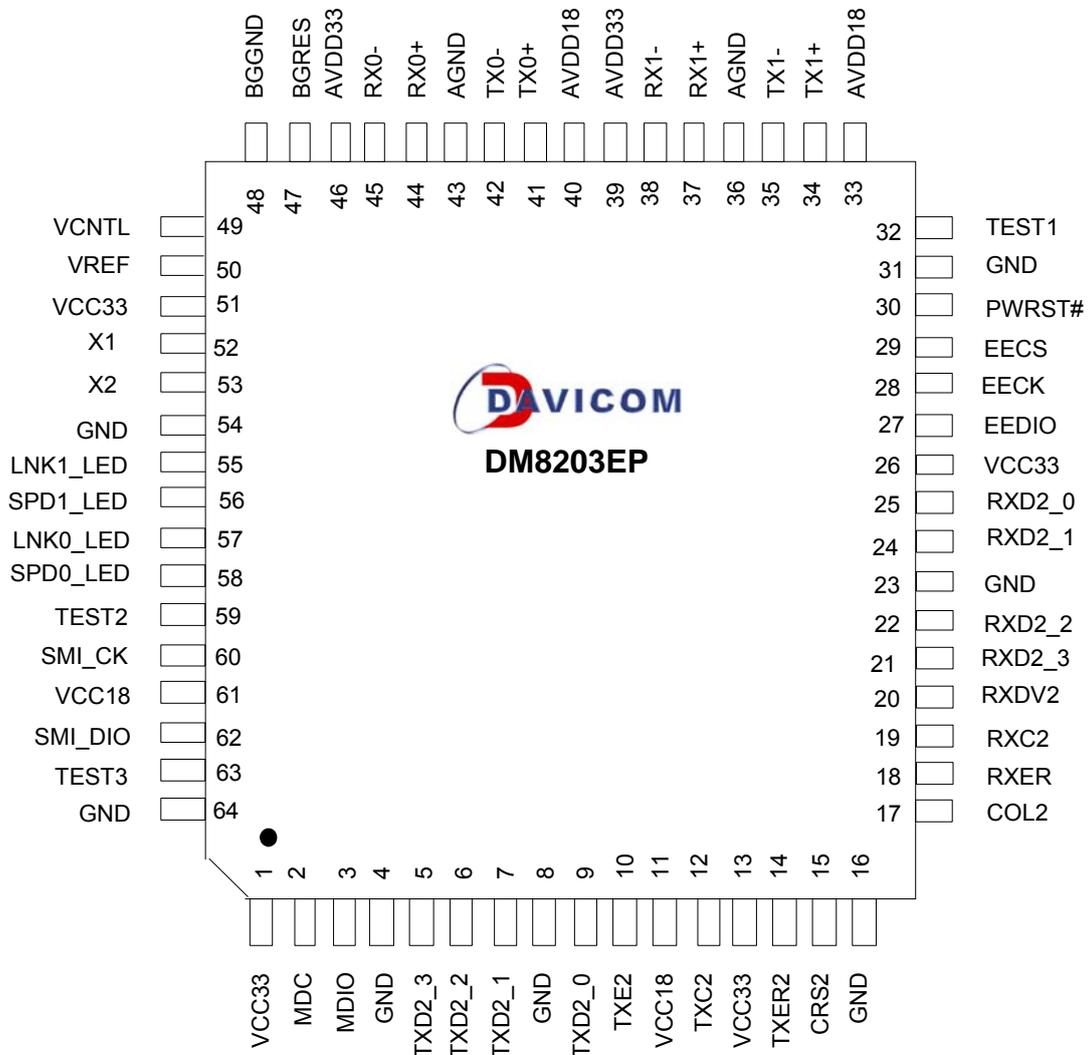
In designing for the requirements of various data, voice, and video applications, enough internal memory has been provided for usage of the DM8203’s three ports, and the internal memory supports up to 1K uni-cast MAC address table. Then to meet the demands of various bandwidth and latency issues in data, voice, and video applications, each port of the DM8203 has four priority transmit queues. These queues can be defined either through port-based operation, 802.1p VLAN, or the IP packet TOS field automatically.

2. Block Diagram



3. Features

- IEEE 802.3/u 10Base-T/100Base-TX compatible
- Ethernet Switch Ports:
 - Two 10/100Mbps PHY
 - One MII/RMI interface with Reversed - MII support
- Supports auto crossover function - HP Auto-MDIX
- Flow Control
 - Supports IEEE 802.3x Flow Control in Full-duplex mode
 - Supports Back Pressure Flow Control in Half-duplex mode
- Per port support bandwidth, ingress and egress rate control
- Per port support priority queues
 - Each port with four queues
 - Port-based, 802.1P VLAN, or IP TOS priority
 - Supports 802.1Q VLAN for up-to 16 VLAN groups
- Supports VLAN ID tag/untag options
- Supports up-to 1K Uni-cast MAC addresses
- Supports store and forward switching approach
- Supports Broadcast Storming filter function
- Supports Serial Data Management Interface
- Automatic aging scheme
- Supports MIB counters for diagnostic
- Supports 100M Fiber (PECL) interface
- EEPROM Interface
 - Power up configurations
 - 93C46 or 93C56 auto detection
- Package
 - 64-pin LQFP
- Power
 - 1.8V/3.3V Dual Power
 - 3.3V I/O with 5V tolerance

4. Pin Configuration
64 pin LQFP:


5. Pin Description

I = Input, O = Output, I/O = Input / Output, O/D = Open Drain, P = Power,
 # = Asserted Low PD=internal pull-low (about 50K Ohm)

5.1 P2 MII / Reduce MII / Reverse MII Interfaces
5.1.1 MII Interface

Pin No.	Pin Name	I/O	Description
2	MDC	O,PD	MI I Serial Management Data Clock
3	MDIO	I/O, PD	MI I Serial Management Data
5,6,7,9	TXD2_3~0	O,PD	Port 2 MI I Transmit Data 4-bit nibble data outputs (synchronous to the TXC2)
10	TXE2	O,PD	Port 2 MI I Transmit Enable
12	TXC2	I	Port 2 MI I Transmit Clock
14	TXER2	O,PD	Port 2 MI I Transmit Error
15	CRS2	I	Port 2 MI I Carrier Sense
17	COL2	I	Port 2 MI I Collision Detect
18	RXER2	I	Port 2 MI I Receive Error
19	RXC2	I	Port 2 MI I Receive Clock
20	RXDV2	I	Port 2 MI I Receive Data Valid
21,22,24,25	RXD2_3~0	I	Port 2 MI I Receive Data 4-bit nibble data input (synchronous to RXC2)

5.1.2 Reduce MII Interface

Pin No.	Pin Name	I/O	Description
2	MDC	O,PD	MI I Serial Management Data Clock
3	MDIO	I/O, PD	MI I Serial Management Data
5,6	TXD2_3~2	O,PD	Reserved
7,9	TXD2_1~0	O,PD	RMII Transmit Data
10	TXE2	O,PD	RMII Transmit Enable.
12	TXC2	O	Output 50MHz Clock
14	TXER2	O, PD	Port 2 MI I Transmit Error
15	CRS2	I	RMII CRS_DV
17	COL2	I	Reserved
18	RXER2	I	Reserved
19	RXC2	I	50MHz Reference Clock
20	RXDV2	I	Reserved
21,22	RXD2_3~2	I	Reserved
24,25	RXD2_1~0	I	RMII Receive Data

5.1.3 Reverse MII Interface

Pin No.	Pin Name	I/O	Description
2	MDC	O,PD	Reserved
3	MDIO	I/O, PD	Reserved
5,6,7,9	TXD2_3~0	O,PD	Port 2 MII Transmit Data 4-bit nibble data outputs (synchronous to the TXC2)
10	TXE2	O,PD	Port 2 MII Transmit Enable
12	TXC2	O	25MHz Clock Output
14	TXER2	O,PD	Port 2 MII Transmit Error
15	CRS2	O	Port 2 MII Carrier Sense Output when TXE2 or RXDV2 are asserted
17	COL2	O	Port 2 MII Collision Output when TXE2 and RXDV2 are asserted
18	RXER2	I	Port 2 MII Receive Error
19	RXC2	I	Port 2 MII Receive Clock
20	RXDV2	I	Port 2 MII Receive Data Valid
21,22,24,25	RXD2_3~0	I	Port 2 MII Receive Data 4-bit nibble data input (synchronous to RXC2)

5.2 EEPROM Interface

Pin No.	Pin Name	I/O	Description
27	EEDIO	I/O, PD	EEPROM Data In/Out
28	EECK	O,PD	EEPROM Serial Clock This pin is used as the clock for the EEPROM data transfer
29	EECS	O,PD	EEPROM Chip Selection

5.3 LED Pins

Pin No.	Pin Name	I/O	Description
55	LNK1_LED	O	Port 1 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY1
56	SPD1_LED	O	Port 1 Speed LED Its low output indicates that the internal PHY1 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY1
57	LNK0_LED	O	Port 0 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY0
58	SPD0_LED	O	Port 0 Speed LED Its low output indicates that the internal PHY0 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY0

5.4 Clock Interface

Pin No.	Pin Name	I/O	Description
52	X1	I	Crystal 25MHz In
53	X2	O	Crystal 25MHz Out

5.5 Network Interface

Pin No.	Pin Name	I/O	Description
34,35	TX1+/-	I/O	Port 1 TP TX/PECL These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode
37,38	RX1+/-	I/O	Port 1 TP RX/PECL These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode
41,42	TX0+/-	I/O	Port 0 TP TX/PECL These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode
44,45	RX0+/-	I/O	Port 0 TP RX/PECL These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode
47	BGRES	I/O	Band-Gap Pin Connect a 6.8K resistor to BGGND in application
48	BGGND	P	Band-Gap Ground
49	VCNTL	I/O	1.8V Voltage Control
50	VREF	O	Voltage Reference Connect a 0.1u capacitor to ground in application

5.6 Miscellaneous Pins

Pin No.	Pin Name	I/O	Description
30	PWRST#	I	Power on Reset Low active with minimum 1ms
60	SMI_CK	I	Serial Data Management Interface Clock
62	SMI_DIO	I/O, PD	Serial Data Management Interface Data In/Out
32	TEST1	I,PD	Test Pin 1 Tie to VCC33 in application
59	TEST2	I, PD	Test Pin 2 Tie to GND in application
63	TEST3	I, PD	Test Pin 3 Tie to VCC33 in application

5.7 Power Pins

Pin No.	Pin Name	I/O	Description
1,13,26,51	VCC33	P	Digital 3.3V
11,61	VCC18	P	Internal 1.8V Core Power
4,8,16,23,31,54,64	GND	P	Digital GND
39,46	AVDD33	P	Analog 3.3V Power
33,40	AVDD18	P	Analog 1.8V Power
36,43	AGND	P	Analog GND

5.8 Strap Pins Table

Pin No.	Pin Name	Description															
28	EECK	Port 2 Speed Selection in Force Mode 0: Port 2 is 10 Mbps in force mode 1: Port 2 is 100 Mbps in force mode															
29	EECS	Port 0 Fiber Mode Enable 0: Port 0 is TP mode 1: Port 0 is Fiber mode															
14	TXER2	Port 1 Fiber Mode Enable 0: Port 1 is TP mode 1: Port 1 is Fiber mode															
2	MDC	Memory BIST Bypass Enable 0: Enable BIST 1: Bypass BIST															
5	TXD2_3	P2 Mode Configuration <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>TXD2_3</th> <th>TXD2_2</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Port 2 MII mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>Port 2 Reverse MII mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>Port 2 RMI mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reverse</td> </tr> </tbody> </table>	TXD2_3	TXD2_2		0	0	Port 2 MII mode	0	1	Port 2 Reverse MII mode	1	0	Port 2 RMI mode	1	1	Reverse
TXD2_3	TXD2_2																
0	0		Port 2 MII mode														
0	1		Port 2 Reverse MII mode														
1	0	Port 2 RMI mode															
1	1	Reverse															
6	TXD2_2																
7,9	TXD2_1,0	SMI Device Address Configuration <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>TXD2_1</th> <th>TXD2_0</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Device address = 0</td> </tr> <tr> <td>0</td> <td>1</td> <td>Device address = 1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Device address = 2</td> </tr> <tr> <td>1</td> <td>1</td> <td>Device address = 3</td> </tr> </tbody> </table>	TXD2_1	TXD2_0		0	0	Device address = 0	0	1	Device address = 1	1	0	Device address = 2	1	1	Device address = 3
TXD2_1	TXD2_0																
0	0		Device address = 0														
0	1		Device address = 1														
1	0	Device address = 2															
1	1	Device address = 3															
10	TXE2	Port 2 Force Mode Enable 0: Port 2 is normal mode 1: Port 2 is force mode															

Note: 1: pull-high 1K~10K, 0: floating (default).

6. Control and Status Register Set

The DM8203 implements several control and status registers, which can be accessed by the serial management interface. These CSRs are byte aligned. All CSRs are set to their default values by hardware or software reset unless specified

Register	Description	Offset	Default value after reset
ECR	EEPROM Control Register	0Ah	00h
EPCR	EEPROM & PHY Control Register	0Bh	00h
EPAR	EEPROM & PHY Address Register	0Ch	00h
EPDRL	EEPROM & PHY Low Byte Data Register	0Dh	00h
EPDRH	EEPROM & PHY High Byte Data Register	0Eh	00h
VID	Vendor ID	28h~29h	0A46h
PID	Product ID	2Ah~2Bh	8203h
SMI_CNTRL	Serial Bus Err Control Register	36h	00h
SMI_STATUS	Serial Bus Status Check Register	37h	00h
P2FRV	Port 2 driving capability Register	3Ah	20h
P2_CNTRL	Port 2 MAC Control	3Bh	–
PHY_CTL	PHY Control	3Ch	00h
MONIR1	Monitor Register 1	41h	–
MONIR2	Monitor Register 2	42h	–
SWITCHCR1	SWITCH Control Register 1	52h	00h
VLANCR 1	VLAN Control Register 1	53h	00h
SWITCHSR	SWITCH Status Register	54h	–
SWITCHCR2	SWITCH Control Register 2	55h	00h
VLANCR 2	VLAN Control Register 2	56h	00h
DSP1,2	DSP Control Register I,II	58h~59h	00h
P_INDEX	Per Port Control/Status Index Register	60h	00h
P_CTRL	Per Port Control Data Register	61h	00h
P_STUS	Per Port Status Data Register	62h	–
P_FORW1	Per Port Forward Register 1	63h	00h
P_FORW2	Per Port Forward Register 2	64h	00h
P_FORW3	Per Port Forward Register 3	65h	00h
P_RATE	Per Port Ingress and Egress Rate Register	66h	00h
P_BW	Per Port Bandwidth Control Register	67h	00h
P_UNICAST	Per Port Block Unicast Ports Register	68h	00h
P_MULTI	Per Port Block Multicast Ports Register	69h	00h
P_BCAST	Per Port Block Broadcast Ports Register	6Ah	00h
P_UNKNWN	Per Port Block Unknown Ports Register	6Bh	00h
P_PRI_VLAN	Per Port Priority & VLAN Control Register	6Ch	00h
P_PRI	Per Port Priority Queue Register	6Dh	00h
VLAN_TAGL	Per Port VLAN Tag Low Byte Register	6Eh	01h
VLAN_TAGH	Per Port VLAN Tag High Byte Register	6Fh	00h
P_MIB_IDX	Per Port MIB Counter Index Register	80h	00h
MIB_DAT	MIB Counter Data Register bit 0~7	81h	00h
MIB_DAT	MIB Counter Data Register bit 8~15	82h	00h
MIB_DAT	MIB Counter Data Register bit 16~23	83h	00h
MIB_DAT	MIB Counter Data Register bit 24~31	84h	00h
PVLAN	Port-based VLAN Mapping Table Registers	B0h~BFh	07h
TOS_MAP	TOS Priority Map Registers	C0h~CFh	00h~FFh
VLAN_MAP	VLAN Priority Map Registers	D0h~D1h	50h,FAh

Key to Default

In the register description that follows, the default column takes the form:

<Access Type>, <Reset Type>, <Default Value>

Where:

<Access Type>:

RO = Read only

RW = Read/Write

R/C = Read and Clear

RW/C1=Read/Write and Cleared by write 1

WO = Write only

Reserved bits should be written with 0

Reserved bits are undefined on read access

<Reset Type>

P = Default value from power on reset (Hardware reset)

S = Default value from software reset (Write bit 6 of Reg. 52H to 1)

E = Default value from EEPROM setting

T = Default value from strap pin

6.1 EEPROM Control Register (0Ah)

Bit	Name	ROM	Default	Description
7	RESERVED	—	RO, 0b	Reserved
6	EE_TYPE	—	RW, PS 0b	EEPROM Type Select This bit works after power-on EEPROM loading done. 0: 93C46(Default) 1: 93C56/66
5:0	RESERVED	—	RO, 0h	Reserved

6.2 EEPROM & PHY Control Register (0Bh)

Bit	Name	ROM	Default	Description
7	RESERVED	—	RO, 0b	Reserved
6	EE_TYPE	—	RO, PS 0b	EEPROM Type Status 0: 93C46(Default) 1: 93C56/66
5	REEP	—	RW, PS 0b	Reload EEPROM. Driver needs to clear it up after the operation completes
4	WEP	—	RW, PS 0b	Write EEPROM Enable
3	EPOS	—	RW, PS 0b	EEPROM or PHY Operation Select When reset, select EEPROM; when set, select PHY
2	ERPRR	—	RW, PS 0b	EEPROM Read or PHY Register Read Command. Driver needs to clear it up after the operation completes.
1	ERPRW	—	RW, PS 0b	EEPROM Write or PHY Register Write Command. Driver needs to clear it up after the operation completes.
0	ERRE	—	RO, PS 0b	EEPROM Access Status or PHY Access Status When set, it indicates that the EEPROM or PHY access is in progress

6.3 EEPROM & PHY Address Register (0Ch)

Bit	Name	ROM	Default	Description
7:6	PHY_ADR	—	RW, PS 0h	PHY Address bit 1 and 0; the PHY address bit [4:2] is force to 0.
5:0	EROA	—	RW, PS 0h	EEPROM Word Address or PHY Register Address

6.4 EEPROM & PHY Data Register (0Dh~0Eh)

Bit	Name	ROM	Default	Description
7:0	EE_PHY_L	—	RW, PS 00h	EEPROM or PHY Low Byte Data (0DH) This data is made to write/read low byte of word address defined in Reg.0CH to EEPROM or PHY
7:0	EE_PHY_H	—	RW, PS 00h	EEPROM or PHY High Byte Data (0EH) This data is made to write/read high byte of word address defined in Reg.0CH to EEPROM or PHY

6.5 Vendor ID Registers (28h~29h)

Bit	Name	ROM	Default	Description
7:0	VIDH	4h.[15:08]	RO, PE 0Ah	Vendor ID High Byte (29h)
7:0	VIDL	4h.[07:00]	RO, PE 46h	Vendor ID Low Byte (28h)

6.6 Product ID Registers (2Ah~2Bh)

Bit	Name	ROM	Default	Description
7:0	PIDH	5h.[15:08]	RO, PE 82h	Product ID High Byte (2Bh)
7:0	PIDL	5h.[07:00]	RO, PE 03h	Product ID Low Byte (2Ah)

6.7 Serial Bus Status Check Register (36h)

Bit	Name	ROM	Default	Description
7:0	SMI_CS	—	RW, PS 00h	SMI Bus Command Checksum for Error Check

6.8 Serial Bus Error Control Register (37h)

Bit	Name	ROM	Default	Description
7	SMI_ECE	—	RW, PS 0b	SMI Bus Error Check Enable 0: Disable 1: Enable
6:1	RESERVED	—	RO, 0h	Reserved
0	SMI_ERR	—	RO, PS 0b	SMI Bus Error Status 0: Checksum is correct 1: Checksum is incorrect

6.9 Port 2 Driving Capability Register (3Ah)

Bit	Name	ROM	Default	Description
7	RESERVED	—	RO, 0b	Reserved
6:5	P2_CURR	—	RW, P 01b	Port 2 TXD/TXE Current Driving/Sinking Capability 00: 2mA 01: 4mA (default) 10: 6mA 11: 8mA
4:0	RESERVED	—	RO, 0h	Reserved

6.10 Port 2 MAC Control Register (3Bh)

Bit	Name	ROM	Default	Description
7:4	RESERVED	—	RO, 0h	Reserved
3	P2_MODE	—	RW, PST 0b	Port2 status in auto-polling mode for MII/RevMII/RMII 0: Auto-polling mode 1: Force mode
2	P2_LINK	—	RW, PS 0b	When Port2 in force mode for MII/RevMII/RMII 0: Link ON 1: Link OFF
1	P2_DPX	—	RW, PS 0b	When Port2 in force mode for MII/RevMII/RMII 0: Full-duplex mode 1: Half-duplex mode
0	P2_SPEED	—	RW, PST 0b	When Port2 in force mode for MII/RevMII/RMII 0: 100M mode 1: 10M mode

6.11 PHY Control Register (3Ch)

Bit	Name	ROM	Default	Description
7	MDIX_DIS_P0	7h.[15]	RW, PSE 0b	Port0 Auto-MDIX Control 0: Auto_MDIX Enable 1: Auto_MDIX Disable
6	MDIX_DIS_P1	7h.[14]	RW, PSE 0b	Port1 Auto-MDIX Control 0: Auto_MDIX Enable 1: Auto_MDIX Disable
5:0	RESERVED	—	RO, 0h	Reserved

6.12 Monitor Strap pin & enable pin status Register 1 (41h)

Bit	Name	ROM	Default	Description
7	H_TEST3	—	RO, PT	Hard-strap TEST3
6	H_TEST2	—	RO, PT	Hard-strap TEST2
5	H_TEST1	—	RO, PT	Hard-strap TEST1
4	H_MDC	—	RO, PT	Hard-strap MDC
3	RESERVED	—	RO, 0b	Reserved
2	H_EECS	—	RO, PT	Hard-strap EECS
1	H_EECK	—	RO, PT	Hard-strap EECK
0	RESERVED	—	RO, 0b	Reserved

6.13 Monitor Strap pin & enable pin status Register 2 (42h)

Bit	Name	ROM	Default	Description
7:6	RESERVED	—	RO, 0h	Reserved
5	HS_TXER2	—	RW, PT	Hard-strap/Soft-strap TXER2
4	HS_TXE2	—	RW, PT	Hard-strap/Soft-strap TXE2
3	HS_TXD23	—	RW, PT	Hard-strap/Soft-strap TXD2_3
2	HS_TXD22	—	RW, PT	Hard-strap/Soft-strap TXD2_2
1	HS_TXD21	—	RW, PT	Hard-strap/Soft-strap TXD2_1
0	HS_TXD20	—	RW, PT	Hard-strap/Soft-strap TXD2_0

6.14 Switch Control Register 1 (52h)

Bit	Name	ROM	Default	Description
7	RESERVED	—	RO, 0b	Reserved
6	RST_SW	—	RW, P 0b	Reset Switch Core and auto clear after 10us
5	RST_ANLG	—	RW, P 0b	Reset Analog PHY Core and auto clear after 10us
4:3	SNF_PORT	11h.[4:3]	RW, PSE 00b	Sniffer Port Number Define the port number to act as the sniffer port 00: Port 0 01: Port 1 10: Port 2 11: Reserved
2	CRC_DIS	11h.[2]	RW, PSE 0b	CRC Checking Disable When set, the received CRC error packet also accepts to receive memory.
1:0	AGE	11h.[1:0]	RW, PSE 00b	Address Table Aging 00: no aging 01: 64 ± 32 sec 10: 128 ± 64 sec 11: 256 ± 128 sec

6.15 VLAN Control Register 1 (53h)

Bit	Name	ROM	Default	Description
7	TOS6	11h.[15]	RW, PSE 0b	Full IP ToS Field for Priority Queue 1: check most significant 6-bit of TOS 0: check most significant 3-bit only of TOS
6	RESERVED	—	RO, 0b	Reserved
5	UNICAST	11h.[13]	RW, PSE 0b	Unicast packet can across VLAN boundary
4	VIDFF	11h.[12]	RW, PSE 0b	Replace VIDFF If the received packet is a tagged VLAN with VID equal to "FFF", its VLAN field is replaced with VLAN tag defined in Reg. 6EH and 6FH.
3	VID1	11h.[11]	RW, PSE 0b	Replace VID01 If the received packet is a tagged VLAN with VID equal to "001", its VLAN field is replaced with VLAN tag defined in Reg. 6EH and 6FH.
2	VID0	11h.[10]	RW, PSE 0b	Replace VID0 If the received packet is a tagged VLAN with VID equal to "000", its VLAN field is replaced with VLAN tag defined in Reg. 6EH and 6FH.
1	PRI	11h.[09]	RW, PSE 0b	Replace priority field in the tag with value define in Reg 6FH bit 7~5.
0	VLAN	11h.[08]	RW, PSE 0b	VLAN mode enable 1: 802.1Q base VLAN mode enable 0: port-base VLAN only

6.16 Switch Status Register (54h)

Bit	Name	ROM	Default	Description
7:2	RESERVED	—	RO, 0h	Reserved
1	EACMEMST	—	RO, P	Top-Memory BIST Status 0: Pass 1: Fail
0	RXMEMST	—	RO, P	Packet-Memory BIST Status 0: Pass 1: Fail

6.17 Switch Control Register 2 (55h)

Bit	Name	ROM	Default	Description
7	RESERVED	—	RO, 0b	Reserved
6	FDX_FLOW	—	RW, PS 0b	Flow Control Option When set In full duplex mode, if link partner's flow control capability is disabled, the flow control of DM8203 corresponding port is also disabled. When this is "0", the flow control is controlled by register 61H bit 4.
5	LRN_PAUSE	—	RW, PS 0b	Learn PAUSE Frame 0: Disable (default) 1: Enable
4	LRN_VLAN	—	RW, PS 0b	Address Learning Consider VLAN Member 0: Address learning despite VLAN member (default) 1: Address learning is disable, if incoming port doesn't exist in its member set.
3	MIRR_PAIR	—	RW, PS 0b	Mirror RX/TX Pair Mode Enable 0: Disable (default) 1: Enable
2:0	RESERVED	—	RO, 0h	Reserved

6.18 VLAN Control Register 2 (56h)

Bit	Name	ROM	Default	Description
7	FIR_VIDFFF	—	RW, PS 0b	Drop Packet with VID==0xFFF Enable 0: Disable 1: Enable
6	FIR_CFI	—	RW, PS 0b	Drop Packet with Nonzero CFI Enable Drop incoming packet, if the CFI field is not equal to zero. 0: Disable 1: Enable
5:0	RESERVED	—	RO, 0h	Reserved

6.19 DSP PHY Control Register 1 (58h)

Bit	Name	ROM	Default	Description
7:0	DSP_CTL1	12h.[7:0]	RW, P 0h	DSP PHY Control Register 1

6.20 DSP PHY Control Register 2 (59h)

Bit	Name	ROM	Default	Description
7:0	DSP_CTL2	12h.[15:8]	RW, P 0h	DSP PHY Control Register 2

6.21 Per Port Control/Status Index Register (60h)

Bit	Name	ROM	Default	Description
7:2	RESERVED	—	RO, 0h	Reserved
1:0	INDEX	—	RW, PS 00b	Port index for register 61h~6Fh Write the port number to this register before write/read register 61h~6Fh

6.22 Per Port Control Data Register (61h)

Bit	Name	ROM	Default	Description
7	RESERVED	—	RO, 0b	Reserved
6	PARTI_EN	13h.[06] 15h.[06] 17h.[06]	RW, PSE 0b	Partition Detection Enable
5	NO_DIS_RX	13h.[05] 15h.[05] 17h.[05]	RW, PSE 0b	Not Discard RX Packets when Ingress Bandwidth Control When received packets bandwidth reach Ingress bandwidth threshold, the packets over the threshold are not discarded but with flow control.
4	FLOW_DIS	13h.[04] 15h.[04] 17h.[04]	RW, PSE 0b	Flow Control Disable Flow control in full duplex mode, or back pressure in half duplex mode enable 0: Enable 1: Disable
3	BANDWIDTH	13h.[03] 15h.[03] 17h.[03]	RW, PSE 0b	Bandwidth Control Mode 0: Control with Ingress and Egress separately, ref to REG 66h. 1: Control with Ingress or Egress, ref to REG 67h
2	BP_DIS	13h.[02] 15h.[02] 17h.[02]	RW, PSE 0b	Broadcast Packet Filter 0: Accept broadcast packets 1: Reject broadcast packets
1	MP_DIS	13h.[01] 15h.[01] 17h.[01]	RW, PSE 0b	Multicast Packet Filter 0: Accept multicast packets 1: Reject multicast packets
0	MP_STORM	13h.[00] 15h.[00] 17h.[00]	RW, PSE 0b	Broadcast Storm Control 0: Only broadcast packets storm are controlled 1: Multicast packets also same as broadcast storm control.

6.23 Per Port Status Data Register (62h)

Bit	Name	ROM	Default	Description
7:6	RESERVED	—	RO, 0h	Reserved
5	LP_FCS	—	RO	Link Partner Flow Control Enable Status
4:3	RESERVED	—	RO, 0h	Reserved
2	SPEED	—	RO	Port Speed Status 0: 10Mbps 1:100Mbps
1	FDX	—	RO	Port Duplex Status 0: Half-duplex 1: Full-duplex
0	LINK	—	RO	Port Link Status 0: Link Off 1: Link On

6.24 Per Port Forward Control Register 1 (63h)

Bit	Name	ROM	Default	Description
7	HOB_DIS	—	RW, PS 0b	Head-of-Line Blocking Prevent Control 0: Disable (Default) 1: Enable
6	DIS_PAUSE	—	RW, PS 0b	Maximum Pause Packet from Link Partner 0: always care pause packet from link partner(default) 1: pause packet by passed after 7 continued pause packet from link partner
5	STORM_UUP	—	RW, PS 0b	Storm Enable for Un-learned Unicast DMAC Packets 0: Disable 1: Enable
4	PAUSE_CO N	—	RW, PS 0b	Send PAUSE Continuously If buffer congestion occur on full duplex, switch will send PAUSE frames: 0: Up to 8-times(default) 1: Continuously until alleviation
3	RESERVED	—	RO, 0b	Reserved
2	FIR_UMDMA C	—	RW, PS 0b	Filter Packets with Un-learned Multicast DMAC 0: Disable 1: Enable
1	FIR_MSMAC	—	RW, PS 0b	Filter Packets with Multicast SMAC 0: Disable 1: Enable
0	FIR_UUDMA C	—	RW, PS 0b	Filter Packets with Un-learned Unicast DMAC 0: Disable 1: Enable

6.25 Per Port Forward Control Register 2 (64h)

Bit	Name	ROM	Default	Description
7:4	RESERVED	—	RO, 0h	Reserved
3:2	MAX_LEN	—	RW, PS 00b	Max Packet Length 00: 1536-bytes 01: 1552-bytes 10: 1800-bytes 11: 2032-bytes
1:0	RESERVED	—	RO, 00b	Reserved

6.26 Per Port Forward Control Register 3 (65h)

Bit	Name	ROM	Default	Description
7	LOOPBACK	—	RW, PS 0b	Loop-Back Mode The transmitted packet will be forward to this port itself.
6	MONI_TX	—	RW, PS 0b	TX Packet Monitored The transmitted packets are also forward to sniffer port.
5	MONI_RX	—	RW, PS 0b	RX Packet Monitored The received packets are also forward to sniffer port.
4	DIS_BMP	—	RW, PS 0b	Broad/Multicast Not Monitored The received broadcast or multicast packets are not forward to sniffer port.
3	UNPLUG_CLS	—	RW, PS 0b	Unplug Clear Address Enable Enable to automatically clear address record in address table after unplug 0: Disable, retaining address record (Default) 1: Enable, clearing address record
2	TX_DIS	—	RW, PS 0b	Packet Transmit Disabled All packets cannot be forward to this port.
1	RX_DIS	—	RW, PS 0b	Packet receive Disabled All received packets are discarded.
0	ADR_DIS	—	RW, PS 0b	Address Learning Disabled The Source Address (SA) field of packet is not learned to address table.

6.27 Per Port Ingress/Egress Control Register (66h)

Bit	Name	ROM	Default	Description
7:4	INGRESS	13h.[15:12] 15h.[15:12] 17h.[15:12]	RW, PSE 0000b	<p>Ingress Rate Control</p> <p>These bits define the bandwidth threshold that received packets over the threshold are discarded.</p> <p>0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps</p>
3:0	EGRESS	13h.[11:08] 15h.[11:08] 17h.[11:08]	RW, PSE 0000b	<p>Egress Rate Control</p> <p>These bits define the bandwidth threshold that transmitted packets over the threshold are discarded.</p> <p>0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps</p>

6.28 Bandwidth Control Setting Register (67h)

Bit	Name	ROM	Default	Description
7:4	BSTH	14h.[07:04] 16h.[07:04] 18h.[07:04]	RW, PSE 0000b	Broadcast Storm Threshold These bits define the bandwidth threshold that received broadcast packets over the threshold are discarded 0000: no broadcast storm control 0001: 8K packets/sec 0010: 16K packets/sec 0011: 64K packets/sec 0100: 5% 0101: 10% 0110: 20% 0111: 30% 1000: 40% 1001: 50% 1010: 60% 1011: 70% 1100: 80% 1101: 90% 111X: no broadcast storm control
3:0	BW CTRL	14h.[03:00] 16h.[03:00] 18h.[03:00]	RW, PSE 0000b	Received and Transmitted Bandwidth Control These bits define the bandwidth threshold that transmitted or received packets over the threshold are discarded 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps

6.29 Per Port Block Unicast Ports Control Register (68h)

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2:0	BLK_UP	—	RW, PS 000b	Ports of Unicast Packet Be Blocked The received unicast packets are not forward to the assigned ports. Note that the assigned port definition: bit 0 for port 0, bit 1 for port 1,

6.30 Per Port Block Multicast Ports Control Register (69h)

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2:0	BLK_MP	—	RW, PS 000b	Ports of Multicast Packet Be Blocked The received multicast packets are not forward to the assigned ports.

6.31 Per Port Block Broadcast Ports Control Register (6Ah)

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2:0	BLK_BP	—	RW, PS 000b	Ports of Broadcast Packet Be Blocked The received broadcast packets are not forward to the assigned ports.

6.32 Per Port Block Unknown Ports Control Register (6Bh)

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2:0	BLK_UKP	—	RW, PS 000b	Ports of Unknown Packet Be Blocked The packets with DA field not found in address table are not forward to the assigned ports.

6.33 Per Port Priority & VLAN Control Register (6Ch)

Bit	Name	ROM	Default	Description
7:6	RESERVED	—	RO, 00b	Reserved
5	FIR_VIPOINT	—	RW, PS 0b	Enable to Filter Packet with Incoming Port is Non-member in VLAN 0: Disable 1: Enable
4	NOTAG_IN	—	RW, PS 0b	Input Force No Tag Assume all received frame are untagged 0: Disable 1: Enable
3:2	RESERVED	—	RO, 00b	Reserved
1:0	VLAN_IAC	—	RW, PS 00b	VLAN Ingress Admit Only Control 00: Accept all frames 01: Accept VLAN-tagged frames only Untagged or priority tagged(VID=0) frames will be dropped 10: Accept untagged frames only 11: Accept frame's VID equal to ingress PVID

6.34 Per Port Priority Queue Control Register (6Dh)

Bit	Name	ROM	Default	Description
7	TAG_OUT	14h.[15] 16h.[15] 18h.[15]	RW, PSE 0b	Output Packet Tagging Enable The transmitted packets are containing VLAN tagged field.
6	PRI_DIS	14h.[14] 16h.[14] 18h.[14]	RW, PSE 0b	Priority Queue Disable Only one transmit queue is supported in this port.
5	WFQUE	14h.[13] 16h.[13] 18h.[13]	RW, PSE 0b	Weighted Fair Queuing 1: The priority weight for queue 3, 2, 1, and 0 is 8, 4, 2, and 1 respectively. 0: The queue 3 has the highest priority, and the next priorities are queue 2, 1, and 0 respectively.
4	TOS_PRI	14h.[12] 16h.[12] 18h.[12]	RW, PSE 0b	Priority ToS over VLAN If an IP packet with VLAN tag, the priority of this packet is decode from ToS field.
3	TOS_OFF	14h.[11] 16h.[11] 18h.[11]	RW, PSE 0b	ToS Priority Classification Disable The priority information from ToS field of IP packet is ignored.
2	PRI_OFF	14h.[10] 16h.[10] 18h.[10]	RW, PSE 0b	802.1 p Priority Classification Disable The priority information from VLAN tag field is ignored.
1:0	P_PRI	14h.[9:8] 16h.[9:8] 18h.[9:8]	RW, PSE 00b	Port Base priority The priority queue number in port base. 00: queue 0 01=queue 1 10=queue 2 11=queue 3

6.35 Per Port VLAN Tag Low Byte Register (6Eh)

Bit	Name	ROM	Default	Description
7:0	VID70	1Bh.[7:0] 1Ch.[7:0] 1Dh.[7:0]	RW, PSE 01h	VID[7:0]

6.36 Per Port VLAN Tag High Byte Register (6Fh)

Bit	Name	ROM	Default	Description
7:5	PRI	1Bh.[15:13] 1Ch.[15:13] 1Dh.[15:13]	RW, PSE 000b	Tag [15:13]
4	CFI	1Bh.[12] 1Ch.[12] 1Dh.[12]	RW, PSE 0b	Tag[12]
3:0	VID118	1Bh.[11:08] 1Ch.[11:08] 1Dh.[11:08]	RW, PSE 0000b	VID[11:8]

6.37 MIB Counters Port Index Register (80h)

Bit	Name	ROM	Default	Description
7	READY	—	RO, PS 0b	MIB counter data is ready When this register is written with INDEX data, this bit is cleared and the MIB counter reading is in progress. After end of read MIB counter, the MIB data is loaded into register 81H~84H, and this bit is set to indicate that the MIB data is ready.
6	MIB_DIS	—	RW, PS 0b	MIB Counter Disable 0: MIB counter is enabled 1: MIB counter is disabled
5	RESERVED	—	RO	Reserved
4:0	INDEX	—	RW, PS 0h	MIB counter index 0~9, each counter is 32-bit in Register 81h~84h. Write the MIB counter index to this register before read them.

6.38 MIB Counter Data Registers (81h~84h)

Bit	Name	ROM	Default	Description
81H	Counter0	—	RO, PS	Counter's data bit 7~0
82H	Counter1	—	RO, PS	Counter's data bit 15~8
83H	Counter2	—	RO, PS	Counter's data bit 23~16
84H	Counter3	—	RO, PS	Counter's data bit 31~24

MIB Counter (INDEX 00h): RX Byte Counter Register

MIB Counter (INDEX 01h): RX Uni-cast Packet Counter Register

MIB Counter (INDEX 02h): RX Multi-cast Packet Counter Register

MIB Counter (INDEX 03h): RX Discard Packet Counter Register

MIB Counter (INDEX 04h): RX Error Packet Counter Register

MIB Counter (INDEX 05h): TX Byte Counter Register

MIB Counter (INDEX 06h): TX Uni-cast Packet Counter Register

MIB Counter (INDEX 07h): TX Multi-cast Packet Counter Register

MIB Counter (INDEX 08h): TX Discard Packet Counter Register

MIB Counter (INDEX 09h): TX Error Packet Counter Register

6.39 VLAN Grouping Table Registers (B0h~BFh)

Define the port member in VLAN group

There are 16 VLAN group that defined in REG B0h~BFh.

Group 0 defined in REG B0h, and group 1 defined in REG B1h ... and so on.

B0h: VLAN 0 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	20h.[02]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	20h.[01]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	20h.[00]	RW, PSE 1b	Mapping to port 0

B1h: VLAN 1 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	20h.[10]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	20h.[09]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	20h.[08]	RW, PSE 1b	Mapping to port 0

B2h: VLAN 2 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	21h.[02]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	21h.[01]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	21h.[00]	RW, PSE 1b	Mapping to port 0

B3h: VLAN 3 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	21h.[10]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	21h.[09]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	21h.[08]	RW, PSE 1b	Mapping to port 0

B4h: VLAN 4 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	22h.[02]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	22h.[01]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	22h.[00]	RW, PSE 1b	Mapping to port 0

B5h: VLAN 5 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	22h.[10]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	22h.[09]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	22h.[08]	RW, PSE 1b	Mapping to port 0

B6h: VLAN 6 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	23h.[02]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	23h.[01]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	23h.[00]	RW, PSE 1b	Mapping to port 0

B7h: VLAN 7 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	23h.[10]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	23h.[09]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	23h.[08]	RW, PSE 1b	Mapping to port 0

B8h: VLAN 8 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	24h.[02]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	24h.[01]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	24h.[00]	RW, PSE 1b	Mapping to port 0

B9h: VLAN 9 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	24h.[10]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	24h.[09]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	24h.[08]	RW, PSE 1b	Mapping to port 0

BAh: VLAN 10 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	25h.[02]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	25h.[01]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	25h.[00]	RW, PSE 1b	Mapping to port 0

BBh: VLAN 11 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	25h.[10]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	25h.[09]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	25h.[08]	RW, PSE 1b	Mapping to port 0

BCh: VLAN 12 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	26h.[02]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	26h.[01]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	26h.[00]	RW, PSE 1b	Mapping to port 0

BDh: VLAN 13 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	26h.[10]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	26h.[09]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	26h.[08]	RW, PSE 1b	Mapping to port 0

BEh: VLAN 14 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	27h.[02]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	27h.[01]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	27h.[00]	RW, PSE 1b	Mapping to port 0

BFh: VLAN 15 Grouping

Bit	Name	ROM	Default	Description
7:3	RESERVED	—	RO, 0h	Reserved
2	PORT_P2	27h.[10]	RW, PSE 1b	Mapping to port 2
1	PORT_P1	27h.[09]	RW, PSE 1b	Mapping to port 1
0	PORT_P0	27h.[08]	RW, PSE 1b	Mapping to port 0

6.40 TOS Priority Map Registers (C0h~CFh)

Define the 6-bit or 3-bit of ToS field mapping to 2-bit priority queue number.

In 6-bit type, the REG 53h.[7] is "1", REG C0h.[1:0] define the mapping for ToS value 0, REG C0h.[3:2] define the mapping for ToS value 1, ... and so on, till REG CFh.[7:6] define ToS value 63.

In 3-bit type, REG C0h.[1:0] defines the mapping for ToS value 0, REG C0h.[3:2] defines the mapping for ToS value 1 ... and so on, and till REG C1h.[7:6] define ToS value 7.

C0h:

Bit	Name	ROM	Default	Description
7:6	TOS3	28h.[07:06]	RW, PSE 01b	If REG 53h.[7] = 1 :TOS[7:2]=03h, otherwise TOS[7:5]=03h
5:4	TOS2	28h.[05:04]	RW, PSE 01b	If REG 53h.[7] = 1 :TOS[7:2]=02h, otherwise TOS[7:5]=02h
3:2	TOS1	28h.[03:02]	RW, PSE 00b	If REG 53h.[7] = 1 :TOS[7:2]=01h, otherwise TOS[7:5]=01h
1:0	TOS0	28h.[01:00]	RW, PSE 00b	If REG 53h.[7] = 1 :TOS[7:2]=00h, otherwise TOS[7:5]=00h

C1h:

Bit	Name	ROM	Default	Description
7:6	TOS7	28h.[15:14]	RW, PSE 11b	If REG 53h.[7] = 1 :TOS[7:2]=07h, otherwise TOS[7:5]=07h
5:4	TOS6	28h.[13:12]	RW, PSE 11b	If REG 53h.[7] = 1 :TOS[7:2]=06h, otherwise TOS[7:5]=06h
3:2	TOS5	28h.[11:10]	RW, PSE 10b	If REG 53h.[7] = 1 :TOS[7:2]=05h, otherwise TOS[7:5]=05h
1:0	TOS4	28h.[09:08]	RW, PSE 10b	If REG 53h.[7] = 1 :TOS[7:2]=04h, otherwise TOS[7:5]=04h

C2h:

Bit	Name	ROM	Default	Description
7:6	TOSB	29h.[07:06]	RW, PSE 00b	If REG 53h.[7] = 1 :TOS[7:2]=0Bh
5:4	TOSA	29h.[05:04]	RW, PSE 00b	If REG 53h.[7] = 1 :TOS[7:2]=0Ah
3:2	TOS9	29h.[03:02]	RW, PSE 00b	If REG 53h.[7] = 1 :TOS[7:2]=09h
1:0	TOS8	29h.[01:00]	RW, PSE 00b	If REG 53h.[7] = 1 :TOS[7:2]=08h

C3h:

Bit	Name	ROM	Default	Description
7:6	TOSF	29h.[15:14]	RW, PSE 00b	If REG 53h.[7] =1 :TOS[7:2]=0Fh
5:4	TOSE	29h.[13:12]	RW, PSE 00b	If REG 53h.[7] =1 :TOS[7:2]=0Eh
3:2	TOSD	29h.[11:10]	RW, PSE 00b	If REG 53h.[7] =1 :TOS[7:2]=0Dh
1:0	TOSC	29h.[09:08]	RW, PSE 00b	If REG 53h.[7] =1 :TOS[7:2]=0Ch

C4h:

Bit	Name	ROM	Default	Description
7:6	TOS13	2Ah.[07:06]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=13h
5:4	TOS12	2Ah.[05:04]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=12h
3:2	TOS11	2Ah.[03:02]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=11h
1:0	TOS10	2Ah.[01:00]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=10h

C5h:

Bit	Name	ROM	Default	Description
7:6	TOS17	2Ah.[15:14]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=17h
5:4	TOS16	2Ah.[13:12]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=16h
3:2	TOS15	2Ah.[11:10]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=15h
1:0	TOS14	2Ah.[09:08]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=14h

C6h:

Bit	Name	ROM	Default	Description
7:6	TOS1B	2Bh.[07:06]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=1Bh
5:4	TOS1A	2Bh.[05:04]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=1Ah
3:2	TOS19	2Bh.[03:02]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=19h
1:0	TOS18	2Bh.[01:00]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=18h

C7h:

Bit	Name	ROM	Default	Description
7:6	TOS1F	2Bh.[15:14]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=1Fh
5:4	TOS1E	2Bh.[13:12]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=1Eh
3:2	TOS1D	2Bh.[11:10]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=1Dh
1:0	TOS1C	2Bh.[09:08]	RW, PSE 01b	If REG 53h.[7] =1 :TOS[7:2]=1Ch

C8h:

Bit	Name	ROM	Default	Description
7:6	TOS23	2Ch.[07:06]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=23h
5:4	TOS22	2Ch.[05:04]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=22h
3:2	TOS21	2Ch.[03:02]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=21h
1:0	TOS20	2Ch.[01:00]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=20h

C9h:

Bit	Name	ROM	Default	Description
7:6	TOS27	2Ch.[15:14]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=27h
5:4	TOS26	2Ch.[13:12]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=26h
3:2	TOS25	2Ch.[11:10]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=25h
1:0	TOS24	2Ch.[09:08]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=24h

CAh:

Bit	Name	ROM	Default	Description
7:6	TOS2B	2Dh.[07:06]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=2Bh
5:4	TOS2A	2Dh.[05:04]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=2Ah
3:2	TOS29	2Dh.[03:02]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=29h
1:0	TOS28	2Dh.[01:00]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=28h

CBh:

Bit	Name	ROM	Default	Description
7:6	TOS2F	2Dh.[15:14]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=2Fh
5:4	TOS2E	2Dh.[13:12]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=2Eh
3:2	TOS2D	2Dh.[11:10]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=2Dh
1:0	TOS2C	2Dh.[09:08]	RW, PSE 10b	If REG 53h.[7] =1 :TOS[7:2]=2Ch

CCH:

Bit	Name	ROM	Default	Description
7:6	TOS33	2Eh.[07:06]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=33h
5:4	TOS32	2Eh.[05:04]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=32h
3:2	TOS31	2Eh.[03:02]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=31h
1:0	TOS30	2Eh.[01:00]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=30h

CDh

Bit	Name	ROM	Default	Description
7:6	TOS37	2Eh.[15:14]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=37h
5:4	TOS36	2Eh.[13:12]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=36h
3:2	TOS35	2Eh.[11:10]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=35h
1:0	TOS34	2Eh.[09:08]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=34h

CEh:

Bit	Name	ROM	Default	Description
7:6	TOS3B	2Fh.[07:06]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=3Bh
5:4	TOS3A	2Fh.[05:04]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=3Ah
3:2	TOS39	2Fh.[03:02]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=39h
1:0	TOS38	2Fh.[01:00]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=38h

CFh:

Bit	Name	ROM	Default	Description
7:6	TOS3F	2Fh.[15:14]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=3Fh
5:4	TOS3E	2Fh.[13:12]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=3Eh
3:2	TOS3D	2Fh.[11:10]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=3Dh
1:0	TOS3C	2Fh.[09:08]	RW, PSE 11b	If REG 53h.[7] =1 :TOS[7:2]=3Ch

6.41 VLAN Priority Map Registers (D0h~D1h)

Define the 3-bit of priority field VALN mapping to 2-bit priority queue number.

D0h:

Bit	Name	ROM	Default	Description
7:6	TAG3	1Fh.[07:06]	RW , PSE 01b	VLAN priority tag value = 03h
5:4	TAG2	1Fh.[05:04]	RW , PSE 01b	VLAN priority tag value = 02h
3:2	TAG1	1Fh.[03:02]	RW , PSE 00b	VLAN priority tag value = 01h
1:0	TAG0	1Fh.[01:00]	RW , PSE 00b	VLAN priority tag value = 00h

D1h:

Bit	Name	ROM	Default	Description
7:6	TAG7	1Fh.[15:14]	RW , PSE 11b	VLAN priority tag value = 07h
5:4	TAG6	1Fh.[13:12]	RW , PSE 11b	VLAN priority tag value = 06h
3:2	TAG5	1Fh.[11:10]	RW , PSE 10b	VLAN priority tag value = 05h
1:0	TAG4	1Fh.[09:08]	RW , PSE 10b	VLAN priority tag value = 04h

7. EEPROM Format

Name	Word	Description
Signature	00h	When the value is 1049h, this word can be used to check EEPROM type automatically.
RESERVED	01h~02h	Reserved Set to "0000h" in application
Load Control 0	03h	Bit [01:00] = Load enable of word 04h & 05h 01b: Enable, 00b/10b/11b: Disable Bit [03:02] = Reserved Set to "00b" or "11b" in application Bit [05:04] = Reserved Set to "00b" or "11b" in application Bit [07:06] = Reserved Set to "00b" or "11b" in application Bit [09:08] = Reserved Set to "00b" or "11b" in application Bit [11:10] = Reserved Set to "00b" or "11b" in application Bit [13:12] = Reserved Set to "00b" or "11b" in application Bit [15:14] = Load enable of word 07h 01b: Enable, 00b/10b/11b: Disable
Vendor ID	04h	2 byte vendor ID (Default: 0A46h), If bit [1:0] of word 03h is "01b", Bit [07:00] will be loaded to REG 28h Bit [15:08] will be loaded to REG 29h
Product ID	05h	2 byte product ID (Default: 8203H), If bit [1:0] of word 03h is "01b", Bit [07:00] will be loaded to REG 2Ah Bit [15:08] will be loaded to REG 2Bh
RESERVED	06h	Reserved Set to "0000h" in application
PHY control	07h	PHY Auto-MDIX Control If bit [15:14] of word 03h is "01b", Bit [08:00] = Reserved Bit [13:09] = Reserved Bit [14] = Port 1 AUTO-MDIX control 1: ON, 0: OFF(default ON) Bit [15] = Port 0 AUTO-MDIX control 1: ON 0: OFF(default ON)
RESERVED	08h~0Fh	Reserved Set to "0000H" in application
Load Control 1	10h	Bit [01:00] = Load enable of word 11h ~ 12h 01b: Enable, 00b/10b/11b: Disable Bit [03:02] = Load enable of word 13h ~ 18h 01b: Enable, 00b/10b/11b: Disable Bit [05:04] = Load enable of word 1Bh ~ 1Dh 01b: Enable, 00b/10b/11b: Disable Bit [07:06] = Load enable of word 1Fh 01b: Enable, 00b/10b/11b: Disable Bit [09:08] = Load enable of word 20h ~ 27h 01b: Enable, 00b/10b/11b: Disable Bit [11:10] = Load enable of word 28h ~ 2Fh 01b: Enable, 00b/10b/11b: Disable

		Bit [13:12] = Reserved Set to "00b" or "11b" in application Bit [15:14] = Reserved Set to "00b" or "11b" in application
Switch Control 0	11h	If bit [01:00] of word 10h is "01b", Bit [07:00] will be loaded to REG 52h Bit [15:08] will be loaded to REG 53h
Switch Control 1	12h	If bit [01:00] of word 10h is "01b", Bit [07:00] will be loaded to REG 58h Bit [15:08] will be loaded to REG 59h
Port 0 Control 0	13h	If bit [03:02] of word 10h is "01b", Bit [07:00] will be loaded to REG 61h of Port 0 Bit [15:08] will be loaded to REG 66h of Port 0
Port 0 Control 1	14h	If bit [03:02] of word 10h is "01b", Bit [07:00] will be loaded to REG 67h of Port 0 Bit [15:08] will be loaded to REG 6Dh of Port 0
Port 1 Control 0	15h	If bit [03:02] of word 10h is "01b", Bit [07:00] will be loaded to REG 61h of Port 1 Bit [15:08] will be loaded to REG 66h of Port 1
Port 1 Control 1	16h	If bit [03:02] of word 10h is "01b", Bit [07:00] will be loaded to REG 67h of Port 1 Bit [15:08] will be loaded to REG 6Dh of Port 1
Port 2 Control 0	17h	If bit [03:02] of word 10h is "01b", Bit [07:00] will be loaded to REG 61h of Port 2 Bit [15:08] will be loaded to REG 66h of Port 2
Port 2 Control 1	18h	If bit [03:02] of word 10h is "01b", Bit [07:00] will be loaded to REG 67h of Port 2 Bit [15:08] will be loaded to REG 6Dh of Port 2
RESERVED	19h~1Ah	Reserved Set to "0000h" in application
Port 0 VLAN Tag	1Bh	If bit [05:04] of word 10h is "01b", Bit [07:00] will be loaded to REG 6Eh of Port 0 Bit [15:08] will be loaded to REG 6Fh of Port 0
Port 1 VLAN Tag	1Ch	If bit [05:04] of word 10h is "01b", Bit [07:00] will be loaded to REG 6Eh of Port 1 Bit [15:08] will be loaded to REG 6Fh of Port 1
Port 2 VLAN Tag	1Dh	If bit [05:04] of word 10h is "01b", Bit [07:00] will be loaded to REG 6Eh of Port 2 Bit [15:08] will be loaded to REG 6Fh of Port 2
	1Eh	Reserved
VLAN Priority Map	1Fh	If bit [07:06] of word 10h is "01b", Bit [07:00] will be loaded to REG D0h Bit [15:08] will be loaded to REG D1h
Port VLAN Group 0,1	20h	If bit [09:08] of word 10h is "01b", Bit [07:00] will be loaded to REG B0h Bit [15:08] will be loaded to REG B1h
Port VLAN Group 2,3	21h	If bit [09:08] of word 10h is "01b", Bit [07:00] will be loaded to REG B2h Bit [15:08] will be loaded to REG B3h
Port VLAN Group 4,5	22h	If bit [09:08] of word 10h is "01b", Bit [07:00] will be loaded to REG B4h Bit [15:08] will be loaded to REG B5h
Port VLAN Group 6,7	23h	If bit [09:08] of word 10h is "01b", Bit [07:00] will be loaded to REG B6h

		Bit [15:08] will be loaded to REG B7h
Port VLAN Group 8,9	24h	If bit [09:08] of word 10h is "01b", Bit [07:00] will be loaded to REG B8h Bit [15:08] will be loaded to REG B9h
Port VLAN Group 10,11	25h	If bit [09:08] of word 10h is "01b", Bit [07:00] will be loaded to REG BAh Bit [15:08] will be loaded to REG BBh
Port VLAN Group 12,13	26h	If bit [09:08] of word 10h is "01b", Bit [07:00] will be loaded to REG BCh Bit [15:08] will be loaded to REG BDh
Port VLAN Group 14,15	27h	If bit [09:08] of word 10h is "01b", Bit [07:00] will be loaded to REG BEh Bit [15:08] will be loaded to REG BFh
ToS Priority Map 0	28h	If bit [11:10] of word 10h is "01b", Bit [07:00] will be loaded to REG C0h Bit [15:08] will be loaded to REG C1h
ToS Priority Map 1	29h	If bit [11:10] of word 10h is "01b", Bit [07:00] will be loaded to REG C2h Bit [15:08] will be loaded to REG C3h
ToS Priority Map 2	2Ah	If bit [11:10] of word 10h is "01b", Bit [07:00] will be loaded to REG C4h Bit [15:08] will be loaded to REG C5h
ToS Priority Map 3	2Bh	If bit [11:10] of word 10h is "01b", Bit [07:00] will be loaded to REG C6h Bit [15:08] will be loaded to REG C7h
ToS Priority Map 4	2Ch	If bit [11:10] of word 10h is "01b", Bit [07:00] will be loaded to REG C8h Bit [15:08] will be loaded to REG C9h
ToS Priority Map 5	2Dh	If bit [11:10] of word 10h is "01b", Bit [07:00] will be loaded to REG CAh Bit [15:08] will be loaded to REG CBh
ToS Priority Map 6	2Eh	If bit [11:10] of word 10h is "01b", Bit [07:00] will be loaded to REG CCh Bit [15:08] will be loaded to REG CDh
ToS Priority Map 7	2Fh	If bit [11:10] of word 10h is "01b", Bit [07:00] will be loaded to REG CEh Bit [15:08] will be loaded to REG CFh

8. PHY Registers

MII Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00h	CONTR OL	Reset	Loop back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved							
		0	0	1	1	0	0	0	1	0	000 0000							
01h	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.	
		0	1	1	1	1	0000				1	0	0	1	0	0	0	1
02h	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	
03h	PHYID2	1	0	1	1	1	0	Model No.					Version No.					
		01011 0000																
04h	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field					
05h	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field					
06h	Auto-Neg. Expansio n	Reserved										Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.		
14h	Specified config	Reversed				PREA MBLE X	TX10M_ PWR	NWAY_P WR	Reserved	MDIX_ CNTL	Reserv ed	Mdix_fixV alue	Mdix_do wn	Reserved				
1Dh	PSCR	Reversed				PREA MBLE X	Reversed	TX_PWR	Reversed									

Key to Default

In the register description that follows, the default column takes the form:

<Access Type> / <Attribute(s)>, <Reset Value>

Where:

<Access Type>

RO = Read only, RW = Read/Write

<Attribute (s)>

SC = Self clearing, P = Value permanently set

<Reset Value>:

1 = Bit set to logic one

0 = Bit set to logic zero

X = No default value

8.1 Basic Mode Control Register (BMCR) – 00h

Bit	Bit Name	Default	Description
15	Reset	RW/SC, 0b	Reset This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed 1 = Software reset 0 = Normal operation
14	Loopback	RW, 0b	Loopback Loop-back control register. When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MII receive outputs 1 = Loop-back enabled 0 = Normal operation
13	Speed selection	RW, 1b	Speed Select Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected medium type 1 = 100Mbps 0 = 10Mbps
12	Auto-negotiation enable	RW, 1b	Auto-negotiation Enable 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status 0 = Auto-negotiation is disabled.
11	Power down	RW, 0b	Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII 1 = Power down 0 = Normal operation
10	Isolate	RW, 0b	Isolate Force to 0 in application.
9	Restart Auto-negotiation	RW/SC, 0b	Restart Auto-negotiation Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning to a value of 1 until auto-negotiation is initiated by the DM8203. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 1 = Restart auto-negotiation. 0 = Normal operation
8	Duplex mode	RW, 1b	Duplex Mode Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 1 = Full duplex operation. 0 = Normal operation
7	Collision test	RW, 0b	Collision Test When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN in internal MII interface. 1 = Collision test enabled. 0 = Normal operation

6:0	RESERVED	RO, 0b	Reserved Read as 0, ignore on write
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8.2 Basic Mode Status Register (BMSR) – 01h

Bit	Bit Name	Default	Description
15	100BASE-T4	RO/P, 0b	100BASE-T4 Capable 1 = DM8203 is able to perform in 100BASE-T4 mode 0 = DM8203 is not able to perform in 100BASE-T4 mode
14	100BASE-TX full-duplex	RO/P, 1b	100BASE-TX Full Duplex Capable 1 = DM8203 is able to perform 100BASE-TX in full duplex mode 0 = DM8203 is not able to perform 100BASE-TX in full duplex mode
13	100BASE-TX half-duplex	RO/P, 1b	100BASE-TX Half Duplex Capable 1 = DM8203 is able to perform 100BASE-TX in half duplex mode 0 = DM8203 is not able to perform 100BASE-TX in half duplex mode
12	10BASE-T full-duplex	RO/P, 1b	10BASE-T Full Duplex Capable 1 = DM8203 is able to perform 10BASE-T in full duplex mode 0 = DM8203 is not able to perform 10BASE-TX in full duplex mode
11	10BASE-T half-duplex	RO/P, 1b	10BASE-T Half Duplex Capable 1 = DM8203 is able to perform 10BASE-T in half duplex mode 0 = DM8203 is not able to perform 10BASE-T in half duplex mode
10:7	RESERVED	RO, 0h	Reserved Read as 0, ignore on write
6	MF preamble suppression	RO, 1b	MII Frame Preamble Suppression 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
5	Auto-negotiation Complete	RO, 0b	Auto-negotiation Complete 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed
4	Remote fault	RO, 0b	Remote Fault 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM8203 implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected
3	Auto-negotiation ability	RO/P, 1b	Auto Configuration Ability 1 = DM8203 is able to perform auto-negotiation 0 = DM8203 is not able to perform auto-negotiation
2	Link status	RO, 0b	Link Status The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface. 1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established

1	Jabber detect	RO, 0b	Jabber Detect This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM8203 reset. This bit works only in 10Mbps mode 1 = Jabber condition detected 0 = No jabber
0	Extended capability	RO/P, 1b	Extended Capability 1 = Extended register capable 0 = Basic register capable only

8.3 PHY ID Identifier Register #1 (PHYID1) – 02h

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM8203. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
15:0	OUI_MSB	RO, 0181h	OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

8.4 PHY ID Identifier Register #2 (PHYID2) – 03h

Bit	Bit Name	Default	Description
15:10	OUI_LSB	RO/P 101110b	OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
9:4	VNDR_MDL	RO/P 001011b	Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3:0	MDL_REV	RO/P 0000b	Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4)

8.5 Auto-negotiation Advertisement Register (ANAR) – 04h

This register contains the advertised abilities of this DM8203 device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	RO/P, 0b	Next page Indication The DM8203 has no next page, so this bit is permanently set to 0. 0 = No next page available 1 = Next page available
14	ACK	RO, 0b	Acknowledge The DM8203's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit. 1 = Link partner ability data reception acknowledged 0 = Not acknowledged
13	RF	RW, 0b	Remote Fault 1 = Local device senses a fault condition 0 = No fault detected
12:11	RESERVED	RW, 00b	Reserved Write as 0, ignore on read
10	FCS	RW, 0b	Flow Control Support 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
9	T4	RO/P, 0b	100BASE-T4 Support The DM8203 does not support 100BASE-T4 so this bit is permanently set to 0 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported
8	TX_FDX	RW, 1b	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported
7	TX_HDX	RW, 1b	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the local device 0 = 100BASE-TX half duplex is not supported
6	10_FDX	RW, 1b	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the local device 0 = 10BASE-T full duplex is not supported
5	10_HDX	RW, 1b	10BASE-T Support 1 = 10BASE-T half duplex is supported by the local device 0 = 10BASE-T half duplex is not supported
4:0	Selector	RW, 1b	Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD

8.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 05h

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	RO, 0b	Next Page Indication 0 = Link partner, no next page available 1 = Link partner, next page available
14	ACK	RO, 0b	Acknowledge The DM8203's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit 1 = Link partner ability data reception acknowledged 0 = Not acknowledged
13	RF	RO, 0b	Remote Fault 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
12:11	RESERVED	RO, 00b	Reserved Read as 0, ignore on write
10	FCS	RO, 0b	Flow Control Support 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
9	T4	RO, 0b	100BASE-T4 Support 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
8	TX_FDX	RO, 0b	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner
7	TX_HDX	RO, 0b	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner
6	10_FDX	RO, 0b	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner
5	10_HDX	RO, 0b	10BASE-T Support 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner
4:0	Selector	RO, 0h	Protocol Selection Bits Link partner's binary encoded protocol selector

8.7 Auto-negotiation Expansion Register (ANER) - 06h

Bit	Bit Name	Default	Description
15:5	RESERVED	RO, 0h	Reserved Read as 0, ignore on write
4	PDF	RO/LH, 0b	Local Device Parallel Detection Fault 1 = A fault detected via parallel detection function. 0 = No fault detected via parallel detection function
3	LP_NP_ABLE	RO, 0b	Link Partner Next Page Ability 1 = Link partner, next page available 0 = Link partner, no next page
2	NP_ABLE	RO/P, 0b	Local Device Next Page Ability DM8203 does not support this function, so this bit is always 0
1	PAGE_RX	RO, 0b	New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management
0	LP_AN_ABLE	RO, 0b	Link Partner Auto-negotiation Ability A "1" in this bit indicates that the link partner supports Auto-negotiation

8.8 Specified Configuration Register – 14h

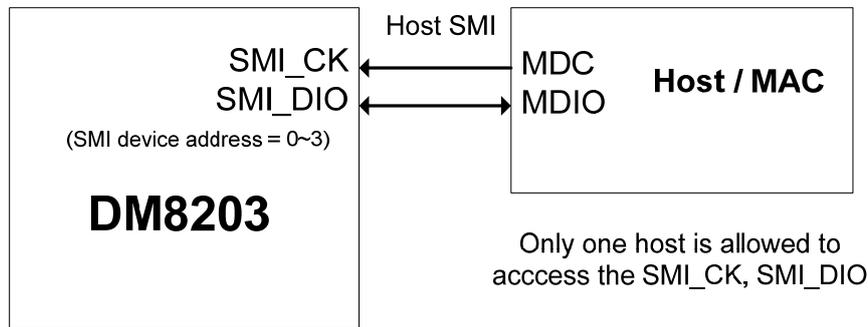
Bit	Bit Name	Default	Description
15:12	RESERVED	RW, 0b	Reserved Force to 0, in application
11	PREAMBLEX	RW, 0b	Preamble Saving Control 0 = When bit 10 is set, the 10BASE-T transmit preamble count is reduced. When bit 11 of register 1DH is set, 12-bit preamble is reduced; otherwise 22-bit preamble is reduced. 1 = Transmit preamble bit count is normal in 10BASE-T mode
10	TX10M_PWR	RW, 0b	10BASE-T mode Transmit Power Saving Control 1 = Enable transmit power saving in 10BASE-T mode 0 = Disable transmit power saving in 10BASE-T mode
9	NWAY_PWR	RW, 0b	Auto-negotiation Power Saving Control 1 = Disable power saving during auto-negotiation period 0 = Enable power saving during auto-negotiation period
8	RESERVED	RO, 0b	Reserved Read as 0, ignore on write
7	MDIX_CNTL	RO, X	The Polarity of MDI/MDIX value 1 = MDIX mode 0 = MDI mode
6	RESERVED	RW, 0b	Reserved Force to 0, in application
5	Mdix_fix Value	RW, 0b	MDIX_CNTL force value: When Mdix_down = 1, MDIX_CNTL value depend on the register value
4	Mdix_down	RW, 0b	MDIX Down Manual force MDI/MDIX. MDIX_CNTL value depend on PHY REG 14h.[5] 0 = Enable <i>HP</i> Auto-MDIX 1 = Disable <i>HP</i> Auto-MDIX
3:0	RESERVED	RW, 0b	Reserved Force to 0, in application

8.9 Power Saving Control Register (PSCR) – 1Dh

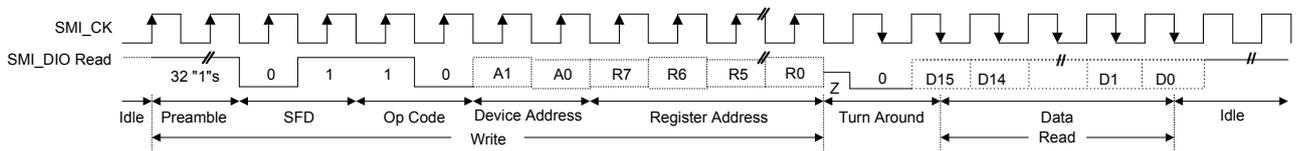
Bit	Bit Name	Default	Description
15:12	RESERVED	RO, 0h	Reserved
11	PREAMBLEX	RW, 0b	Preamble Saving Control when both bit PHY REG 14h.[11:10] are set, the 10BASE-T transmit preamble count is reduced. 1 = 12-bit preamble is reduced. 0 = 22-bit preamble is reduced.
10	RESERVED	RW, 0b	Reserved Force to 0, in application
9	TX_PWR	RW, 0b	Transmit Power Saving Control Disabled 1 = When cable is unconnected with link partner, the driving current of transmit is reduced for power saving. 0 = Disable transmit driving power saving function
8:0	RESERVED	RO, 0h	Reserved

9. Functional Description

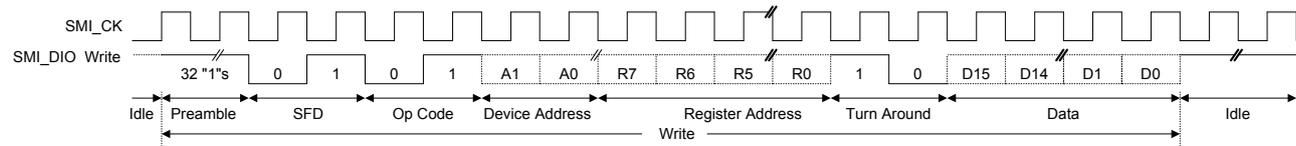
9.1 Serial Management Interface



Host SMI - Read Frame Structure



Host SMI - Write Frame Structure



The Host SMI consists of two pins, one is SMI_CK and another is SMI_DIO. User can access DM8203's EEPROM, PHY registers, MIB counters and Configuration registers through Host SMI.

The <Device Address> field of the frame means SMI device address that is configured by strap pin (TXD2_0 & TXD2_1). The <Register Address> field of the frame is mapped to address of control and status register set of DM8203. The read/writ data is valid on low byte (D7~D0) of <Data> field, the high byte (D15~D8) of data is reserved.

9.2 Switch Function

9.2.1 Address Learning

The DM8203 has a self-learning mechanism for learning the MAC addresses of incoming packets in real time. DM8203 stores MAC addresses, port number and time stamp information in the Hash-based Address Table. It can learn up to 1K unicast address entry.

The switch engine updates address table with new entry if incoming packet's Source MAC Address (SMAC) does not exist and incoming packet is valid (non-error and legal length).

Besides, DM8203 has an option to disable address learning for individual port by REG 65h.[0]

9.2.2 Address Aging

The time stamp information in address table is used for aging process. The switch engine updates time stamp whenever the corresponding SMAC receives. The switch engine would delete the entry if its time stamp is not updated for a period of time. The aging timer can be programmed or disabled by REG 52h.[1:0].

9.2.3 Packet Forwarding

The DM8203 forwards the incoming packet according to following decision:

- If Destination MAC Address (DMAC) is Multicast/Broadcast, the packet is forwarded to all ports, except to the port on which the packet was received.
- If DA is Unicast, the switch engine would look up address table. If the DA is not found, the packet would be treated as a multicast packet and forward to other ports. If entry is found and its destination port number is different to source port number, the packet would be forward to correct port.
- Switch engine also look up VLAN, Port Monitor setting and other forwarding constraints for the forwarding decision, more detail will discuss in later sections.

The DM8203 will filter incoming packets under following conditions:

- Error packets, including CRC errors, alignment errors, illegal size errors.
- PAUSE packets.
- If incoming packet is UNICAST and its destination port number is equal to source port number.

9.2.4 Inter-Packet Gap (IPG)

IPG is the idle time between any two valid packets at the same port. The typical number is 96 bits time. In other word, the value is 9.6u sec for 10Mbps and 960n sec for 100Mbps.

9.2.5 Back-off Algorithm

The DM8203 implements the binary exponential back-off algorithm in half-duplex mode compliant to IEEE standard 802.3.

9.2.6 Late Collision

Late Collision is a type of collision. If a collision error occurs after the first 512 bit times of data are transmitted, the packet is dropped.

9.2.7 Full Duplex Flow Control

The DM8203 supports IEEE standard 802.3x flow control frames on both transmit and receive sides. On the receive side, The DM8203 will defer transmitting next normal frames, if it receives a pause frame from link partner. On the transmit side, The DM8203 issues pause frame with maximum pause time when internal resources such as received buffers, transmit queue and transmit descriptor ring are unavailable. Once resources are available, The DM8203 sends out a pause frame with zero pause time allows traffic to resume immediately.

9.2.8 Half Duplex Flow Control

The DM8203 supports half-duplex backpressure. The inducement is the same as full duplex mode. When flow control is required, the DM8203 sends jam pattern and results in a collision. The flow control ability can be set in bit 4 of register 61h.

9.2.9 Partition Mode

The DM8203 provides a partition mode for each port, see REG 61h.[6]. The port enters partition mode when more than 64 consecutive collisions are occurred. In partition mode the port continuous to transmit but it will not receive. The port returned to normal operation mode when a good packet is seen on the wire. The detail description of partition mode represent following:

(1). Entering Partition State

A port will enter the Partition State when either of the following conditions occurs:

- The port detects a collision on every one of 64 consecutive re-transmit attempts to the same packet.
- The port detects a single collision which occurs for more than 512 bit times.
- Transmit defer timer time out, which indicates the transmitting packet is deferred to long.

(2). While in Partition State:

The port will continue to transmit its pending packet, regardless of the collision detection, and will not allow the usual Back-off Algorithm. Additional packets pending for transmission will be transmitted, while ignoring the internal collision indication. This frees up the ports transmit buffers which would otherwise be filled up at the expense of other ports buffers. The assumption is that the partition is signifying a system failure situation (bad connection/cable/station), thus dropping packets is a small price to pay vs. the cost of halting the switch due to a buffer full condition.

(3). Exiting from Partition State

The Port exits from Partition State, following the end of a successful packet transmission. A successful packet transmission is defined as no collisions were detected on the first 512 bits of the transmission.

9.2.10 Broadcast Storm Filtering

The DM8203 has an option to limit the traffic of broadcast or multicast packets, to protect the switch from lower bandwidth availability.

There are two types of broadcast storm control, one is throttling broadcast packet only, the other includes multicast. This option can be selected by REG 61h.[0].

The broadcast storm threshold can be programmed by EEPROM or REG 67h, the default setting is no broadcast storm protecting.

9.2.11 Bandwidth Control

The DM8203 supports two types of bandwidth control for each port. One is the ingress and egress bandwidth rate can be controlled separately, the other is combined together, the selection be set through REG 61h.[3]. This function is disabled by default, user can enable and configure rate by REG 66h in separate bandwidth control mode and REG 67h.[3:0] in combined mode.

The behavior of bandwidth control as below:

- (1). In separated mode, if flow control function is enabled and the ingress bandwidth reach threshold, Pause or Jam packet will be transmitted. The ingress packets will be dropped if flow control is disabled.
- (2). In separated mode, if egress bandwidth reach threshold, the egress port will not transmit any packets, but the ingress bandwidth of source port will be throttled that prevent packets from forwarding.
- (3). In combined mode, if the sum of ingress and egress bandwidth over threshold, the bandwidth will be throttled.

9.2.12 Port Monitoring Support

The DM8203 supports "Port Monitoring" function on per port base, detail as below:

- (1). Sniffer Port and Monitor Port

There is only one port can be selected as "sniffer port" by REG 52h.[4:3], multiple ports can be set as "receive monitor port" or "transmit monitor port" by per-port REG 65h.[6] or REG 65h.[5].

- (2). Receive monitor

All packets received on the "receive monitor port" are send a copy to "sniffer port". For example, port 0 is set as "receive monitor port" and port 2 is selected as a "sniffer port". If a packet is received form port 0 and predestined to port 1 after forwarding decision, the DM8203 will forward it to port 1 and port 2 in the end.

- (3). Transmit monitor

All packets transmitted on the "transmit monitor port" are send a copy to "sniffer port". For example, port 1 is set as "transmit monitor port" and port 2 is selected as "sniffer port". If a packet is received from port 0 and predestined to port 1 after forwarding decision, the DM8203 will forward it to port 1 and port 2 in the end.

- (4). Exception

The DM8203 has an optional setting that broadcast/multicast packets are not monitored (see REG 65h.[4]). It's useful to avoid unnecessary bandwidth.

9.2.13 VLAN Support

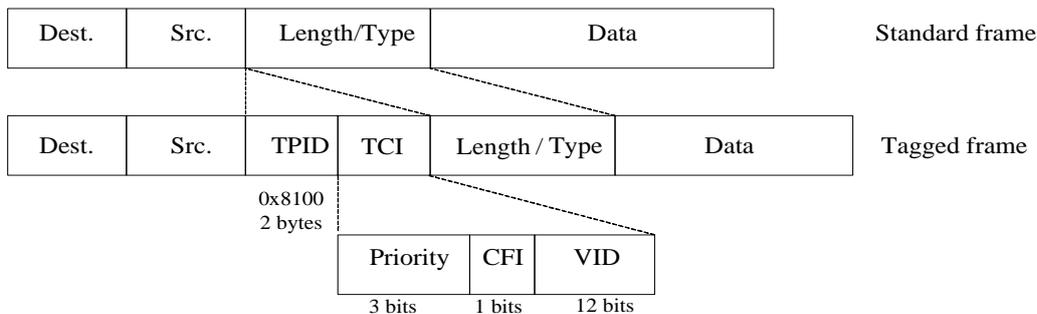
9.2.13.1 Port-Based VLAN

The DM8203 supports port-based VLAN as default, and up to 16 groups. Each port has a default VID called PVID (Port VID, see REG 6Fh). For VLAN setting, the DM8203 use LSB 4-bytes of PVID as index and map to the VLAN Group Mapping Registers (REG B0h~BFh) to decide the destination port(s).

9.2.13.2 802.1Q-Based VLAN

Regarding IEEE 802.1Q standard, Tag-based VLAN uses an extra tag to identify the VLAN membership of a frame across VLAN-aware switch/router. A tagged frame is four bytes longer than an untagged frame and contains two bytes of TPID (Tag Protocol Identifier) and two bytes of TCI (Tag Control Information).

The DM8203 also supports 802.1Q-based VLAN, and up to 16 groups. User can enable 802.1Q-based VLAN by REG 53h.[0]. It's obvious that the tagged packets can be assigned to several different VLANs which are determined according to the VID inside the VLAN Tag. Therefore, the operation is similar to port-based VLAN. The DM8203 use LSB 4-bytes VID of VLAN tag of received packet and the VLAN Group Mapping Register (REG B0h~BFh) to configure the VLAN partition. If the destination port of received packet is not belong to VLAN group, it will be discarded.



9.2.13.3 Tag/Untag

User can define each port as Tag port or Un-tag port by bit REG 6Dh.[7] in 802.1Q-based VLAN mode. The description of Tag and Un-tag operation is show as below:

- (1). Receive untagged packet and forward to Un-tag port. Received packet will forward to destination port without modification.
- (2). Receive tagged packet and forward to Un-tag port. The DM8203 will remove the tag from the packet and recalculate CRC before sending it out.
- (3). Receive untagged packet and forward to Tag port. The DM8203 will insert the PVID tag when an untagged packet enters the port, and recalculate CRC before delivering it.
- (4). Receive tagged packet and forward to Tag port. Received packet will forward to destination port without modification.

9.2.14 Priority Support

The DM8203 supports Quality of Service (QoS) mechanism for multimedia communication such as VoIP and video conferencing.

The DM8203 provides three priority classifications: Port-based, 802.1p-based and DiffServ-based priority. See next section for more detail. The DM8203 offers four level queues for transmit on each port.

The DM8203 provides two packet scheduling algorithms: Weighted Fair Queuing and Strict Priority Queuing. Weighted Fair Queuing (WFQ) based on their priority and queue weight. Queues with larger weights get more service than smaller. This mechanism can get highly efficient bandwidth and smooth the traffic. Strict Priority Queuing (SPQ) based on priority only. The packets on the highest priority queue is transmitted first. The next highest-priority queue is work until last queue empties, and so on. This feature can be set in REG 6Dh.[5].

9.2.14.1 Port-Based Priority

Port-based priority is the simplest scheme and as default. Each port has a 2-bit priority value as index for splitting ingress packets to the corresponding transmit queue. The port priority value can be configured in REG 6Dh.[1:0].

9.2.14.2 802.1p-Based Priority

The DM8203 extracts 3-bit priority field from received packet with 802.1p VLAN tag, and maps this field against VLAN Priority Map Registers (REG D0h~D1h) to determine which transmit queue is designated. The VLAN Priority Map Registers are programmable.

9.2.14.3 DiffServ-Based Priority

DiffServ-based priority use the most significant 6-bit of the ToS field in standard IPv4 header, and maps this field against ToS Priority Map Registers (REG C0h~CFh) to determine which transmit queue is designated. The ToS Priority Map Registers are programmable too. In addition, User can only refer to most significant 3-bit of the ToS field optionally, see REG 53h.[7].

9.3 MII Interface

9.3.1 MII Data Interface

The DM8203 port 2 provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the DM8203 port 2 and external device (a PHY or a MAC in reverse MII).

- TXD2 (transmit data) is a nibble (4 bits) of data that are driven by the DM8203 synchronously with respect to TXC2. For each TXC2 period, which TXE2 is asserted, TXD2 (3:0) are accepted for transmission by the external device.
- TXC2 (transmit clock) from the external device is a continuous clock that provides the timing reference for the transfer of the TXE2, TXD2. The DM8203 can drive 25MHz clock if it is configured to reversed MII mode.
- TXE2 (transmit enable) from the DM8203 port 2 MAC indicates that nibbles are being presented on the MII for transmission to the external device.
- RXD2 (receive data) is a nibble (4 bits) of data that are sampled by the DM8203 port 2 MAC synchronously with respect to RXC2. For each RXC2 period which RXDV2 is asserted, RXD2 (3:0) are transferred from the external device to the DM8203 port 2 MAC reconciliation sub layer.
- RXC2 (receive clock) from external device to the DM8203 port 2 MAC reconciliation sub layer is a continuous clock that provides the timing reference for the transfer of the RXDV2, RXD2, and RXER2 signals.
- RXDV2 (receive data valid) input from the external device to indicates that the external device is presenting recovered and decoded nibbles to the DM8203 port 2 MAC reconciliation sub layer. To interpret a receive frame correctly by the reconciliation sub layer, RXDV2 must encompass the frame, starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.
- RXER2 (receive error) input from the external device is synchronously with respect to RXC2. RXER2 will be asserted for 1 or more clock periods to indicate to the reconciliation sub layer that an error was detected somewhere in the frame being transmitted from the external device to the DM8203 port 2 MAC.
- CRS2 (carrier sense) is asserted by the external device when either the transmit or receive medium is non-idle, and de-asserted by the external device when the transmit and receive medium are idle. The CRS2 can also in output mode when the DM8203 port 2 is configured to reversed MII mode.
- COL2 (collision detection) is asserted by the external device, when both the transmit and receive medium is non-idle, and de-asserted by the external device when the either transmit or receive medium are idle. The COL2 can also in output mode when the DM8203 port 2 is configured to reversed MII mode.

9.3.2 MII Serial Management

The MII serial management interface consists of a data interface, basic register set in DM8203 port 0 and 1, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, include internal two ports, get status and error information, and determine the type and capabilities of the attached PHY device(s). The DM8203 default is polling 3 ports basic registers 0, 1, 4, and 5 to get the link, duplex, and speed status automatically. Alternatively, the DM8203 can be programmed to read or write any registers of 3 ports by section 6.8~11 CSR B, C, D, and E.

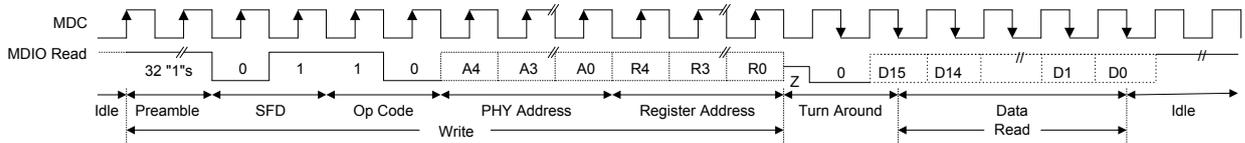
The DM8203 management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16,17, 18, 21, 22, 23 and 24~27.

In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP) :< 10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) field between Register Address field and Data field is provided for MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written onto management registers.

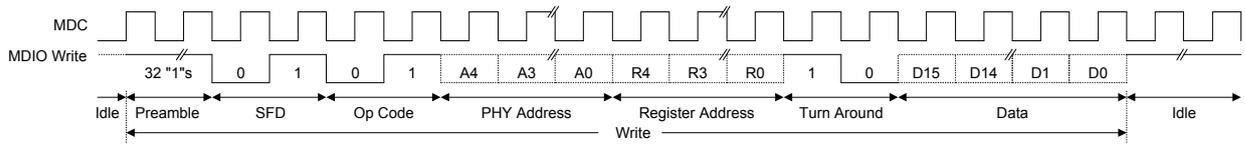
9.3.3 Serial Management Interface

The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of MDC (Management Data Clock), and MDIO (Management Data Input/Output) signals.

The MDIO pin is bi-directional and may be shared by up to 32 devices.



Management Interface - Read Frame Structure



Management Interface - Write Frame Structure

9.4 Internal PHY Functions

9.4.1 100Base-TX Operation

The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

9.4.1.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the desertions of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating the end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

9.4.1.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to the repeated 5B sequences, like the continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

9.4.1.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler, and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block

9.4.1.4 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard, for 100Base -TX transmission over Category-5 unshielded twisted pair cable.

9.4.1.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting The data stream output, from the NRZI encoder

into two binary data streams, with alternately phased logic One event.

9.4.1.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

9.4.1.7 4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

9.4.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.

The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

9.4.2.1 Signal Detect

The signal detects function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

9.4.2.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

9.4.2.3 MLT-3 to NRZI Decoder

The DM8203 decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

9.4.2.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ decoder.

9.4.2.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for

100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

9.4.2.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

9.4.2.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, and it descrambles the data streams, and presents the data streams to the Code Group alignment block.

9.4.2.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected and subsequent data is aligned on a fixed boundary.

9.4.2.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).

The T/R symbol pair is also stripped from the nibble, presented to the Reconciliation layer.

9.4.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM8203 is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

9.4.4 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in full duplex operation.

9.4.5 Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only during Receive operations.

9.4.6 Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

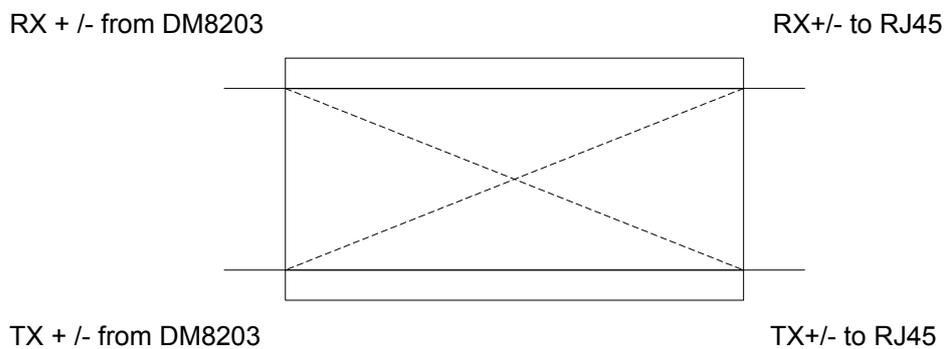
Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-negotiation but support a common mode of operation to establish a link.

9.5 HP Auto-MDIX Functional Descriptions

The DM8203 forwards the incoming packet according to following decision:

The DM8203 supports the automatic detect cable connection type, MDI/MDIX (straight through/cross over). A manual configuration by register bit for MDI or MDIX is still accepted.

When set to automatic, the polarity of MDI/MDIX controlled timing is generated by 16-bits LFSR. The switching cycle time is located from 200ms to 420ms. The polarity control is always switch until detect received signal. After selected MDI or MDIX, this feature is able to detect the required cable connection type. (Straight through or crossed over) and make correction automatically



* MDI: _____

* MDIX: - - - - -

10. DC and AC Electrical Characteristics

10.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Conditions
VCC33	3.3V Supply Voltage	-0.3	3.6	V	
VCC18	1.8V core power supply	-0.3	1.95	V	
AVDD33	Analog power supply 3.3V	-0.3	3.6	V	
AVDD18	Analog power supply 1.8V	-0.3	1.95	V	
V _{IN}	DC Input Voltage (VIN)	-0.5	5.5	V	
T _{STG}	Storage Temperature range	-65	+150	°C	
T _A	Ambient Temperature	0	+70	°C	
L _T	Lead Temperature (TL, soldering, 10 sec.).	-	+260	°C	Lead-free Device

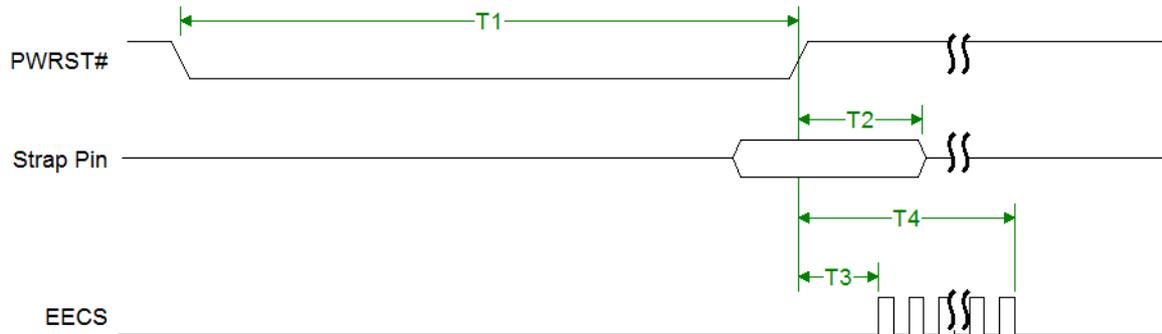
10.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VCC33	3.3V Supply Voltage	3.135	-	3.465	V	-
VCC18	1.8V core power supply	1.71	-	1.89	V	-
AVDD33	Analog power supply 3.3V	3.135	-	3.465	V	-
AVDD18	Analog power supply 1.8V	1.71	-	1.89	V	-
P _D (Power Dissipation)	100BASE-TX	-	107	-	mA	1.8V only
		-	54	-	mA	3.3V only
	10BASE-TX	-	57	-	mA	TX idle, 1.8V only
		-	64	-	mA	100% utilization, 1.8V only
		-	11	-	mA	3.3V only

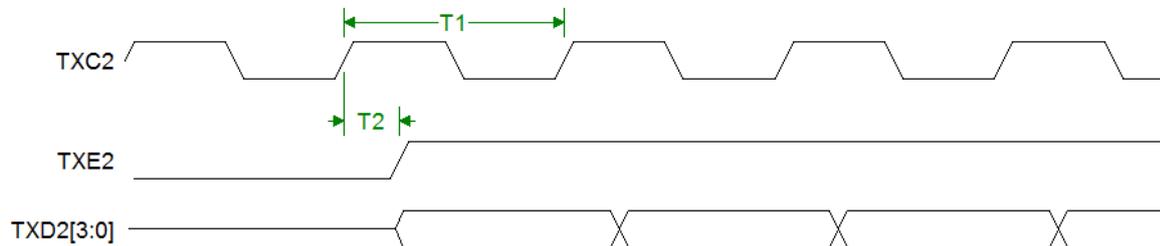
10.3 DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
VIL	Input Low Voltage	-	-	0.8	V	Vcond1
VIH	Input High Voltage	2.0	-	-	V	Vcond1
IIL	Input Low Leakage Current	-1	-	-	uA	VIN = 0.0V, Vcond1
IIH	Input High Leakage Current	-	-	1	uA	VIN = 3.3V, Vcond1
Outputs						
VOL	Output Low Voltage	-	-	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	-	-	V	IOH = -4mA
Receiver						
VICM	RX+/RX- Common Mode Input Voltage	-	1.8	-	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
VTD10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	19	20	21	mA	Absolute Value
ITD10	10TX+/- Differential Output Current	44	50	56	mA	Absolute Value

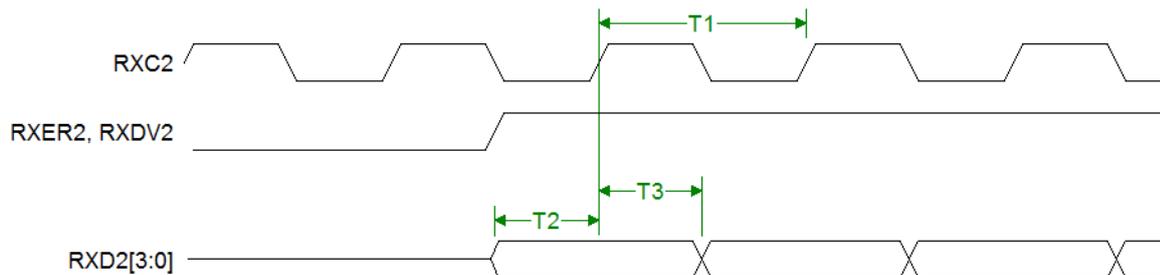
Note: Vcond1 = VCC33 = 3.3V, VCC18 = 1.8V, AVDD33 = 3.3V, AVDD18 = 1.8V.

10.4 AC Characteristics
10.4.1 Power On Reset Timing


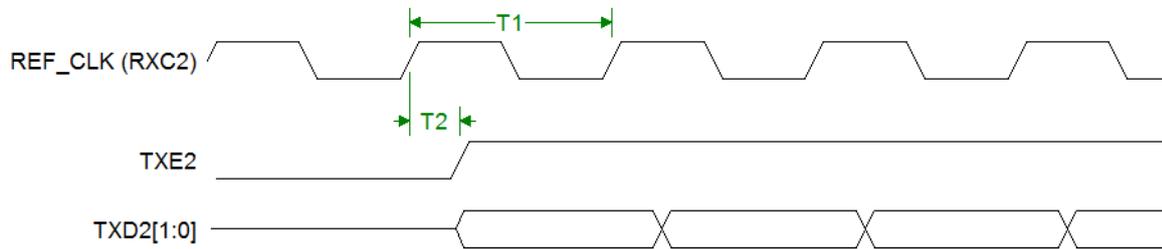
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	PWRST# Low Period	1	-	-	ms	-
T2	Strap pin hold time with PWRST#	40	-	-	ns	-
T3	PWRST# high to EECS high	-	5	-	us	
T4	PWRST# high to EECS burst end	-	--	4	ms	

10.4.2 Port 2 MII Interface Transmit Timing


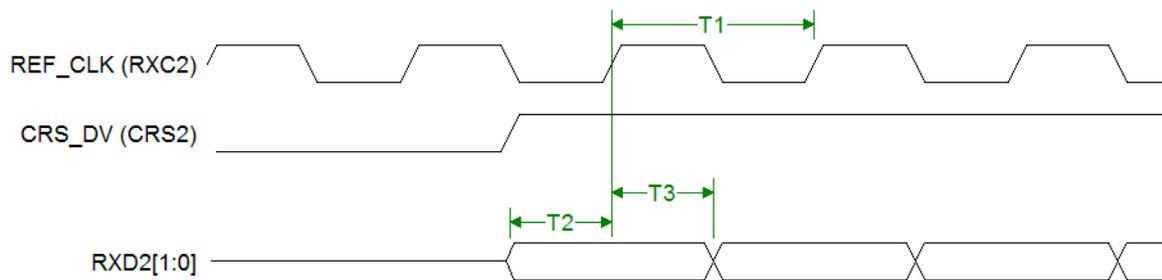
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	100M MII Transmit Clock Period	-	40	-	ns
T1	10M MII Transmit Clock Period	-	400	-	ns
T2	TXE2, TXD2 to TXC2 Rising Output Delay		8		ns

10.4.3 Port 2 MII Interface Receive Timing


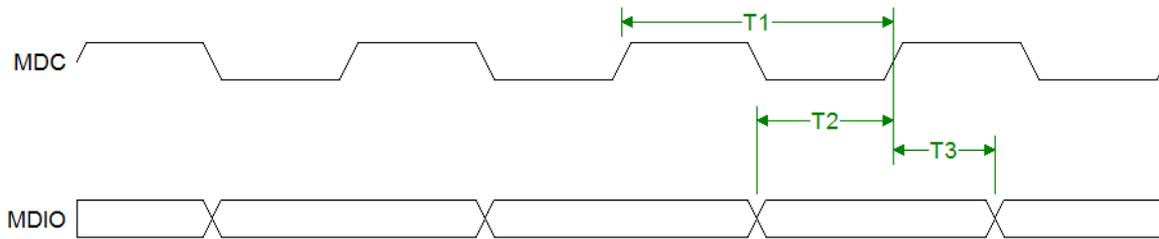
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	100M MII Receive Clock Period	-	40	-	ns
T1	10M MII Receive Clock Period	-	400	-	ns
T2	RXER2, RXDV2 and RXD2 to RXC2 Setup Time	5	-	-	ns
T3	RXER2, RXDV2 and RXD2 to RXC2 Hold Time	5	-	-	ns

10.4.4 Port 2 RMI Interface Transmit Timing


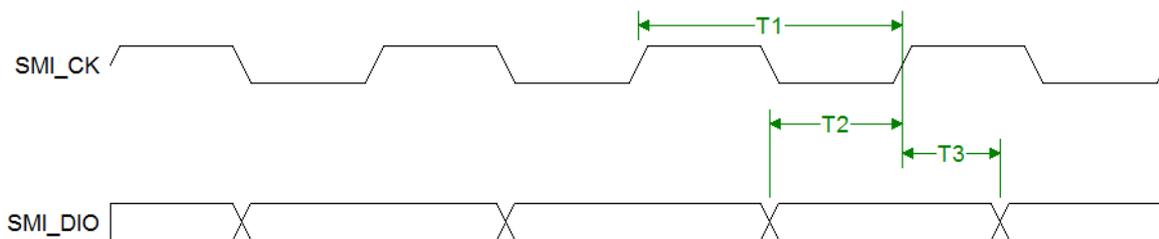
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RMI REF_CLK Period	-	20	-	ns
T2	TXE2, TXD2 to REF_CLK Rising Output Delay		8		ns

10.4.5 Port 2 RMI Interface Receive Timing


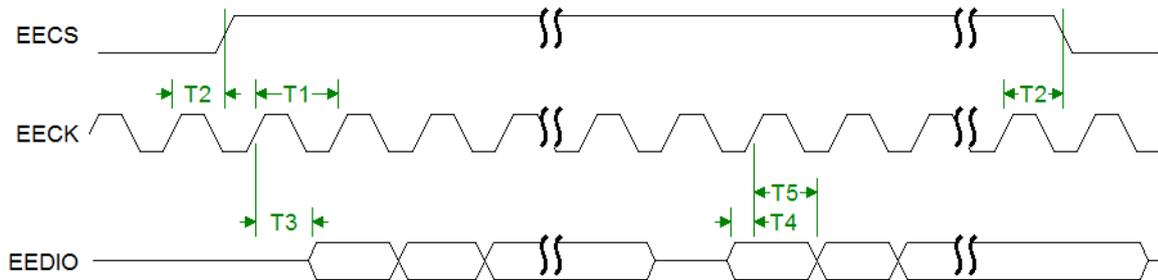
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RMI REF_CLK Period	-	20	-	ns
T2	CRS_DV, RXD2 to REF_CLK Setup Time	4	-	-	ns
T3	CRS_DV, RXD2 to REF_CLK Hold Time	2	-	-	ns

10.4.6 MII Management Interface Timing


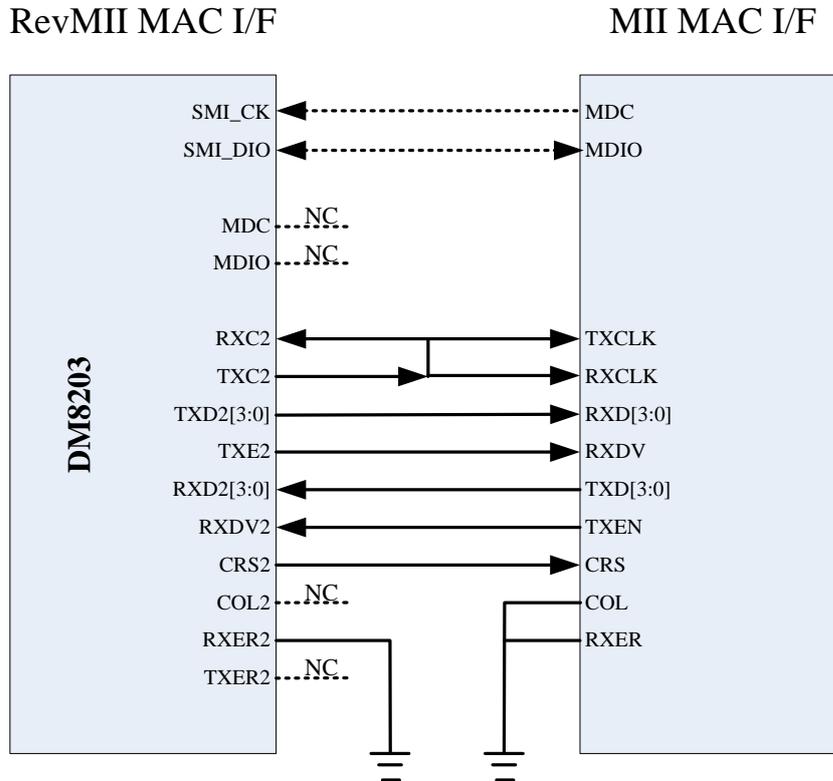
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	MDC Period	-	1920	-	ns
T2	MDIO to MDC Setup Time on Read/Write Cycle	40	-	-	ns
T3	MDIO to MDC Hold Time on Read/Write Cycle	40	-	-	ns

10.4.7 Host SMI Interface Timing


Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	SMI_CLK Period	80	-	-	ns
T2	SMI_DIO to SMI_CLK Setup Time on Read/Write Cycle	40	-	-	ns
T3	SMI_DIO to SMI_CLK Hold Time on Read/Write Cycle	40	-	-	ns

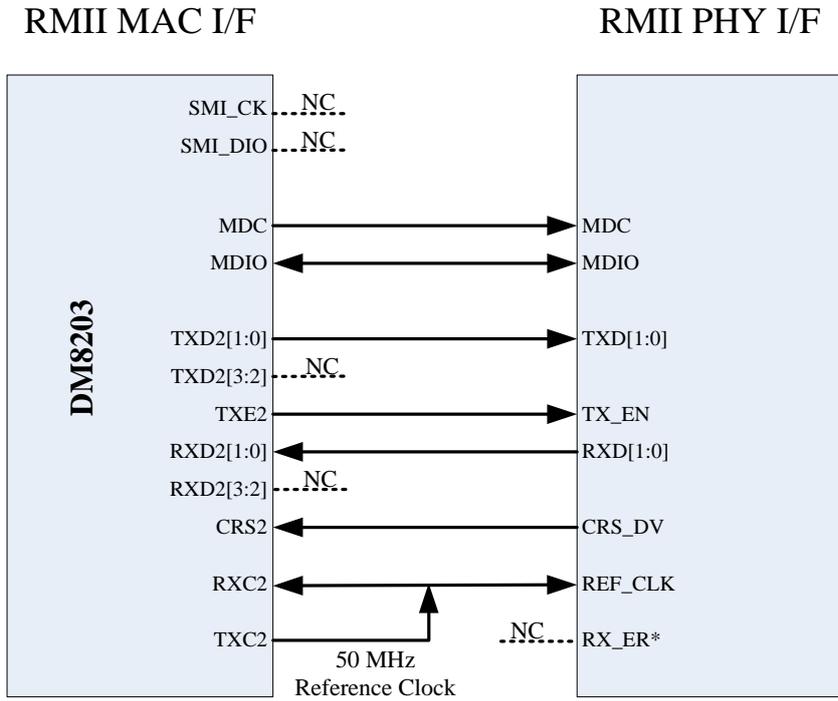
10.4.8 EEPROM Timing


Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EECK Period	-	5120	-	ns
T2	EECS to EECK Rising Output Delay	-	4160	-	ns
T3	EEDIO to EECK Rising Output Delay on Output State	-	4160	-	ns
T4	EEDIO to EECK Rising Setup Time on Input State	8	-	-	ns
T5	EEDIO to EECK Rising Setup Time on Input State	8	-	-	ns

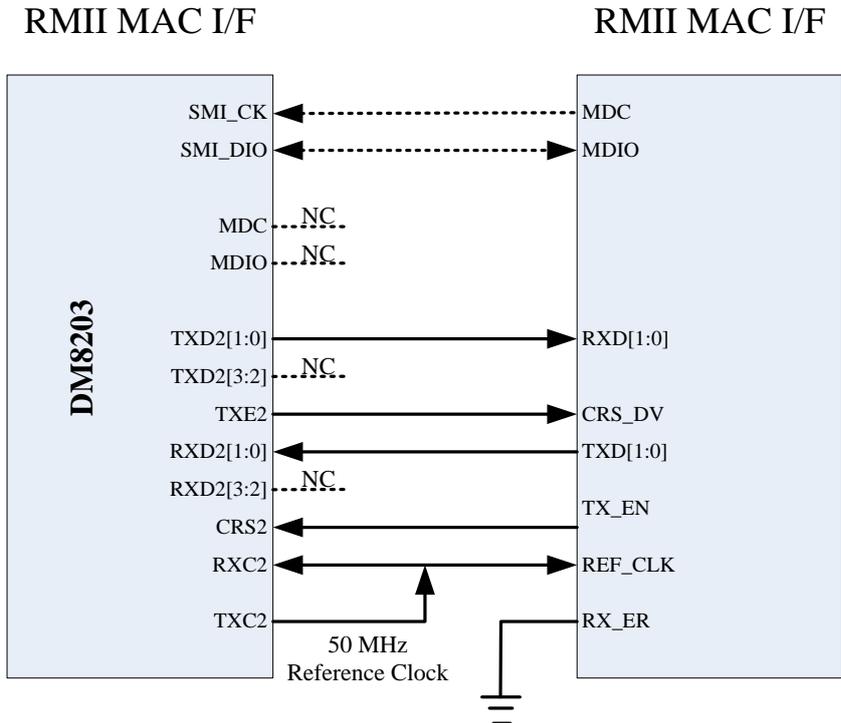
11.2 Application of Reverse MII


Note: The TXE2 and TXD2_2 pins of DM8203 must be pull-up resistor with 4.7K ohm to VCC33 in this application.

11.3 Application of Reduce MII to PHY



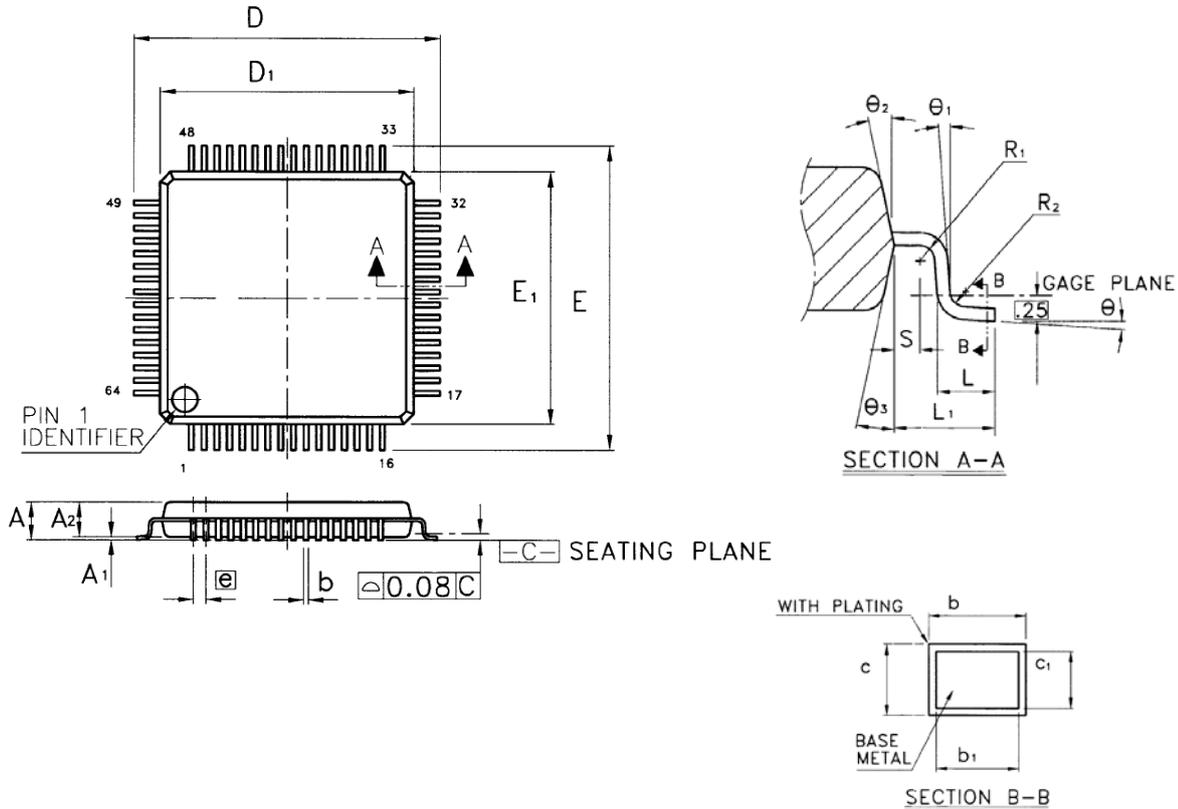
Note: The TXD2_3 pin of DM8203 must be pull-up resistor with 4.7K ohm to VCC33 in this application.

11.4 Application of Reduce MII to MAC


Note: The TXE2 and TXD2_3 pins of DM8203 must be pull-up resistor with 4.7K ohm to VCC33 in this application.

12. Package Information

64 Pins LQFP Package Outline Information:



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A ₁	0.05	-	0.15	0.002	-	0.006
A ₂	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b ₁	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	-	0.20	0.004	-	0.008
c ₁	0.09	-	0.16	0.004	-	0.006
D	12.00 BSC			0.472 BSC		
D ₁	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E ₁	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L ₁	1.00 REF			0.039 REF		
R ₁	0.08	-	-	0.003	-	-
R ₂	0.08	-	0.20	0.003	-	0.008
S	0.20	-	-	0.008	-	-
θ	0°	3.5°	7°	0°	3.5°	7°
θ ₁	0°	-	-	0°	-	-
θ ₂	12° TYP			12° TYP		
θ ₃	12° TYP			12° TYP		

1. Dimension D₁ and E₁ do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

13. Ordering Information

Part Number	Pin Count	Package
DM8203EP	64	LQFP (Pb-free)

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