Questa® Advanced Simulator

Questa's core simulation and debug engine

The Questa® Advanced Simulator combines high performance and capacity simulation with unified advanced debug and functional coverage capabilities for the most complete native support of Verilog, SystemVerilog, VHDL, SystemC, SVA, UPF and UVM.

The Questa Advanced Simulator is the core simulation and debug engine of the Questa Verification Solution; the comprehensive advanced verification platform capable of reducing the risk of validating complex FPGA and SoC designs.

Questa spans the levels of abstraction required for complex SoC and FPGA design and verification from TLM (Transaction Level Modeling) through RTL, gates, and transistors and has superior support of multiple verification methodologies including Assertion Based Verification (ABV), the Open Verification Methodology (OVM) and the Universal Verification Methodology (UVM) to increase testbench productivity, automation and reusability.

Breaking the Speed Limits on SoC Verification with the Questa Flow

On-demand Web Seminar

Learn best practice in verification flows in the industry today, and how to implement the optimal flow to speed your SoC design verification cycle.

Features

- High Performance and Capacity
- Assertion Based Verification
- Test Automation
- Questa Verification Management
- Integrated Multi-Language Debugging
- Power Aware Verification

High Performance and Capacity

The Questa Advanced Simulator achieves industry-leading performance and capacity through very aggressive, global compile and simulation optimization algorithms of SystemVerilog and VHDL, improving SystemVerilog and mixed VHDL/SystemVerilog RTL simulation performance by up to 10X. Questa also supports very fast time-to-next simulation and effective

library management while maintaining high performance with unique capabilities to pre-optimize and define debug visibility on a block by block basis enabling dramatic regression throughput improvements of up to 3X when running a large suite of tests. To increase simulation performance for large designs with long simulation times, Questa also has a Multi-Core option. Questa Multi-Core takes advantage of modern compute systems by partitioning the design to run in parallel on multiple CPU's or computers using either automatic or manually driven partitions. To achieve even greater performance, Questa supports TBX; the highest performance Transaction Level link to the Veloce platform enabling a 100x increase in performance with debug visibility and a common testbench.

Benefits

- **High-performance, multi-language engine** for the most sophisticated regression suites
- **Highly productive advanced verification** solution with verification management for coverage closure of large, complex electronic systems
- **Easy to use, fast time-to-debug** through native assertions and a complete multi-abstraction and multi-language debug environment including transaction-level debug
- **Constrained-random stimulus** generation to automate test development

- **Native advanced SystemVerilog testbench capabilities** with OVM and UVM combined with unique debug function to ease the development and debug of advanced testbenches
- **High bandwidth Transaction Level** (TBX) integration with the Veloce Platform to achieve dramatic simulation acceleration
- **Native support** of Power Aware Simulation using UPF
- **Multi-Core simulation** which supports all design languages and constructs and either automatically or manually partitions the design to run in parallel while maintaining a single database for debug and coverage.