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HYUNDAI SEMICONDUCTOR HY53C256

256K×1-Bit CMOS DRAM

M111201B-JAN92

DESCRIPTION

The HY53C256 is a high speed 262,144×1 bit CMOS dynamic random access memory. Fabricated with HYUNDAI CMOS technology, the HY53C256 offers a fast page mode for high data bandwidth, fast usable speed, CMOS standby current and, for the HY53C256L, reduced CMOS standby mode supply current (I_{DD5}).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system perfor mance.

Fast page mode operation allows random or sequential access of up to 512 bits within a row with cycle times as fast as 50 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the HY53C256 design is optimized suited for cache based mainframe and minicomputers, graphics, digital signal processing and high performance microprocessor systems.

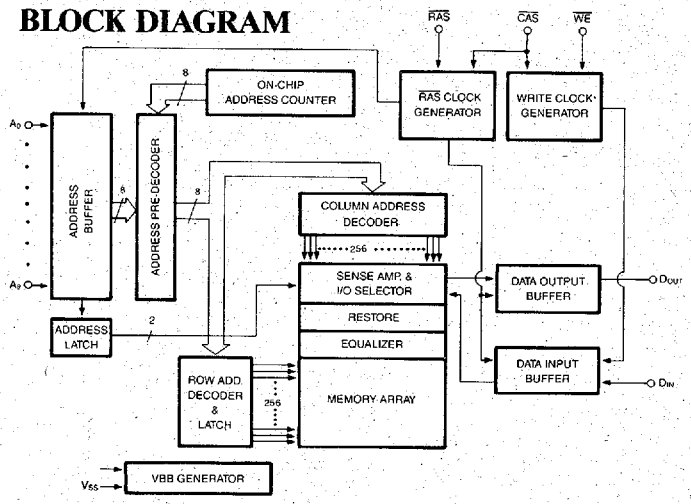
The HY53C256L offers a maximum data retention power of 5 mW when operating in CMOS standby mode and performs $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. This mode is entered by holding $\overline{RAS}$ at a voltage greater than V_{DD}-0.2 when it is inactive.

FEATURES

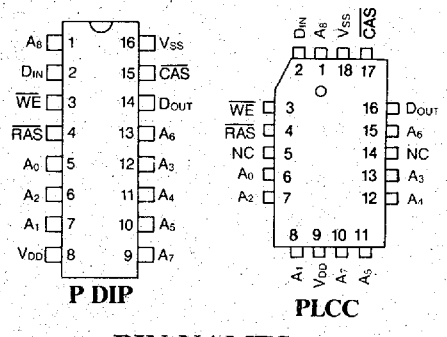
- **Low power dissipation for HY53C256L**
  - **Operating Current, 100ns : 50mA (max.)**
  - **TTL Standby Current : 2mA (max.)**
  - **CMOS Standby Current : 1mA (max.)**
- **Read-Modify-Write Capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability**
- **Common I/O capability**
- **Fast Page Mode operation for a sustained data rate up to 20 MHz**
- **256 Refresh cycles/4 ms**
- **High reliability 16 pin 300 mil P-DIP and 18 pin PLCC**
- **Fast access time and cycle time (ns)**

	HY53C256-70	HY53C256-80	HY53C256-10	HY53C256-12
Max $\overline{RAS}$ Access Time, t_{RAC}	70	80	100	120
Max $\overline{CAS}$ Access Time, t_{CAC}	15	20	25	30
Min Fast Page Mode Cycle Time, t_{PC}	50	55	60	70
Min Cycle Time, t_{RC}	130	145	175	205

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0—A_8	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature Under Bias	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 125	℃
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	1.0	W

NOTE :
1. Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC CHARACTERISTICS

(T_A=0℃ to 70℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY53C256 MIN.	HY53C256 MAX.	UNIT	NOTE
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$		—	10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		—	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−70	—	70	mA	1,2
			−80	—	60		
			−10	—	50		
			−12	—	45		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH}, other inputs≥V_{SS}	HY53C256	—	3	mA	
			HY53C256L	—	2		
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70	—	70	mA	2
			−80	—	60		
			−10	—	50		
			−12	—	45		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70	—	45	mA	1,2
			−80	—	40		
			−10	—	35		
			−12	—	30		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$≥V_{DD}-0.2V, $\overline{CAS}$= V_{IH}, other inputs≥V_{SS}	HY53C256	—	2	mA	
			HY53C256L	—	1		
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min)	−70	—	70	mA	2
			−80	—	60		
			−10	—	50		
			−12	—	45		
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	V_{DD}+1	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		—	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	—	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.

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AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY53C256-70		HY53C256-80		HY53C256-10		HY53C256-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	100	75K	120	75K	ns	
2	t_{RC}	Read or Write Cycle Time	130	—	145	—	175	—	205	—	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50	—	55	—	65	—	75	—	ns	
4	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	ns	
5	t_{RAH}	Row Address Hold Time	15	—	15	—	15	—	20	—	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	45	—	55	—	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	35	20	40	20	55	25	65	ns	1
8	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	
9	t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	25	—	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	55	25	60	25	75	30	90	ns	2
11	t_{RAC}	Access Time from $\overline{RAS}$	—	70	—	80	—	100	—	120	ns	3,4,5
12	t_{AA}	Access Time from Column Address	—	35	—	40	—	45	—	55	ns	5,6,12
13	t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	25	—	30	ns	5,12
14	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	15	75K	20	75K	25	75K	30	75K	ns	
15	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time in Read Cycel	15	—	20	—	25	—	30	—	ns	
16	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	0	—	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5	—	5	—	5	—	5	—	ns	7
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5	—	5	—	5	—	5	—	ns	7
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	15	—	20	—	ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	15	0	20	0	25	0	30	ns	8
21	t_{OH}	Data Hold Time From $\overline{CAS}$	0	—	0	—	0	—	0	—	ns	8
22	t_{WP}	Write Pulse Width	15	—	15	—	20	—	25	—	ns	
23	t_{CP}	$\overline{CAS}$ Precharge Time	15	—	15	—	20	—	25	—	ns	
24	t_{AR}	Column Address Hold Time From $\overline{RAS}$	55	—	60	—	70	—	80	—	ns	
25	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	20	—	25	—	30	—	35	—	ns	
26	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time in Write Cycle	25	—	25	—	30	—	35	—	ns	
27	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55	—	60	—	70	—	80	—	ns	
28	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	ns	9,10
29	t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	25	—	ns	
30	t_{DS}	Data In Setup Time	0	—	0	—	0	—	0	—	ns	11
31	t_{DH}	Data In Hold Time	15	—	15	—	20	—	25	—	ns	11
32	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	55	—	60	—	70	—	80	—	ns	
33	t_{RWC}	Read-Modify-Write Cycle Time	155	—	175	—	210	—	245	—	ns	
34	t_{RRW}	Read-Modify-Write Cycle, $\overline{RAS}$ Pulse Width	95	—	110	—	135	—	160	—	ns	
35	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in RMW Cycle	70	—	80	—	100	—	120	—	ns	9
36	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	15	—	20	—	25	—	30	—	ns	9
37	t_{AWD}	Column Address to $\overline{WE}$ Delay	35	—	40	—	45	—	55	—	ns	9
38	t_{CAP}	Access Time from Column Precharge	—	45	—	50	—	55	—	65	ns	12

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#	SYMBOL	PARAMETER	HY53C256-70		HY53C256-80		HY53C256-10		HY53C256-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{PC}	Fast Page Mode Read or Write Cycle Time	50	—	55	—	60	—	70	—	ns	
40	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	75	—	85	—	95	—	110	—	ns	
41	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	30	—	35	—	ns	
42	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	25	—	30	—	35	—	ns	
43	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	0	—	ns	
44	t_{CSR}	$\overline{CAS}$ Setup Time, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10	—	10	—	10	—	10	—	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	20	—	25	—	30	—	40	—	ns	
46	t_{CSH}	$\overline{CAS}$ Hold Time	70	—	80	—	100	—	120	—	ns	
47	t_T	Transition Time(Rise and Fall)	3	25	3	25	3	25	3	25	ns	13
48	t_{RI}	Refresh Interval(256 Cycles)	—	4	—	4	—	4	—	4	ms	14

NOTES :

1. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, the access time is controlled by t_{AA} and t_{CAC}.
2. t_{RCD}(max.) is specified for reference only. Operation within t_{RCD}(max.) limits insures that t_{RAC}(max.) and t_{AA}(max.) can be met. If t_{RCD} is greater than the specified t_{RCD}(max.), the access time is controlled by t_{AA} and t_{CAC}.
3. Assumes that $t_{RAD} \leq t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.).
5. Measured with a load equivalent to two TTL inputs and 100 pF in parallel.
6. Assumes that $t_{RAD} \geq t_{RAD}$(max.).
7. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
8. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
9. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
10. t_{WCS}(min.) must be satisfied in an Early Write Cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.). AC measurements assume t_T=5 ns.
14. An initial 200μs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

CAPACITANCE(1)

(T_A=25℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, D_{IN}	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	8	pF
C_{OUT}	D_{OUT}	—	8	pF

NOTE :

1. Capacitance is measured at the worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAMS

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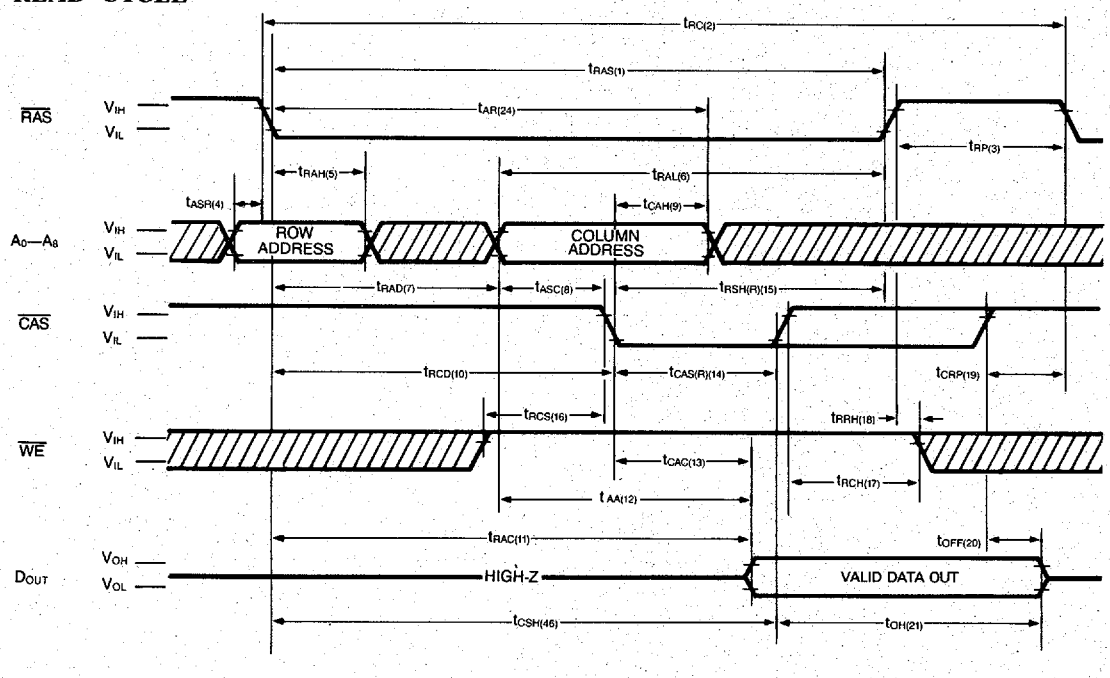
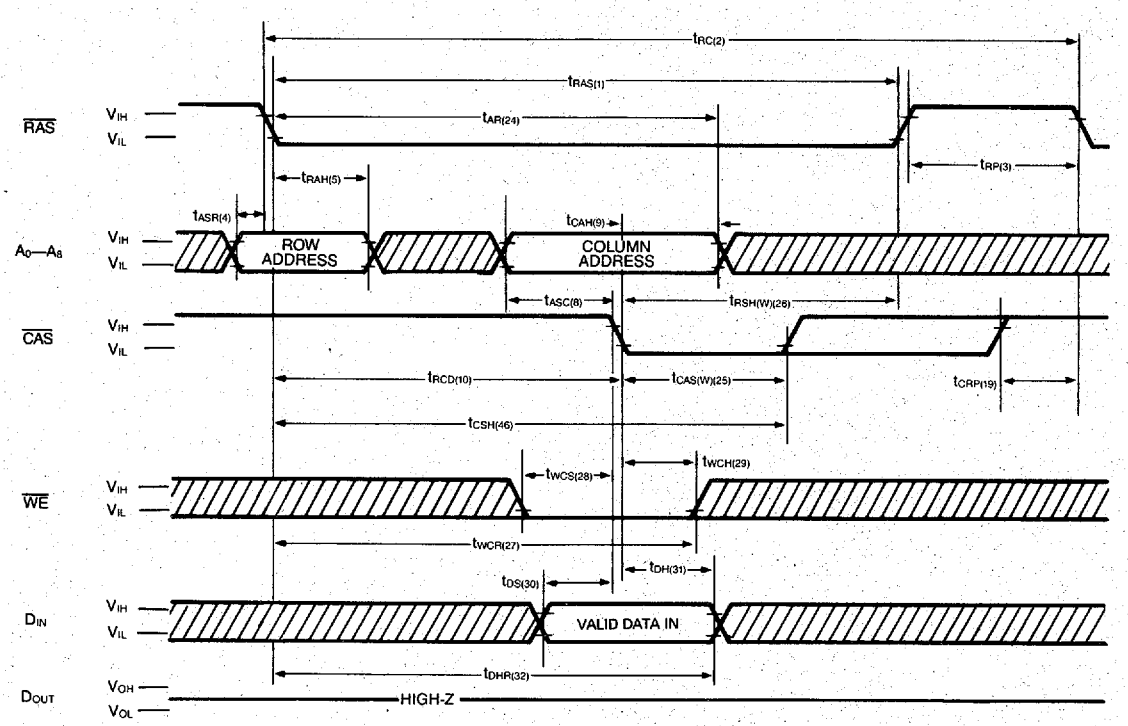
READ CYCLE



EARLY WRITE CYCLE



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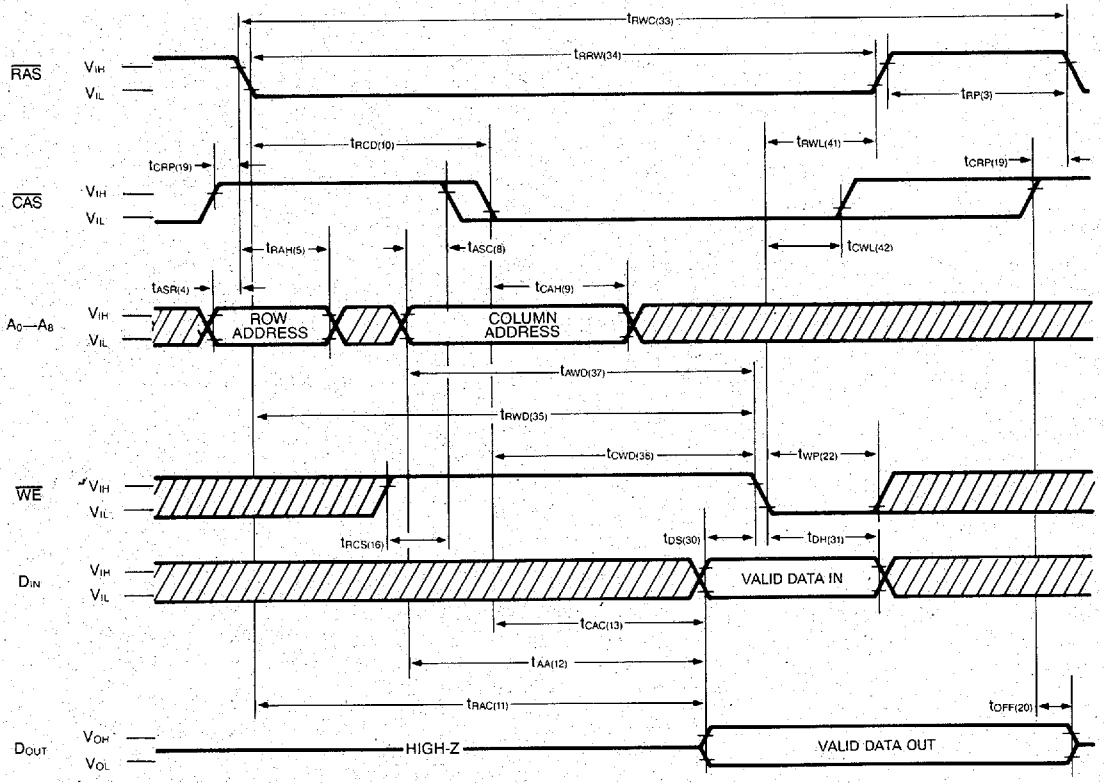
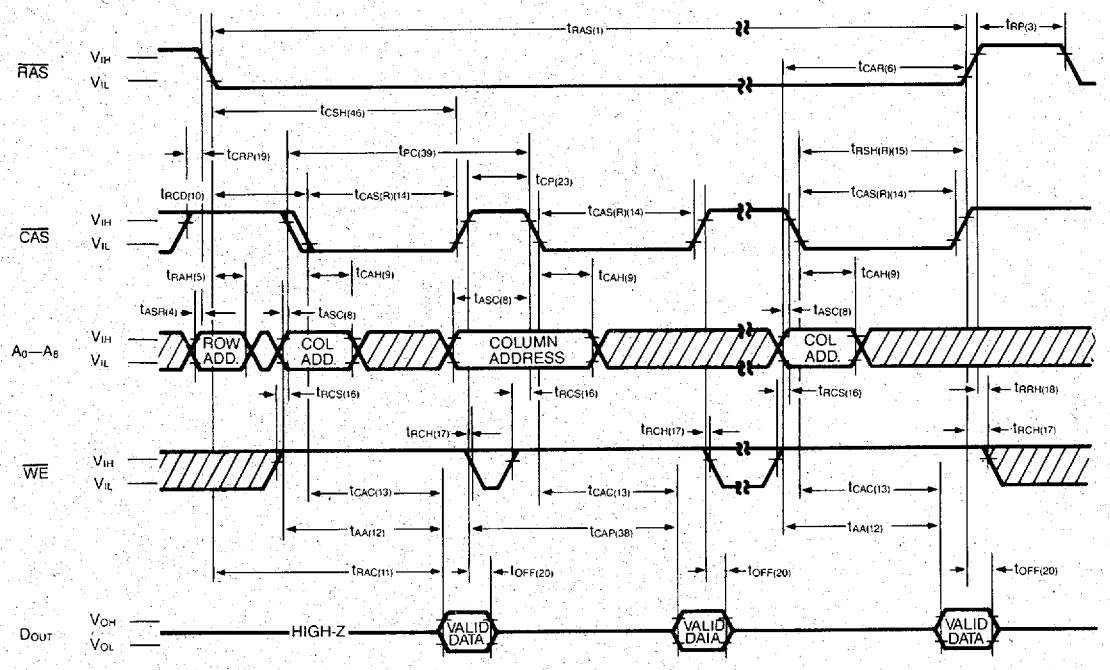
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



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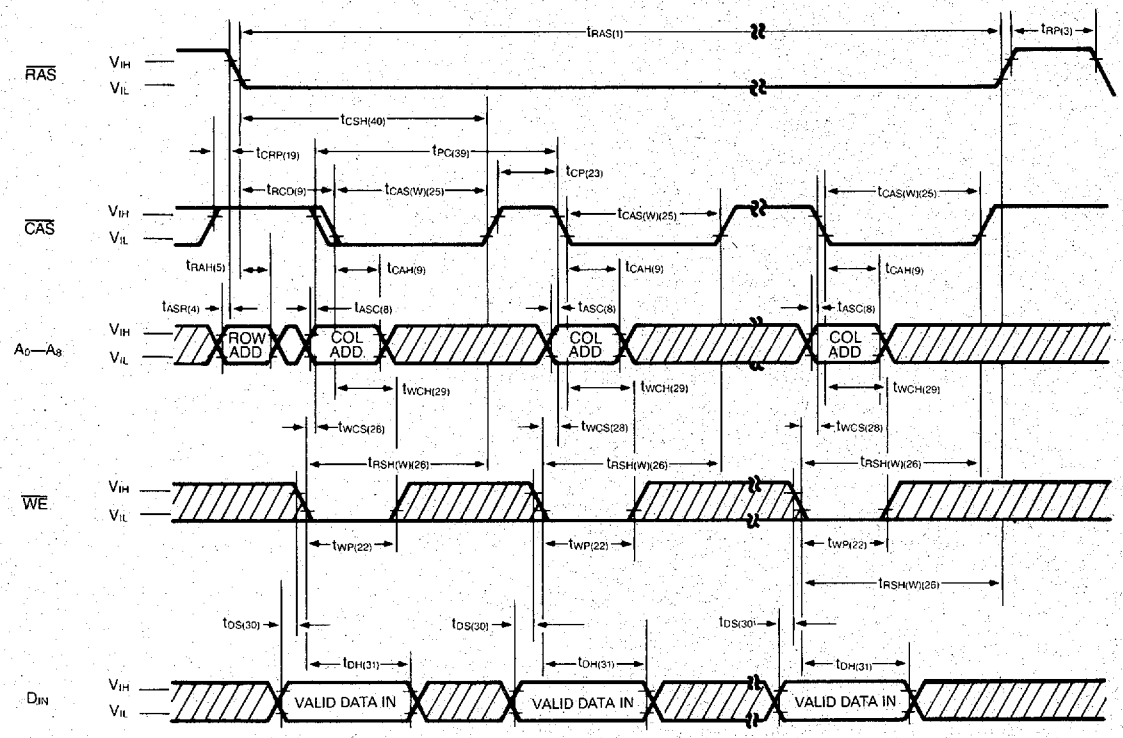
FAST PAGE MODE WRITE CYCLE



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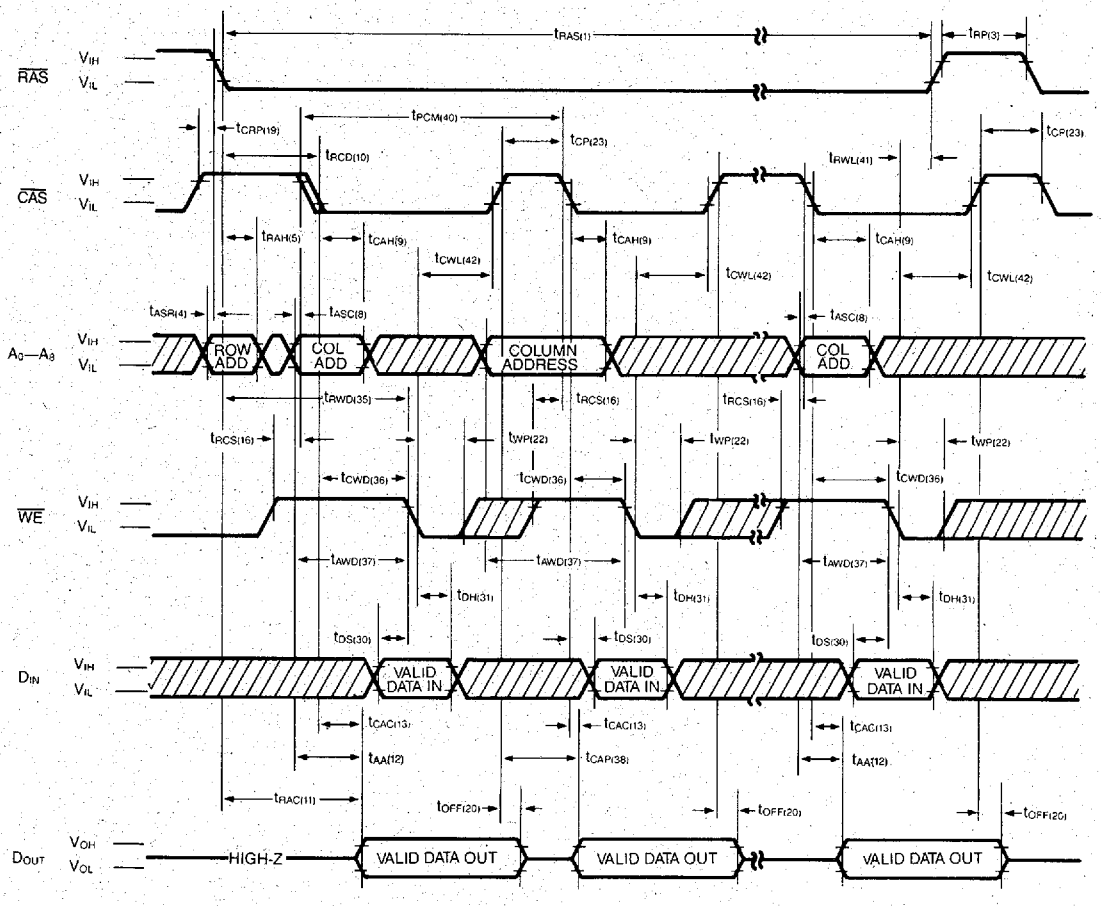
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



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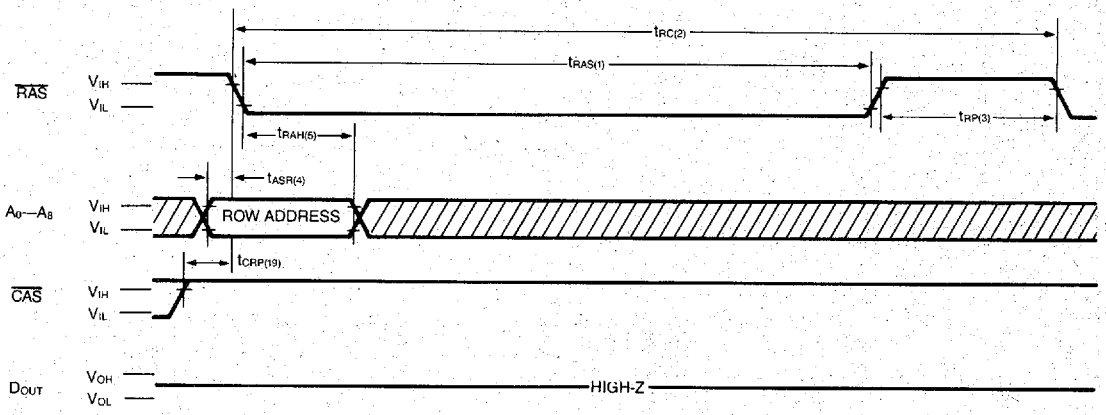
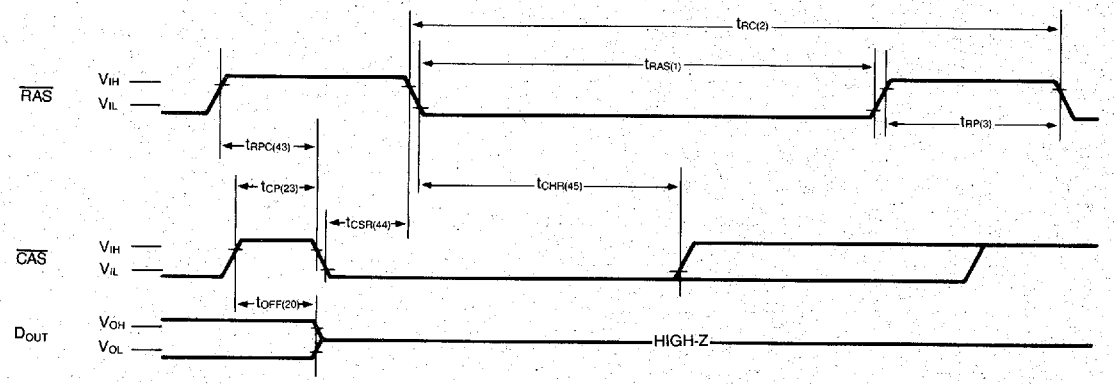
RAS-ONLY REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE



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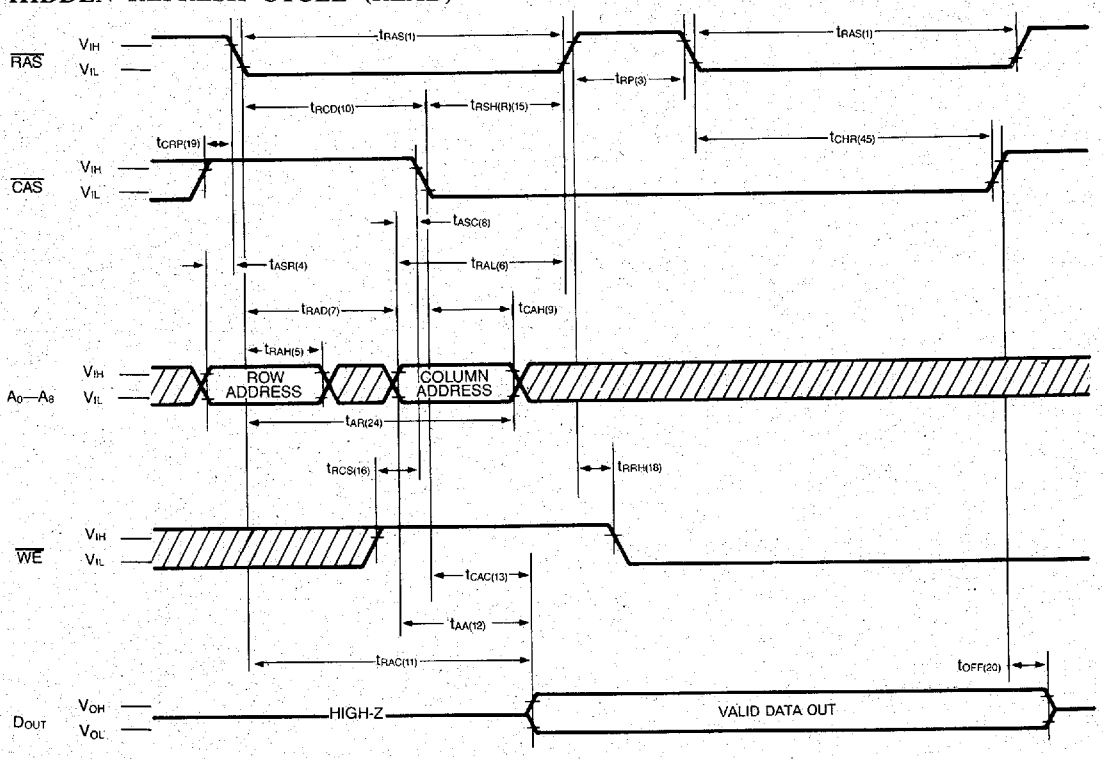
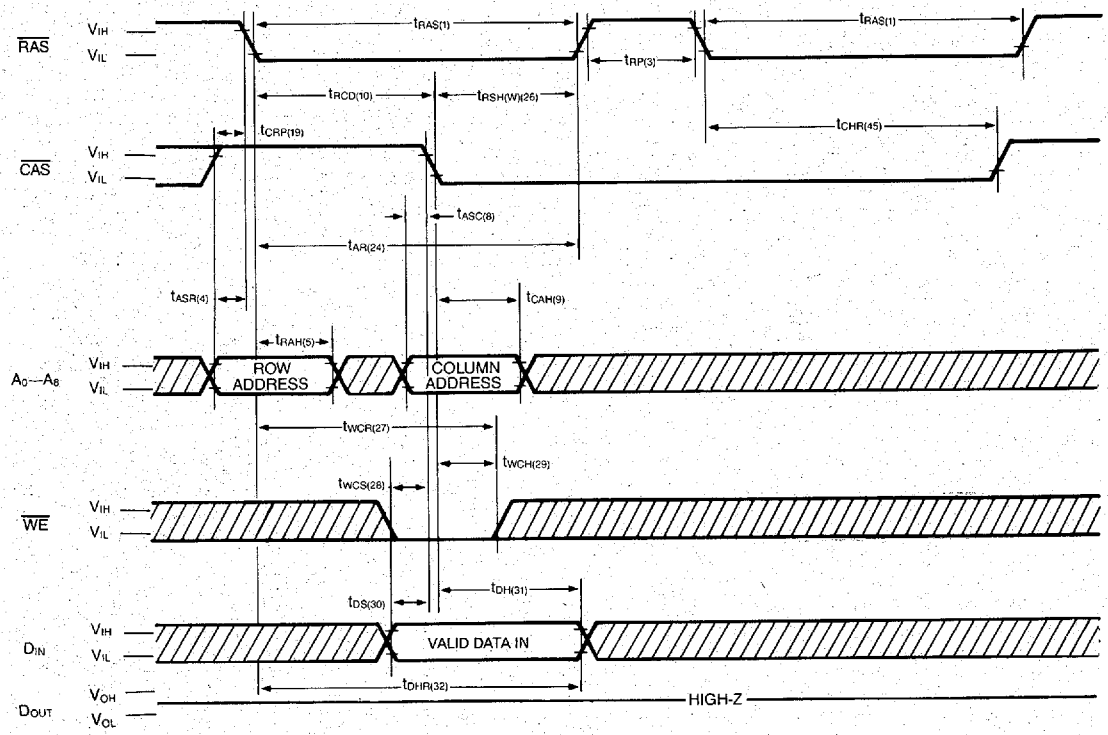
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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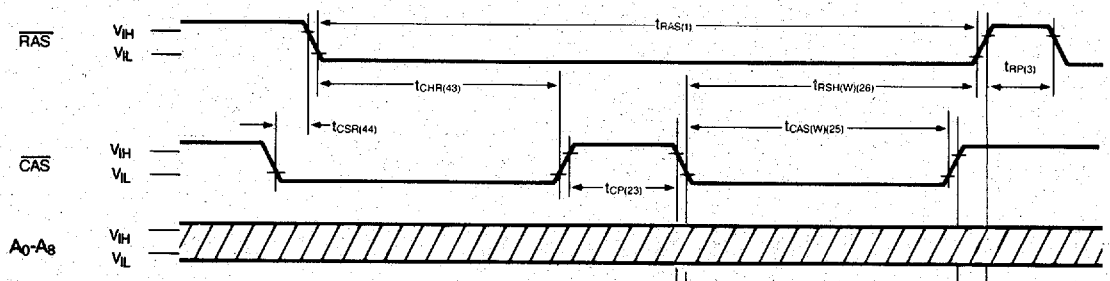
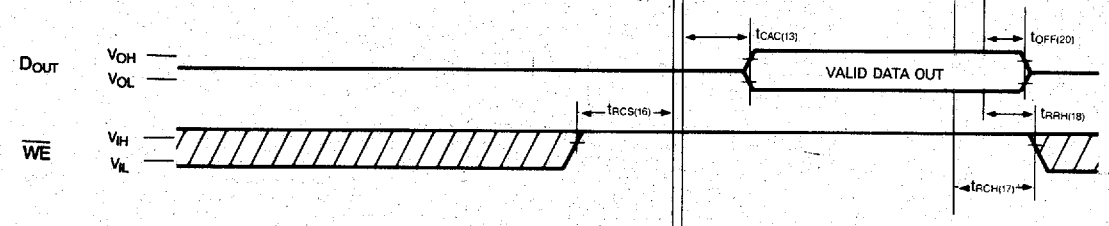
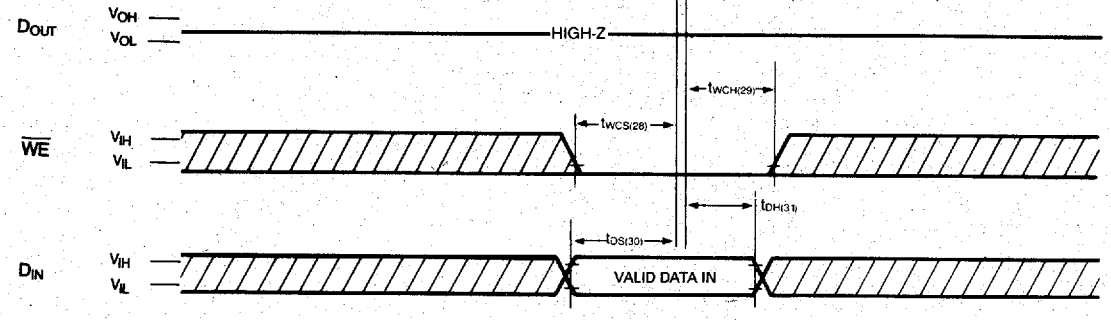
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



READ CYCLE



WRITE CYCLE



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FUNCTIONAL DESCRIPTION

The HY53C256 is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The HY53C256 reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

MEMORY CYCLE

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out becomes valid only when t_{RAC}, t_{AA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between t_{RAC}, t_{AA} and t_{CAC}. For example, the access time is limited by t_{AA} when t_{RAC}(min.) are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled write cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the output(D_{OUT}) pin will be in the High-Z state at the beginning of the write function. Ending the write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

REFRESH CYCLE

To retain data, 256 refresh cycles are required in each 4 ms period. There are two ways to refresh the memory :

1. By clocking each of the 256 row addresses(A_0 through A_7) with $\overline{RAS}$ at least every 4 ms. Any read, wrtie, read-modify-write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The HY53C256 will use the output of an internal 8-bit counter as the source of row address and ignore external address inputs.
   $\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, D_{OUT} will remain in the High-Z state during the cycle.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to write consecutive data patterns (256 write cycles) and then verify the written data by applying 256 consecutive read cycles.

DATA RETENTION MODE

The HY53C256 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY53C256 power consumption is reduced to the low I_{DD5} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DD5})}{t_{RX}}$$

Where t_{RC}=Refresh Cycle Time
t_{RX}=Refresh Interval/256

FAST PAGE MODE OPERATION

Fast page mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high.

Thus, access begins at the occurrence of a valid column address rather than at the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable.

During fast page mode operation, read, write, read-modify-write, or read-write-read cycles are possible at random addresses within a row. Following the initial entry cycle into fast page mode, access is t_{AA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is determined by the $\overline{CAS}$ rising edge(specified by t_{CAP} as shown in figure 1). If the column address is valid after the rising edge of $\overline{CAS}$, the access is timed from the occurrence of the valid address and is specified by t_{AA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast page mode provides a sustained data rate of over 20 MHz for applications that require high data rates like bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate :

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

DATA OUTPUT OPERATION

The HY53C256 data output pin(D_{OUT}) has a three-state capability and is controlled by $\overline{CAS}$. When $\overline{CAS}$ is high($\geq V_{IH}$), the output is in the High-Z state. Table 1 summarizes the D_{OUT} states possible for various memory cycles.

POWER ON

After application of the V_{DD} an initial pause of 200μs is required followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

During power on, the V_{DD} current requirement of the HY53C256 is dependant on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on to avoid current surges.

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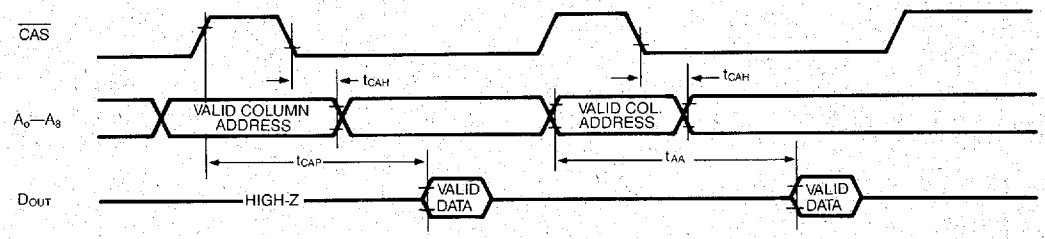
TABLE 1. DATA OUTPUT OPERATION FOR VARIOUS CYCLE TYPES

CYCLE TYPE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle(Early Write)	High-Z
$\overline{WE}$-Controlled Wirte Cycle(Late Write)	Active, not valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle(Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh Cycle	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data Remains as in Previous Cycle
$\overline{CAS}$-only Cycle	High-Z

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION



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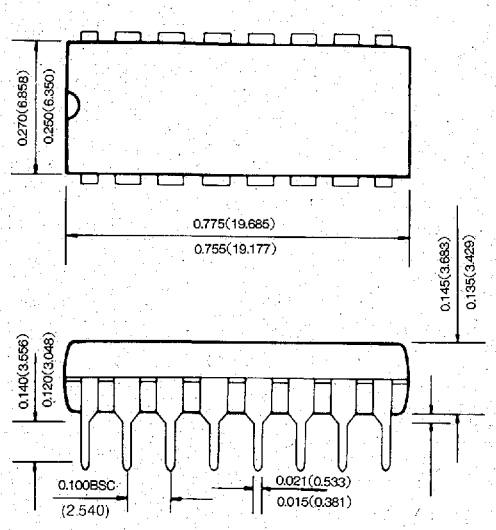
PACKAGE INFORMATION

• 16 PIN PLASTIC DUAL IN LINE PACKAGE−300 MIL



• 18 PIN PLASTIC LEADED CHIP CARRIER−330 MIL