Tanner EDA Tools v16.30
Release Notes

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Tanner EDA Tools Version 16.30

What's New in S-Edit v16.30

Annotation of Simulation Results

- The Annotate command has been enhanced to support annotation of Small Signal results, Model parameters, and Device parameters on schematic.

Differential Voltage Probing

- Differential voltage probing of two nets may now be performed from S-Edit. First select a reference net, then subsequent voltage probes will display the difference between the probed net and the reference net.

Performance Improvements

- Performance improvements in saving and loading designs, in particular designs with buses and arrays. Also fixed crash on saving in certain circumstances.
- Performance improvements in loading schematics with lots of libraries.

Miscellaneous New Features

- S-Edit now supports environment variables in path names. Environment variables may be referenced by %VARIABLE%, $VARIABLE, or ${VARIABLE}.
- The “Sort by name” button has been removed from the Properties Navigator, and properties are now always sorted alphabetically, case insensitive.
- In Evaluated Mode, properties are now displayed using their Description string rather than the property name. In Evaluated mode, non-editable properties are now displayed with gray background and their values cannot be modified.
- A net name can now be inherited from a property name. A reference to a non-existent pin (e.g. %vdd) in the SPICE.OUTPUT is now redirected to a sibling property on the instance.
- S-Edit Library Navigator now shows all cells when no library is selected, the same behavior as L-Edit.
- CDF Technology can now be imported using File > Import > Import CDF.
- A new field to indicate simulation temperature (.temp) is added to the Setup Simulation dialog.
- A new tcl command, **workspace menu**, is added to create menu commands. Use **workspace menu –help** for details.
- In Setup Simulation > Corner Simulations, individual corner simulations may now be temporarily disabled, without having to delete the corner.Right click on the column heading to disable the corner.
- A button has been added to the Filter edit control in the Library Navigator. The button indicates a history droplist if the edit field is empty; otherwise it is an X, and pressing it clears the filter edit field.

Bug Fixes

- Fixed a problem where "Stop simulation" button became inactive even though simulation continued in T-Spice.
- Slow rendering when in evaluated property mode has been improved.
- S-Edit cell copy now resets the revision count to 1.
- Fixed a syntax error in SPICE output if there is no space between a variable and comma.

- Fixed problem where probing did not work when no analysis option was selected.
- Toolbar buttons now operate correctly on dockable windows.
- Annotate current is now displayed on subcircuit pins.
- Fixed problem where evaluated properties for SDL.OUTPUT and Publish to SDL were incorrect if Spice export was not done yet.
- Suffix "K" for kilo is now handled correctly.
- Editing property in "Edit User Property Value" window no longer gives identical callback warning twice.
- Unresolved cellviews are no longer stored in the database.

What's New in T-Spice v16.30

Miscellaneous New Features

- T-Spice now supports environment variables in path names. Environment variables may be referenced by %VARIABLE%, $VARIABLE, or ${VARIABLE}.
- Checkpoint-restart of transient analysis allows simulations to be repeatedly restarted from a checkpointed transient time.
- New HiSim version 2.8 transistor model.
- New HiSIM_HV versions 2.10 and 2.20 high voltage transistor models.
- T-Spice now sends warning and error messages to the S-Edit log window. Messaging can be enabled/disabled from a new T-Spice GUI Simulation toolbar button.
- New dialog input field Setup > Application… > External Programs > Digital simulator path provides a means of setting the executable path for the Verilog-AMS digital simulator.
- BSIM PARAMCHK model parameter default value has been changed to be assigned using **.option paramchk=[0|1]**.
- The T-Spice UI Simulation Manager now retains job information across application sessions. Control of this is available from **Simulation Settings > Output > Empty simulation manager list.**

Bug Fixes

- Improved DC convergence.
- New option autoconv=[0|1] (default: 1) enables a number of convergence improvement algorithms.
- Added DTEMP device instance parameter for BSIM4 models.
- Corrected behavior of .IC initial voltage conditions for DC sweeps.
- Aldec Riviera Pro digital simulator's dataset.asdb file is copied to the T-Spice simulation results directory at the completion of Verilog-AMS jobs.
- Corrected headers in the *.measure and *.monte output files for multi-sweep information.
- New option MACMOD enables substitution of subcircuit definitions for missing MOSFET model references, and vice-versa.
- New option MEASFORM changes the format of the .measure results file.
- Verilog-A/MS files can now be encrypted from the T-Spice File > Encrypt… menu and used in simulations.
- Corrected problems with equations that contain && (AND) and || (OR) operators without spaces or delimiters between variable names.
- Corrected the Monte Carlo seed parameter behavior to match the documentation description, such that a negative value results in a random seed value from the clock.
- Corrected HiSIM_HV pin current displayed values to include needed internal terms when resistor networks are in place.
- Added support for inductor IC initial conditions.
- Changed .measure errors to be warnings instead of fatal errors which would stop the simulation.

- Added standard diode device parameters to the Juncap diode, with mappings to native Juncap parameters as follows: AREA -> AB, PJ -> LS, PGATE -> LG.
- Corrections were made to handle forward references of subcircuit internal nodes, e.g. xsense x1.nodeQ senser …, where subcircuit x1 has not yet been defined.
- Corrected “no dc path to gnd” warnings and behavior to properly account for gshunt, cshunt, and other option settings.
- Corrected the flicker noise calculation for resistors and diodes.
- Corrected the .assert command to match model=mod_name when mod_name is a .model defined in a subcircuit.
- Corrected the Compile Verilog-AMS to not fail when the code is pure structural, containing only module instances with no operations.
- Corrected the .assert … duration=d command to correctly limit results to violations that last longer than d.
- The default value of the type parameter for Philips/NXP Juncap diodes was incorrectly -1 instead of 1.
- Corrected behavior when .print with no arguments is declared within a .subckt definition. Only print nodes and elements at and below that level, not full circuit.
- Subcircuit pin current printouts can now be made with i(instance_name, pin_name) syntax, e.g. .print i(xtop.xinverter,out)
- Improved Wavetool support for converting HSPICE multi-sweep and binary files
- Corrected crash on Windows/64 bit computers when simulating NXP/Philips models (Mextram, Diode500, …)
- The .assert command with node=name option has been corrected to rightly report the node name in violation messages.

What's New in W-Edit v16.30

- A new measurement function “measure pp” to measure peak to peak values has been added.

Bug Fixes

- Fixed a problem where the Y-axis was not rescaled to fit new arithmetic trace.
- Fixed problem where the Y-axis was not scaled properly for small data values.
- The "begin" parameter of absolutejitter now works correctly.
- Fixed a problem creating a parametric plot for Monte Carlo transient analysis.
- Improved Raw file import to auto detect and correct little/big endian byte order.

What's New in L-Edit v16.30

PyCells

- L-Edit now supports Interoperable Process Design Kits (iPDKs) using PyCell technology. iPDKs are vendor independent design kits for a particular process containing parameterized cells written in Python. These Python based cells are called PyCells. PyCells in L-Edit are only supported on Windows 64 bit at this time.

Enhanced T-Cell Parameters and Callbacks

- Two new T-Cell parameter types are now available, Radio and Cyclic. These are displayed as Radio Buttons and Drop-downs in the Instance and Edit Object dialogs. Boolean type parameters are now displayed as a checkbox.
- T-Cell parameters now have additional attributes, Use, Query, and Editable. Use and Query are TCL functions that control whether the parameter is displayed in the Instance or Edit Object dialog. Editable is a TCL function that controls whether the parameter is modifiable in the Instance or Edit Object dialogs.

- T-Cell parameters now support callbacks. A callback is a TCL function that is called when the parameter value is changed.
- L-Edit now provides a mechanism to automatically load tcl scripts when an OpenAccess databases is opened. A TCL file named autoload.tanner located in an OpenAccess library folder is automatically loaded when the library is opened. If autoload.tanner is not present, then a file named autoload.file, if present, is loaded. Callbacks are typically loaded via source commands in the autoload.tanner or autoload.file file.

Edit Object: Step though objects one by one

- The Edit Object dialog now has the ability to step through selected objects one at a time, by pressing the One by one.. button on the dialog, and then using the arrow buttons to step though the list of objects. Changes made in the dialog prior to pressing One by one… are applied to all selected objects when the One by one button is pressed, and cannot subsequently be cancelled. When the arrow button is pressed, changes in the dialog are applied to the current object in the dialog and cannot be cancelled. Options to highlight objects with markers as you step through include i) Highlight shape, ii) Display circle, and iii) Display cross hairs.

Hierarchical Find

- A new docking view control has been added, called Hierarchical Find. Using this control you can search for ports, labels, instances, vias, and unnamed objects throughout the hierarchy of the design. The scope of the search can be i) the current cell, ii) the current cell and hierarchy, iii) all cells in the current library, and iv) all libraries. Results are presented in a table. Selecting an item in the table will select the corresponding item on the layout, pushing into the hierarchy if needed. Options to highlight objects with markers as you select in the table include i) Highlight shape, ii) Display circle, and iii) Display cross hairs. The highlight options are stored in the registry at the application level.

Automatic Viewport Change

- A new setting has been added in Setup Application > Selection called Automatic Viewport Change, with options i) Leave view unchanged, ii) Pan to center of object(s), and iii) Zoom to objects. This setting applies when probing from S-Edit, when stepping through objects in the Edit Object(s) dialog, when selecting items in the Hierarchical Find report, and when highlighting errors in the Verification Navigator. The corresponding set of viewport options have been removed from the Setup Verification Navigator Options dialog.

Mouse Snap Grid: Separate X and Y and offset

- The mouse snap grid in Setup Design > Grid now has separate X and Y values for snapping different amounts in the X and Y direction. There are also X and Y offset values, so the snap grid may be offset from the origin.

Retarget Library of Selected Cells

- A new feature to retarget cells to a different library has been added to the Replace Instances menu in the Library Navigator. This feature retargets instances of selected cells in the Library Navigator to like named cell-views in a different library. The scope of the replacement is chosen from i) selections, ii) instances in the current cell, iii) instances in current cell and hierarchy, and iv) all cells in the current library.

Remove Reservation after Saving

- An option in Setup Application > general has been added to remove the reservation on a cell when saving an OpenAccess database. Options include removing reservations on either modified cells, unmodified cells, neither, or both.

OpenAccess Performance Improvements

- In OpenAccess databases, the Rename and Delete commands now allow selection of which libraries in which to check for references of the renamed or deleted cell, in order to retarget instances to the new renamed cell or to remove references to the deleted cell. This can significantly improve performance by reducing the number of cells that need to be loaded for the operation. For example, one can usually exclude checking PDK libraries from rename and delete operations, as one's design cells would not be instanced in the PDK.
- If an OpenAccess database is saved with the Library Navigator Filter set to Toplevel, or the Layer Palette set to "In Use in File", then these settings are ignored when the database is opened, as these settings force a load of all cells in the database.

SDL

- The SDL Router now supports different pitch and offset values for each routing layer. New columns for pitch and offset have been added to the Setup Design > Tech Layers dialog. If these fields are blank, then the value is taken from the values in the Setup Router dialog.
- The SDL router has improved warnings for missing ports, ports on invalid layers or ports that cannot be reached without violating design rules. There are also new error messages for invalid setup in Setup Design > Tech Layers.
- Fixed a problem where nets were being marked with a green check even if they were not routed to completion. This could occur when a there was a problem in the setup.
- Fixed problem in SDL netlist import where using the options "Remove device designator" together with "Insert multiple devices where M>1" did not always remove the device designator correctly.
- **Important Change:** Built in terminal names for primitive devices C, R, D and L in SDL Load Netlist parser are now PLUS and MINUS rather than CP/CM, RP/RM, DP/DM, and LP/LM. Ports in layout cells for these devices should now match the PLUS/MINUS names.

SPEF Extraction

- A Standard Parasitic Exchange Format (SPEF) file can now be extracted from SDL using the Parasitic Extraction (PX) engine. Invoke **Extract > Extract SPEF with PX…** from the SDL command menu.

Calibre Interactive Toolbar

- A new Calibre® toolbar implements Calibre Interactive, allowing one to launch Calibre jobs directly from L-Edit. It launches Calibre RVE, from which one can probe results back to L-Edit or S-Edit.

Jump from a Dialog to Help Documentation

- Pressing the F1 key while a dialog is open will open the documentation at the location of that dialog. Adobe Reader will open a new document each time. Foxit pdf reader has an option to jump to a new location in an already open document.

Japanese Translation

- Japanese translation of L-Edit user interface now includes dialog boxes and docking views. Some warnings and errors are also translated.

Miscellaneous New Features

- L-Edit now attempts to automatically determine the toplevel library when opening an OpenAccess database, and no longer presents the **Confirm Toplevel Library** dialog if the toplevel library can be determined. If the toplevel library cannot be determined, then the dialog is presented, listing only those libraries that are candidates for toplevel.
- L-Edit now supports environment variables in path names. Environment variables may be referenced by %VARIABLE%, $VARIABLE, or ${VARIABLE}.
- A new command, File > Database > Cell Reservation Report, creates a report showing which cells are reserved, each cell's reservation owner and the time the reservation was made.
- The Instance Location Summary Add-In now includes a column for the instance name.
- The order of layer palettes in the layer palette drop down can now be changed by pressing the Reorder button in the Setup layer Palettes dialog.
- Highlight Layout in SDL now displays the outline of wires, rather than the centerline.
- Nets in SDL may now be highlighted by selecting an object on the net, and invoking SDL Navigator > Command Menu > Highlight Selected Net. This can be faster than having to find the net in the SDL Navigator list of nets.
- A UPI command, LSelection_ConvertToCurvedPolygon(), has been added to convert an all angle polygon to a polygon with curved edges.
- An option is added to Setup Application > General to control if the active window is used, or a new window is opened when opening a cell.
- New UPI commands are now available for import and export of DXF (LFile_ImportDXF, LCell_ExportDXF) and Gerber (LFile_ImportGerberFolder, LFile_ImportGerberFile, LCell_ExportGerber, LCell_ExportGerberDrill).
- A new UPI function, LCell_GetParameterAsTime(), has been added.
- Setup > Import Technology can now import T-Cell parameters from CDF files.
- A new UPI command, LFile_ImportTechnology_GDSLayerMap, has been added to import a GDS Layer Map.
- A new UPI command, LFile_ImportTechnology_LEF, has been added to import LEF Technology.
- A name aliases can now be created when assigning a technology reference when creating a new OA design.
- A button has been added to the Filter edit control in the Library Navigator. The button indicates a history droplist if the edit field is empty; otherwise it is an X, and pressing it clears the filter edit field.
- A new tcl command, **workspace menu**, is added to create menu commands. Use **workspace menu –help** for details.

Bug Fixes

- DRC error markers no longer disappear when performing Edit in Place.
- When attempting to delete a layer that is used in a locked cell, L-Edit will no longer delete the layer, and will print a warning to the log window. Also fixed problems where layer names were deleted and replaced with auto-generated names.
- SDL Clock router no longer creates metal spacing errors.
- The Edit Object dialog on a custom via is now initialized with the pitch of the custom via.
- L-Edit no longer crashes, and gives a message, if a divide by zero is performed inside a T-Cell.

- The Copy Cell dialog will now initialize to the selected instance, if one instance is selected. If no instances selected, or more than one selected, then the Copy Cell dialog initializes to the active cell.
- SDL netlist import will now reuse existing auto-generated T-Cells if the parameters are matching rather than regenerating a new one.
- When deleting a layer, the layer name is now preserved if the layer does not actually get deleted due the option “Delete layer even if it contains geometry” not checked, and the layer has geometry.
- L-Edit command line now supports copy/paste of multiple lines of text.
- LVL Compare Layout Dialog now allows for longer Cellnames.
- Edit Objects of multiple boxes with "X Y corner and dimensions" editing no longer changes the size of the boxes.
- Align operation during Edit-in-place now correctly accounts for instance rotation.
- Angles no longer get rounded to the nearest integer when exporting tori to DXF.
- T-Cell generator code is now included when copying T-Cells across TDBs.
- Fixed problem in Node Highlight, where some area of a box is not highlighted correctly.
- "File > Import Mask Data > DXF/Gerber" functions are now available when a layout window is not open.
- DXF and Gerber Import/Export functions are now accessible from customized toolbars.
- Fixed problem in certain rendering options of a layer, a selected wire segment (or edge) becomes invisible.
- Draw >Boolean/Grow operations now produce correct results when display units are different from technology units.
- Multiple electrical ports selected and changed now prompts to change label in addition to same name as port.
- Fixed problems when the tech reference file is in a non-English named folder; i) the tech reference could not be opened, and ii) the error message is incorrectly decoded.
- Verification Error Navigator center view on error & zoom is now centering and zooming correctly on error in imported results database. Fixed problem handling “CN” comment lines.
- OASIS import and export now support file level properties.
- SDL Flylines no longer change color toggling a different net's flyline visibility
- SDL now logs an error message when LEF units and TDB resolution don't match.
- Fixed problem in snapping with Alt+M (force move).
- Manually deleting lock files in an OpenAccess database is not recommended, however L-Edit is now more robust and will no longer crash if a lock file is deleted while in use.
- When a UPI function modifies a cell, L-Edit will now attempt to obtain a reservation if the database is OpenAccess. If the reservation cannot be obtained, the UPI function may still modify the cell, but without a reservation the cell cannot be saved. Use the UPI function **LCell_GetLock** to prevent modifications locked or reserved cells.
- Fixed problem where Copy then Paste to Cursor would place instance randomly until cursor is moved.
- “Mark cells for flattening during DRC, Extraction and Node Highlighting” now creates a list on the cell to be DRC’ed of cells in hierarchy to flatten. This fixes problems in trying to mark locked cells and cells in TDB or OpenAccess libraries.
- Shortcut keys now work correctly when window is dockable
- Move Origin command no longer selects all objects after execution. Also no longer loads entire OpenAccess database.
- L-Edit is now printing rulers and coordinates correctly.
- Import of Oasis file now reads the resolution from the Oasis file.
- Fixed a problem where technology import from a TDB file was not importing all the layers.
- Blockages and Boundaries are now read from OpenAccess.
- Crashes and other problems with Layout Text Generator are fixed.

- In OASIS Import, fixed Type 0 repetition bug.

What's New in HiPer Verify v16.30

Miscellaneous New features

- HiPer Verify now supports environment variables in path names. Environment variables may be referenced by %VARIABLE%, $VARIABLE.
- The width of the cell selector tab in the Verification Error Navigator now stretches as the width of the Error Navigator is increased.
- DRC Error markers are now preserved when switching cells then coming back.

Bug Fixes

- Export Results from the Verification Error Navigator now writes results in a Calibre RVE compatible format.
- Fixed floating point comparison in Device definition macro code in Extract.

LVS

- New algorithm to find and short out parasitic elements, with improved memory performance.
- Improved performance merging diodes in LVS. We now avoid N**2 construction of merged element lists.
- A new command line option –Q will suppress processing information in the command line window when running LVS in batch mode.

What's New in HiPer PX v16.30

SPEF Extraction

- A Standard Parasitic Exchange Format (SPEF) file can now be extracted from SDL using the Parasitic Extraction (PX) engine. Invoke **Extract > Extract SPEF with PX…** from the SDL command menu.

Miscellaneous New features

- HiPer PX now supports environment variables in path names. Environment variables may be referenced by %VARIABLE%, $VARIABLE.

Bug Fixes

- Running HiPer PX no longer crashes L-Edit if environment variables are defined in the Calibre Defines field in Setup DRC.

Operating System Notification

- Starting with Version 16.30 Tanner EDA Tools is no longer supported on Microsoft® Window XP, Windows Vista, or RedHat® 4. Supported operating systems are Windows 7, Windows 8, Windows 8.1, RedHat 5 and RedHat 6.

Tanner Tools Version 16.25

What's New in S-Edit v16.25

- There are no changes in S-Edit v16.25.

What's New in T-Spice v16.25

Bug Fixes

- Changed the Philips/NXP Juncap diode model parameter TYPE to have a default value of 1 instead of -1, now matching documentation.

What's New in W-Edit v16.25

Bug Fixes

- There are no changes in W-Edit v16.25.

What's New in L-Edit v16.25

Bug Fixes

- The layout cell is now redrawn after an OpenAccess cell update operation.

What's New in HiPer Verify v16.25

- There are no changes in HiPer Verify v16.25.

What's New in HiPer PX v16.25

Bug Fixes

- Fixed problem where different devices with the same name can result in incorrect terminal layers for HiPer PX.
- Fixed several bugs to improve connectivity extraction in HiPer PX.

Tanner EDA Tools Version 16.24

What's New in S-Edit v16.24

- Vector printing of schematic hierarchy is no longer shifting in printout.
- Fixed problem in zoom out using the mouse wheel.

What's New in T-Spice v16.24

Bug Fixes

- You can now plot Verilog-A variables that are declared in the VA code with the format: (* desc="VDSAT" *) real VDSAT;
- 37361 Monte Carlo analysis results were only stored in the *.monte file for the final alter group
- Corrected Monte Carlo variations for parametric sweeps, which were re-sampling on inner sweep steps, rather than maintaining constant variations for each Monte sample.
- Corrected broken option modmonte behavior, where device-level variations were not working.
- Enabled the ability to sweep device and subcircuit M multiplicity term in parameter sweeps
- Fixed a frozen application problem caused by non-terminated comment line on input, /* comment */, missing */
- Corrected Verilog-A `include behavior to allow nesting of included files that lacked a trailing empty line.

What's New in W-Edit v16.24

Bug Fixes

- There are no changes in W-Edit v16.24.

What's New in L-Edit v16.24

Bug Fixes

- Wire Utilities no crash when used on a reserved cell.
- Custom via no longer loses its upper and lower layer setting after editing.
- Fixed crash if an object was removed from inside electrical port via Clear Layer command.
- L-Edit no longer crashes upon importing a CIF file.

What's New in HiPer Verify v16.24

Bug Fixes

- Fixed problem where DRC TOLERANCE FACTOR was incorrectly applied to orthogonal edges.
- Fixed missed error if violation distance was 0.001 Microns.
- Fixed problem in EXT, ENC, and INT where REGION option would create a triangle instead of a rectangle.

Tanner EDA Tools Version 16.23

What's New in S-Edit v16.23

- The command window is now made visible when there is a warning or error.
- Fixed problem where scroll wheel gets "stuck" when moved quickly.
- Fixed crash when instancing a cell by double click with Evaluation Mode turned ON.

What's New in T-Spice v16.23

Bug Fixes

- Incorrect sweep syntax in Spice file no longer causes the computer to hang.
- Currents are not plotted if the .print command is used inside the subcircuit and node name is not defined.
- BSIM-SOI AC small-signal parameters now include M multiplier scaling effects, as determined by option mout.
- A fatal error message “Bad Getparam() call” has been eliminated when probing terminal charges (.option probeq) of HiSIM_HV transistors.
- BSIM-SOI version 3.2 flicker noise calculation has been corrected.
- VHDL mixed-signal simulations failed in release v16.22 and are now working correctly.
- HiSIM_HV releases 1.24 and 2.01 are now available with several bug fixes.
- HiSIM release 2.61 is now available with several bug fixes.

What's New in W-Edit v16.23

Bug Fixes

- There are no changes in W-Edit v16.23.

What's New in L-Edit v16.23

Bug Fixes

- Made improvements in layout rendering performance on large layout. This could affect operations, such as pan, zoom, move, nudge, or anything that causes rendering of the layout.
- Improved drawing performance on large layout with large SDL netlist.
- Made improvements in rendering performance when drawing while edit-in-place.
- The Library Navigator no longer comes to the top when L-Edit is started, but now remembers it’s position relative to other docked windows.
- Fixed a problem when editing a vertex of an AA polygon causing snapping to unexpected points and mouse to not move smoothly on grid.
- L-Edit freezes when loading cells in OA database with paste to cursor turned on. The cause of the problem was the way that rulers were saved.
- LCell_MakeLogo inside T-Cell no longer crashes L-Edit.
- Save cell to TDB now only appends library name to end of the cell name when the unmodified cell name already exists in the target database.
- Improved slow saving to OA when there are many unnamed instances.
- Boolean dialog now gives focus to result layer so user can type in a new layer.
- LEF export now writes obstruction shapes from subcells.
- A warning in the SDL placer is now given for netlists that have collisions between net and instance names.

- Moving Origin now updates display as it should, regardless of state of update display in Setup Application UPI.
- Design Navigator cell tree no longer collapses after instancing a cell.
- The selected option in the Move By dialog is now saved and used to initialized the dialog the next time it is invoked.
- Prevent L-Edit from crashing when a tcell has a divide by zero error.
- Drawing temporary rulers now works correctly when markers are toggled off.
- File>Save Copy no longer requires creation of a new empty folder.
- L-Edit no longer freezes when a Boolean parameter in a T-Cell with default value "true" (small letters) is changed by pressing T or F keys
- T-Cell code is now saved when doing save operation after undo.
- L-Edit no longer pop-ups when selecting an instance in S-Edit, when L-Edit is minimized.
- LObject_ChangeLayer and LSelection_ChangeLayer now ignore instances and vias,and process labels.
- Fixed problem that cell boundary becomes too large when adding an electrical port while edit-in-place.
- Fixed problem where Layout rendering disappears when selecting an error when editing in place.
- Area calculator no longer triggers updating of all cells in an OA database.
- Fixed selection list problem that could cause a crash. Also fixed other crashes.

What's New in HiPer Verify v16.23

Bug Fixes

- Fixed crash when extracting multiple cells and "Open SPICE output file after extracting" is checked.
- LVS now uses tolerance setting correctly for X Elements.
- Fixed bug in PX integration leading to Extract failing with message “Netlist extraction fails because of an unknown reason”.
- Fixed bug in INT operation on edge layers leading to Extract failing with message “Netlist extraction fails because of an unknown reason”.
- Fixed false errors in Dimensional Check Operations when input layers are edge layers.

What's New in Tanner Tools Installation v16.23

Bug Fixes

- W-Edit now appears with the correct icon.
- Fixed problem running Support Utilities on Win XP 32bit machines.

What's New in Tanner EDA Tools for Linux v16.23

Bug Fixes

- LVS command in Linux no longer gives error "No relevant top-level circuitry to flatten", even when there is a top level circuit.

Tanner EDA Tools Version 16.22

What's New in S-Edit v16.22

- Fixed problem where Edited Property displays original value in property grid after switching to evaluated mode.
- Added -selected to database instances, ports, labels, netlabels and netcaps tcl commands.
- Fixed problem where File> Export Spice ignored the Export Control Property when in Evaluated mode.

What's New in T-Spice v16.22

Bug Fixes

- Removed Verilog-A additional information (instance name and file) that was printed with each $strobe output line.
- Corrected non-functional [Stop Simulation] button during transient preview simulations.
- Fixed improper aliasing of Verilog-A module internal node with containing subcircuit node of the same name.
- Corrected an erroneous “Verilog-A license failure” error message for users without Verilog-A licenses when a subcircuit definition is missing.
- Corrected AC analysis terminal current plot values for HiSIM_HV MOSFETs.
- Corrected a crash when a node name contain a colon :
- Subcircuit pin currents can now be used in .measure statements and print expressions, e.g. .print tran ‘ddt(i2(Xosc))’ ; .measure tran I2_Avg avg i2(Xinverter)

What's New in W-Edit v16.22

Bug Fixes

- There are no changes in W-Edit v16.22.

What's New in L-Edit v16.22

Bug Fixes

- L-Edit no longer freezes when cursor is placed on Tools>SDL Navigator>LEF/DEF.
- Fixed Cell name control in WaferTools Die Map dialog.
- L-Edit titlebar now correctly displays cell and design name when layout window is maximized.
- Reordering T-Cell parameters now takes effect immediately, without changing anything else.
- Delete key now works in T-Cell Edit Object(s) dialog.
- Fixed problem in which L-Edit incorrectly gave message that array was too big.
- Fixed problem in the direction that an edge moved using the Move dialog. Also fixed direction of move when inside an Edit-in-Place.
- Ripup Net no longer deletes the objects inside a port.
- In an OpenAccess database, changing extract spice output filename now sets cell changed flag.
- Fixed crash after Align operation when multiple designs open.

- Fixed crash reading tdb file that has a label with data type greater than 256 or a net name associated with it.
- Fixed L-Edit crash when scrolling the mouse wheel while the mouse is not over L-Edit.
- Fixed buffer insertion in SDL which would sometimes drop connections to a few cells. Fixed clustering obey the number of target fanouts properly.
- Fixed problem where "File info" information is not saved when a tdb file is saved by "File > Save as".

Note:

- When using L-Comp, the function LC_InitializeState() can malfunction when multiple designs are open. It will use the active window, which is not necessarily associated with the intended design. When writing L-Comp code, it is recommended to use LC_InitializeStateFromCell(cellCurrent) instead. All newly created T-Cells will use this function automatically. LC_InitializeState is deprecated and will eventually be removed.

What's New in HiPer Verify v16.22

Bug Fixes

- Output files from the RDB option of the DENSITY and NET AREA RATIO commands are now placed relative to the database folder, if a full path is not given.

What's New in Tanner EDA Tools for Linux v16.22

Bug Fixes

- There are no changes in Tanner EDA Tools for Linux v16.22

Tanner EDA Tools Version 16.21

What's New in S-Edit v16.21

- Boolean properties in the properties grid now have a drop list with "True", "False", and "Expression" options. When "Expression" is selected, a dialog box appears offering the ability to set an expression as the value of the property.

What's New in T-Spice v16.21

Bug Fixes

- Corrected Monte Carlo variations within duplicate subcircuit instances to ensure proper device mismatch sampling.

What's New in W-Edit v16.21

Bug Fixes

- There are no changes in W-Edit v16.21.

What's New in L-Edit v16.21

Bug Fixes

- Fixed crash in after moving a point port while edit in place.
- Fixed crash in certain circumstances after drawing 45 or AA persistent ruler.
- Fixed GDS import of arrays with 90 degree rotation, when y delta value is stored before x delta value.
- Library Navigator no longer switches to a different design when performing Update or Save All.
- "Save cell as TDB file" now works correctly when cells have same name but different libraries.
- The Library Navigator may not be placed undocked, to prevent problems that occur when it is undocked.
- Loading new design in L-Edit now makes the new design the active library in the Library Navigator.
- The mouse wheel may now be used to scroll through custom Layer Palettes when placed over the Layer Palette drop down.
- Fixed problem where if L-Edit crashed with an OA cell reserved, then after restarting L-Edit user could no longer get a reservation on that cell.

What's New in HiPer Verify v16.21

Bug Fixes

- Fixed problem where results cell selected in Verification Error Navigator would change after selecting a violation, after importing in verification results from a file.
- Verification Error Navigator Import results dialog now remember the last file loaded.
- Net names are now written to the RDB file when using box ports. (Known issue: When multiple ports are on the same net, the net name will not be written to the RDB file)

What's New in Tanner EDA Tools for Linux v16.21

Bug Fixes

- Fixed crash in W-Edit when clicking on "View traces hierarchically", and "Include other traces"

Tanner EDA Tools Version 16.20

What's New in S-Edit v16.20

Cross Probing and Selection Synchronization

- Probing a net or a device from Schematic to Layout has been improved with the introduction of two new features in S-Edit, Layout Probe and Synchronize Schematic Selection. Selecting "Layout" from the probe pull down menu and pressing the “probe to Layout” button, you can click on instances or nets in schematic, and the corresponding instance or net will be highlighted in layout, and L Edit will pop to the front. If Layout probe is not selected but "Synchronize Selection" icon is in locked state, then selecting an instance in net in schematic using the normal selection methods will select the corresponding instance or net in layout, but L-Edit will not pop to the front.

Property Editing and Display Enhancements

- Properties may now be edited while in Evaluated mode. This allows one to operate S-Edit in evaluated mode continuously, without having to constantly switch between evaluated and non-evaluated mode.
- A new service property called “Query” has been added to control the display of a property in the property navigator. Only properties whose Query value evaluates to True will be displayed in the property navigator when in Evaluated mode. A new “Show Query” button in the property navigator toggles the display of all properties or only those with Query equals True.
- A new service property called “Editable” has been added to control the editability of a property when in evaluated mode. Only properties whose Editable value evaluates to True will be editable in the properties navigator when Evaluated mode is on.

Evaluated Labels

- Evaluated labels are supported in v16.20. A Boolean service property on the label called “Evaluation” controls whether a label is evaluated. On import of Cadence databases, cdsName, cdsParam, and cdsTerm labels are now preserved as evaluated labels.

IPL Callbacks

- IPL Callbacks are supported in S-Edit v16.20.

Miscellaneous New features

- A new tcl command has been implemented to stretch or squeeze the width of text in S-Edit. The syntax is “setup schematictext set -stretch <stretchvalue>” and applies globally to all text on schematic or symbol views. The command may be put into a script for autoloading each time S-Edit is launched.
- A new tcl command has been implemented to change the font in S-Edit. The syntax is “setup schematictext set -fontface <font name>” and applies globally to all text on schematic or symbol views. The command may be put into a script for autoloading each time S-Edit is launched.
- In Setup Simulation dialog, "Data" option has been added for transient, dc, ac and parameter sweeps.
- A new toolbar button has been added in S-Edit called “Publish to SDL” Pressing this button exports the netlist out of S-Edit in imports it into L-Edit/SDL.

- Text Labels with Direction = Up, which display text from bottom up when vertical, now display text right side up when in a symbol that is rotated such that the text is horizontal.

Bug Fixes

- Unresolved references no longer get saved to a new library with "_unresolved" added to the name. Unresolved references may therefore be easily repaired after the design is saved.
- Flat SPICE export in S-Edit now handles the "m" parameter correctly by writing multiple subcircuit instances.
- Fixed problem where snap to grid would remove all hotspots and solder points.
- Edit->GoTo line menu now works on veriloga or verilogams views.
- Fixed incorrect text orientation in vector printing of instances with 270 degree rotation angle.
- The MasterCell drop down field is now sorted alphabetically.
- Fixed crash when using the modulo operator % in a property expression. Need to the the escape character (backslash) before %.
- Fixed crash when deleting a cell while pushed into an instance in that cell.

What's New in T-Spice v16.20

Miscellaneous New features

- The temperature of a simulation is now always displayed on the header of the Simulation Status window.
- New transient ramp mode is similar to powerup mode except ramping is performed prior to time zero. Usage: .tran timestep stoptime ramp [=ramptime]
- Added resistor model parameter T_ABS, absolute temperature, which is used in some foundry model libraries.

Bug Fixes

- Improved the .warn command behavior to apply to all warning message, including Verilog-A/MS messages
- Corrected .IC assigned values to support expressions when in a subcircuit context
- Corrected .noise listcount=n to list all noise devices that have exactly equal contributions; previously only the first was listed
- Corrected Philips MOS 11 and PSP model crash when binned model name has a numeric name extension (i.e. modelname.1)
- Added error detection for invalid, less than absolute zero, .temp and tnom values
- .IC and .nodeset commands are now re-evaluated at each parameter sweep step, so that value expressions may be dependent upon the sweep variable
- Updated the RPI a-Si Level 15 TFT model with new equations for scaling certain terms according to transistor size W/L
- Corrected some device thermal noise calculations to include dtemp device delta temperature effects.
- Corrected diode ID noise calculation which was sometimes negative, causing undefined total noise values.
- Fixed a problem where if a Verilog-A module is instanced repeatedly within a subcircuit, all instances will have the device parameter values for the first instance.
- Updated the RPI a-Si MOS level 15 equations to include transistor size scaling of leakage current terms
- User-defined functions in .subckt blocks were not processed after the first instance of the subcircuit, resulting in a parse error

- Fixed problem where parameter value was incorrect in corner simulations. The problem was unique to the situation where the .param name is defined twice (redefined) within an alter block, and then changed in a future alter block.
- Incorrect results for the first point in temperature sweep has been fixed.

What's New in W-Edit v16.20

- Fixed crash in W-Edit when "Find Maximum" button is pressed.
- Changed syntax of “measure fft” command to make DCremove argument truly a flag. Instead of using “-dcremove 1” to remove DC trace, just “-dcremove” does it.

What's New in L-Edit v16.20

Cross Probing and Selection Synchronization

- Probing a net or a device from Layout to Schematic has been improved with the introduction of two new toolbar buttons in L-Edit, Layout Probe and Synchronize Schematic Selection. Using the probe tool you can click on instances or nets in layout, and the corresponding instance or net will be highlighted in schematic, and S-Edit will pop to the front. With Synchronize Selection, selecting an instance in net in layout using the normal selection methods will select the corresponding instance or net in schematic, but S-Edit will not pop to the front.

Schematic Driven Layout - Assisted Routing

- A new mode called **Assisted Routing** is now available in the SDL Navigator that enables a number of productivity enhancements when performing manual routing using SDL.
    - When the mouse is placed near a pin, a bulls eye shaped snap point is shown on the pin and drawing will snap to the center of the pin.
    - When the mouse is placed over a pin, the net, pin name with instance hierarchy, and layer of object in the pin are displayed on the status bar.
    - Starting a route at a pin marks that pin with a check in the SDL navigator, and places the object on the same layer as the pin. All geometry drawn for that route will be tagged with that net. Ending a segment on a pin marks that pin with a check in the SDL navigator.
    - A flyline is rendered from the current mouse location to the target pin Flylines are shown in the color of the layer of the target pin. The target pin is automatically chosen, however a hotkey, “*”, can be pressed to change the target pin to the pin closest to the current mouse location.
    - When routing a net, alignment snap points are displayed to show horizontal or vertical alignment with each object in the target pin.
    - If Interactive DRC is turned on, then crossing geometry in the current cell on a different net will cause the flyline to change color to indicate that a short has occurred.
    - Green checks in SDL are updated by SDL Command Menu > Extract > Check Connectivity.
- A new toolbar button has been added in S-Edit called “Publish to SDL” Pressing this button exports the netlist out of S-Edit in imports it into L-Edit/SDL.

Miscellaneous New features

- The Selection Details report now displays the list of labels and ports by name.

Bug Fixes

- L-Edit now handles repetitions of “Type 0” correctly for Oasis import
- Fill Shape With Rows crashes L-Edit if the placement site contains only a port.
- SDL Check Connectivity now lists the instance name and pin name for unknown pin warnings.
- Alignment functions new treat electrical ports (test and shapes) as a single object.
- GDS Import is now able to recover from a syntax error in the GDS file in which the end struct before the next begin struct is missing.
- The view name can now be selected in the Compare Layout Dialog.
- Placing via array using shift +] no longer places vias offgrid
- Fixed problem where the router flips horizontal/vertical layers if the first layer is disabled for routing.
- Improved performance reading data back into L-Edit upon completion of autorouter.
- MultiGrid toolbar values are now correctly saved in the registry.
- Fixed problem in Find Object dialog with Match whole names only option.
- Added datatype option for TCL layer command.
- Layout Text Generator no longer crashes L-Edit.
- Performance slowdown of selecting objects on large layout is fixed.
- Fixed problem where in some cases assignment of keyboard shortcut works differently after close/reopen of L-Edit.
- Layer name is no longer limited by the window size in the Copy/Add Layer and Mask Bias dialogs.Fixed I/O error if GDS file path is different from TDB file path.
- Fixed problem where Circle, Pie and Torus toolbar buttons did not appear when L-Edit is started in certain circumstances.
- Fixed problem where LFile_SaveAs would save file before loading of cells for OA database is completed.
- SDL netlist import now only issues warnings for the subcircuit being imported, not for the entire netlist.
- Route power rails now allow entry in only left or only right side by leaving the field for the side you don’t want to route blank.
- Ctrl+PageDown now works on arrays with negative delta.
- Fixed crash after performing Cell Copy on the same cell twice in succession, with retarget instances selected.
- LEF Export now writes orthogonal wires and polygons as well as boxes.

Note:

- There is a known issue that when the Library Navigator is undocked, then after clicking in the Library Navigator, then menus and other docked views will no longer function. It is recommended keep the Library Navigator docked.

What's New in HiPer Verify v16.20

Miscellaneous New features

DRC/Extract

- Speed of command file parsing and syntax checking has been improved.
- HiPer Verify can now parse (and ignore) the LVS PROPERTY INITIALIZE command.

LVS

- Running LVS from batch file now gives an error message if another instance of LVS is already running.
- The LVS prematch file now accepts a single column of node names in the list of nodes to match. If a single column is present then LVS will compare the same name on both the schematic and layout side. The list of toplevel ports in layout may easily

be obtained using the Selection Details report in L-Edit, which now lists the names of ports and labels.

Bug Fixes

- Fixed crash in L-Edit reading results data upon completion of HiPer Verify.
- In HiPer Verify Extract, the Cumulative Top Level device count now reports the device count as if the circuit were flattened, rather than the sum of devices in each subcircuit.
- R and C in the CDL netlist is now parsed correctly.
- HiPer Verify no longer reports false error if NET AREA RATIO expression involves division by zero.

Operating System Notification

Tanner EDA Tools v16.2 will be the last release of Tanner Tools Supporting Window XP.

Tanner EDA Tools Version 16.12

What's New in S-Edit v16.12

Bug Fixes

- Fixed problem importing OpenAccess schematic containing a SimInfo export but no views named “symbol”.
- Saving a design for the first time after loading no longer takes more time than subsequent saves.
- When cells with the same name from different libraries are written to SPICE, the library name is now appended to the cell name to make the names unique.

What's New in T-Spice v16.12

Bug Fixes

- Modified the ddt() function to return 0 rather than an invalid real value when analysis type is not transient.
- Corrected conditional functions (if(c,a,b) and c?a:b) which could under some circumstances return an incorrect value due to plot terms in the clauses.
- New function has been added: limit(value, min_value, max_value).
- Modified diode expli behavior to scale for very small IS saturation current density effects.
- Fixed a problem with .measure results not being printed for multiple analysis simulations.

What's New in W-Edit v16.12

Bug Fixes

- There are no fixes in W-Edit v16.12.

What's New in L-Edit v16.12

Bug Fixes

- Fixed problem introduced in v16.10 where shoRenaming target cells in Cell Copy operation no longer crashes L-Edit.
- Fixed problem where illegal OASIS was written when input polygons had duplicate points.
- In Edit Object dialog, you no longer need to click twice to uncheck the “Locked” or “Mirror” options.
- Fixed crash that sometimes occurs when opening a design with net names.
- Focus now remains in layout window after performing operations such as selecting a layer, instancing, and Edit Object.

What's New in HiPer Verify v16.12

Bug Fixes

- LVS no longer crashes when running in batch mode.

- Fixed parser of permutable terminals. It was incorrectly including the comma in the terminal name, instead of considering it a separator.

What's New in EDA Tanner Tools for Linux v16.12

Bug Fixes

- Many user interface bugs on Linux have been fixed in S-Edit, L-Edit and W-Edit.

Tanner EDA Tools Version 16.11

What's New in S-Edit v16.11

Bug Fixes

- Verilog parser now parses words that begin with “end”, such as “endcase” correctly.
- Valid values of “radio” type parameters are now imported by OpenAccess import.
- Export image no longer crashes S-Edit.

What's New in T-Spice v16.11

Bug Fixes

- Current-Controlled Current Source AC current plot values have been corrected.
- Corrected an error introduced in T-Spice v16.10 - when a .subckt pin name is the same as a global node name (gnd, gnd!, ground, or a .global node) then the global node was used for connections within the subcircuit, rather than connecting to the pin.
- Restored behavior that was previously available but lost in v16.10 – allow .param definitions to be recursive (self-referencing) as in .param vto_n = ‘vto_n + .5’

What's New in W-Edit v16.11

Bug Fixes

- Fixed crash when switching language from Japanese back to English.
- Fixed problem when zooming, sometimes some of the traces are not displayed.
- Fixed problem where Shift + Drag + Drop did not create text label.

What's New in L-Edit v16.11

Bug Fixes

- Ripup nets in SDL now removes the vias placed by manual routing.

What's New in HiPer Verify v16.11

Bug Fixes

- Batch LVS now handles -1 and -2 options (layout cell and schematic cell) correctly.
- LVS now parses Verilog files with Japanese folder names.

What's New in Tanner Tools v16.11

Bug Fixes

- Missing tcl8 folder is now installed. This fixes problems running tcl commands.

Tanner EDA Tools Version 16.10

What's New in S-Edit v16.10

Import OpenAccess

- Schematics can now be imported into S-Edit from an OpenAccess database. The schematic is still saved in the current S-Edit database format. For OpenAccess from Cadence the import can translate Cadence cdsParam properties from the cdfDump files.

Schematic – Layout – LVS – Waveform Cross Probing

- Cross probing of nets, instances, and views is now possible in both directions between S-Edit and L-Edit. To probe a net from S-Edit to L-Edit, select a net in S-Edit, then slow right click and choose the Jump to option. To probe a net from L-Edit to S-Edit, select the net in L-Edit and invoke Tools > Jump To. Probing instances behaves in a similar manner. Geometry in L-Edit must be tagged with net information in the SDL environment in order to jump to nets.
- Probing a trace from W-Edit can now jump to the corresponding net in S-Edit.

Miscellaneous New features

- A new Snap to grid feature is available in S-Edit to snap objects onto the grid. The scope of operation can be chosen from selections, cell, design, or all libraries.
- Pressing the F6 key now provides an easy way of running TCL file that is already open and active.
- The “workspace bindkeys” tcl command can be used to report and set key bindings. The "workspace" subcommands "toolbar", "bindkeys", and "dockinglayout" should allow the UI to be customized and transferred between users.
- The “workspace getactive” tcl command can be used to retrieve the library, view name and interface name of the top level cell, and other information. Use workspace getactive – help for full details.

Bug Fixes

- Fixed problem where one could not save copy of design to a folder that is one level above the design folder.
- S-Edit now exports netlist using MEG instead of X for mega unit.
- VERILOG.PRIMITIVE = True now prevents empty cell definitions from being exported to the Verilog file.
- Copy Cell dialog now gives clear indication of source and destination libraries when multiple projects are open.
- Copy Cell with Overwrite option now completely replace the cell being over-written, including all properties.
- The Save modified Libraries dialog now clearly names of modified libraries when the same library name is used in different designs.
- The properties "Pages" and "PageNumber" are now evaluated.
- Fixed problem where current probe gave "Unknown term" error in W-Edit when probing on a subcircuit pin.
- Fixed 'Setup Simulation' dialog opening when working in “Run with no analyses" chosen.
- Fixed problem when you push into verilog/spice view and make changes, the changes are not saved when you pop out of context. Similarly, changes to verlilog

and Spice views were not saved when using forward and back buttons to switch views.

What's New in T-Spice v16.10

- Improved performance of DC/Parameter sweep simulations when the circuit contains large amounts of hierarchy with equivalent subcircuit instances
- Improved performance of DC sweeps when the sweep variable is also a .param, e.g., .DC Vin 2 4 0.1 where .param Vin=3v.
- Juncap diodes can now be used as the internal bulk-drain and bulk-source junction diodes for BSIM3 v3.3 and BSIM4 v4.7 transistors. This feature is enabled with the .model juncap=2 parameter (0 = use native BSIM diodes, 1 = Juncap 1 diodes, 2 = Juncap 2 diodes, default value: 0). Standard Juncap diode model parameters can be included in the BSIM .model card.
- Error and warning messages have been improved to always include the file name and line number where the violation occurred.
- Added support for hierarchy of .subckt definitions, i.e. subcircuit definitions may be locally defined within other subcircuit definitions
- Allow Verilog-A/MS files to be pre-compiled and stored as a database, then reused quickly from subsequent simulations
- Allow printing of subcircuit pin currents, e.g. .print i1(x1.xcontroller)
- New .warn command provides a means of suppressing or modifying the behavior of unwanted or unimportant warning messages.
- Precompiled Verilog-A models are included to support R2_CMC and R3_CMC resistors, HICUM bipolars, and BSIM6 and BSIM-CMG MOSFETs.

Bug Fixes

- Corrected diode transit-time and knee current derivative terms for improved convergence and AC analysis.
- When BSIM devices have parameters SA, SB, and SD set to zero, handle it as unassigned values and do not evaluate the stress effect equations.
- Allow voltage controlled current and voltage sources, g and e devices, to have expressions involving VCCS and VCVS currents, e.g. cur='-i1(e1)'
- Corrected problems plotting .data variable values
- Allow a library section to be both deleted (.del lib my.lib typical) and added (.lib my.lib typical) within a .alter block
- If a MOS device has parameters SA, SB, or SD set to zero, handle as unassigned values
- Added support for .assert option level=notice
- Corrected .assert command problems with the mod=name argument, to ensure that only devices using the named model are processed
- Fixed crash when processing .ic and .nodeset commands involving internal node or device names
- Issue an error message if analysis commands contain more than one outer variable sweep, rather than silently ignoring
- Corrected .option tolmult scaling of convergence tolerances, which was repeatedly accumulated for simulations with outer variable sweeps
- Improved the performance and memory usage for the parsing and setup stages of large circuit simulations
- Label the initial (.alter=0) simulation block from the .title command setting
- Corrected the initial time=0 state of BSIM4 internal variables when .tran simulation is performed without a .op request
- Corrected the .assert when=setup behavior to work with .alter blocks
- Corrected .step in combination with .dc sweeps of voltage sources to properly sweep all specified values

- Fixed .param expression values that involve a complicated interaction of .data sweep variables and .alter block param changes
- Fixed .step behavior when the variable values are assigned from a .param which is subsequently changed in a .alter block
- Allow .temp values to be assigned from .param values or expressions
- Ensure that plotting .measure results is correct and consistent with equivalent .step and .DC outer sweeps
- All NXP (Philips) models can now be referenced using either the HSPICE or the NXP numbering system for LEVEL and VERSION. E.g. The latest MOS Model 11 release is LEVEL=63 VERSION=1102.1 or LEVEL=11021
- The device instance parameter area=value can now be abbreviated to a=value for diodes, mesfets, jfets, and bipolars.
- The shmod=[0,1] model parameter has been added to MOS Models 11 and 20 for enabling and disabling the self-heating equations. All T-Spice models that have self-heating equations now include shmod model parameter support.
- Corrected a bug in which certain forms of DC sweeping with outer parameter sweeps failed with a Verilog-A compile error.
- Corrected sweep hierarchy issues so that multiple .step sweeps plus .dc or .tran outer sweeps are handled consistently and correctly.
- Support input filenames and paths consisting of international character sets, e.g. Japanese.
- Verilog-A code that contains file open operations such as “$fopen(“filename.txt”, “a”);” should be changed to the equivalent ““$fopen(“filename.txt”);” in order to support multi-threaded access and multiple simultaneous files open.

What's New in W-Edit v16.10

Waveform Comparison Tool

- A new waveform comparison tool is available in W-Edit. The tool compares multiple traces between two simulations and indicates whether they match or are different, and can give a detailed report of differences. The comparison builds on the measure diff command, and all options and tolerances from the measure diff command can be used.

New Measurements

The following new measurements have been implemented:

- **measure diff** — The “measure diff” measurement compares two traces at a time, reporting either a binary “match/differ” result, or a more detailed point-by-point comparison.
- **measure cpk** — The “measure cpk” measurement calculates an indicator of the process capability for a waveform relative to specified upper and lower limits.
- **measure dpu** — The “measure dpu” measurement calculates the total number of defects per unit based on the points in a waveform. Given one or both of an upper and lower specification limit, the dpu is calculated as the area under a normal distribution that falls outside the specification limit(s). The mean and standard deviation of the normal distribution are equal to the mean and standard deviation of the points in the waveform.
- **measure stddev** — The “measure stddev” measurement calculates the standard deviation of a waveform. This measurements intended for statistical (discrete) data such as histograms.
- **measure yield** — The “measure yield” measurement calculates the ratio of the number of data points between the Y-axis levels Upper and Lower relative to the total number of data points.

Performance Improvements

- Performance improvements have been made for common operations on large databases.

Miscellaneous New features

- Trace can now be exported from W-Edit in SPICE PWL (piece-wise linear) format.
- Text Labels can now be copied from one chart to another.

Bug Fixes

- Fixed error when removing multiple simulations.
- Initial 'Move Plot' from right click menu is now correct for upper and lower plots.
- Fixed problem where Waveform calculator inserted incorrect expression in AC plots.
- Fixed problem where sometimes the Trace Style option is grayed out.
- Cursor values are now updated when cursor is moved from one extreme to another.
- Chart compatibility is now checked correctly when probing a trace from DC sweep simulation while the transient chart is already open.
- Fixed W-Edit crash when moving cursor with cursor toolbar set to auto-hide.

What's New in L-Edit v16.10

Standard Cell Placer and Clock Router in SDL

- A new automatic Standard Cell placer is now included in SDL. The placer is driven by a Spice, CDL, or Verilog netlist and a LEF description of the standard cells. SDL can also read and write LEF/DEF files.
- The auto router has been enhanced with clock tree routing and buffer insertion to minimize skew of clock nets.
- Performance of the SDL navigator has significantly increased for large nets, and overall capacity and completion rate of the router has improved. Performance opening tdb files with large number of objects placed by the router has improved, and performance of rip-up-all-nets has improved.
- A new “Tech Layers” tab in Setup Design now contains routing, pin, and keepout layer information. Default purposes for creation of routing, keepouts, and pins are also specified.
- An SDF file can now be written for layout in the SDL environment. Use SDL Command Menu > Extract > Write SDF…
- A Verilog netlist can now be written from SDL.

SDL Short and Open Connectivity Checker

- A new connectivity checker is available in SDL (SDL Command Menu > Extract > Check Connectivity). When a netlist is present in SDL, the connectivity checker is able to verify that connections are correctly made between instances in the current cell, and is able to identify shorts and opens. The SDL Connectivity Checker will also assign net names to untagged geometry, based on the netlist in SDL

OASIS Import/Export

- L-Edit is now able to import and export the OASIS mask format.

Locked Instances

- The position of instances in L-Edit can now be locked by setting a “Locked” checkbox in the Edit Objects dialog. A setting in Setup Application > Selection controls whether locked instances may be selected.

Toolbars

- Toolbars in L-Edit no longer get rearranged when the application is resized, minimized/maximized, etc. Toolbars can now be customized using the dropdown to the right of each toolbar, and new custom toolbars can be created with user chosen buttons. The appearance of toolbars also respect Themes (Windows > Theme).
- The arrangement of Toolbars in v16.10 will NOT inherit arrangements from previous installed versions. Once customized, however, the arrangement will be preserved.

Miscellaneous New features

- L-Edit can now open GDS files directly, without having to import into an existing database. Use File > Open and browse to the GDS file. GDS files can also be opened in L-Edit by drag-and-drop, and double click.
- A new option to move an AA edge in perpendicular direction while preserving the length of the edge has been added to the existing capability to move an AA edge in perpendicular direction while preserving the angle of adjacent edges. Behavior is controlled by an option in Setup Application.
- The Draw > Move By command has been enhanced to allow moving a single selected edge by a specified amount in a perpendicular direction.
- An option has been added to the to the delete dialog to not delete a cell if it is instanced somewhere in the design.
- A new UPI command, LCell_MakeLogo, is available to run the Draw > Layout Generators > Layout Text Generator command.
- An option has been added to Gerber export option to export wires as polygons (RS274X only).
- The Find command now has a Find Net option, which will select polygons on the chosen net. Polygons are tagged with net info either by routing using SDL or by next extraction in SDL (SDL Command Menu > Extract > Check Connectivity).
- L-Edit now prevents cell names being created with space, asterisk, and colon. These characters are used internally as separators for library:cell*view names.
- The new “workspace toolbar” tcl function can be used to show and hide toolbars, and can be bound to a button.
- The "workspace" subcommands "toolbar", "bindkeys", and "dockinglayout" should allow the UI to be customized and transferred between users.Copy cells across designs can now be done in v16 without adding a library, if both designs are open in L-Edit.
- "Fracture Polygons" is now an option in the Generate Layers dialog.

Bug Fixes

- Cell list in Libraries Navigator now stays in place when deleting a cell.
- SDL now matches port names and pin names in a case-insensitive manner.
- Improved parsing of Gerber written by Cadence Allegro, in which coordinates written with implicit decimals are written incorrectly.
- Ripup all nets is now working correctly in “By Instance” view.
- Cells imported from GDS file should be shown as bold.
- Object Snapping to Round Join or End style wires no longer crashes L-Edit.
- Boolean operations now correctly handle wires with round ends/joins.
- Generate Layers, Boolean Operations, DRC, and Extract can now operate on wires with more than 8190 segments.

- Place Via command, “[“, and “]”, now place vias at the correct location when in Edit in Place mode.
- Fixed problem using an EDIF netlist in SPR, which presented a message stating “There was no TDB standard cell library selected”.
- Unresolved autogen cells are now always displayed with and “X”. Fixed problem where T-Cells in code format would not be displayed as an “X” if there was an error in execution.
- Instance of via cells are now correctly saved when performing Unreserve and then selecting Save.
- Fixed problem where an OA database cannot be saved on a shared drive if the user doesn't have full permissions.
- Fixed problem where SDL Router hangs on net with electrical port containing a polygon.
- Fixed a problem in conversion of v15 vias to stdVias and custom vias that occurred in certain circumstances.
- Fixed crash in L-Edit when trying to save a tech library that contains 'tech.tdb.cdslck' file.
- Clear Markers now works correctly while in Edit in Place.
- Memory leak in L-Edit when exporting a GDS file is fixed.
- Fixed crash when invalid layer-purpose-pair name entered in dialog.
- Copy cell with Copy Hierarchy option now correctly updates instances in the target cell to reference the copied hierarchy.
- Curve Tools Chamfer and Fillet now give correct results on wires. Also fixed problem where some polygon vertices would not get filleted.
- The “Consider multiple edges as single edge” and “Only consider vertices whose angle is” options have been removed from the fillet/chamfer tool. In many applications where these options would be used, it is better to first convert the all angle polygon to a curved polygon, and then use fillet/chamfer.
- View > Pan > Object pan now works when cell is locked.
- Changing layer palette by UPI now gives same as changing by mouse.
- Die labeler inserts correct spacing between characters.
- Clear Markers not working when edit-in-place
- Fixed surround problem in guard rings.
- Fixed problem when ports (or labels) are on more than one layer, and some of the ports are on a hidden layer, then in certain conditions you can’t select the other ports that are not on hidden layers.
- Added support for vias inside ports.
- Fixed crash on exporting long port names to CIF.

What's New in HiPer Verify v16.10

Parasitic Extraction

- HiPer PX parasitic extraction is now integrated with HiPer Verify Extract. Devices are defined in the HiPer Verify command file and are extracted by HiPer Verify. Hiper PX calculates parasitic resistances and capacitances. A single run invoked from the L-Edit user interface extracts devices and parasitics and produces a single combined netlist.
- The stand-alone Parasitic Extraction tool has been moved to Tools > Add-Ins > Legacy Parasitic Extractor.

LVS

- The LVS user interface is now available in Japanese. Also, LVS now supports Unicode net and element names.
- LVS now supports Structural Verilog netlists.
- LVS now allow users to specify which subcircuit in the netlist to compare.

- Empty subcircuits or modules are now automatically defined as primitives. If you want to ignore these elements, use the "Remove device models named:" option on the Parasitics tab.
- Probing is now supported from LVS error results to S-Edit/L-Edit.

Command Line DRC and Extract

- DRC and Extract can now be run from the command line. Calibre and Dracula command files, as well as Tanner's XML format command files, can be run on GDSII layout databases. The command line application can also be used to create a Tanner XML command file format from a Calibre or Dracula file.

Enahancements

- The BY NET option is now supported for CUT, ENCLOSE, INTERACT and TOUCH commands.
- The EVEN/ODD options are now supported for CUT, TOUCH, ENCLOSE, INTERACT commands.
- The SINGULAR ALSO and SINGULAR ONLY options are now supported for the INTERACT command.
- The REGION CENTERLINE option is now supported for dimensional check operations.
- Performance of the ANGLE operation has been improved on hierarchical layout.
- Performance of the SHRINK operation has been improved on hierarchical layout.

Bug Fixes

- CORNER TO CORNER errors are now correctly flagged.
- ENCLOSE command now handles with donut shape correctly.
- Error parsing RECTANGLES command with INSIDE OF option is fixed.
- Fixed false and missing errors on ABUT option of INT, EXT, and ENC operations.
- Fixed false errors in INT, EXT, and ENC due to hierarchy.
- Fixed missing error for OUTSIDE ALSO option of ENC operation.
- Fixed missing error for PERP option of EXT operation.
- Fixed false errors on dimensional check operations with constraint >a < b.
- Fixed false and missing errors in SINGULAR option of RECTANGLE ENCLOSURE.
- Fixed crash on NET AREA RATIO command in certain conditions when the input to the NET AREA RATIO was a BY layer in a connect statement.
- Fixed problem in Extract to make sure that connectivity is passed down to the BY layer if present in the SCONNECT BY statements.
- In OpenAccess databases GDS Data types are now assigned from Layer-Purpose-pairs to objects when exporting data for HiPer Verify. This is done because data types are not stored on objects in OpenAccess.
- Fixed problem where the OFFGRID command was using the TDB resolution rather than the rule deck PRECISION setting.
- Fixed parsing error on Implicit layer definitions inside a dimensional check operation (INT, EXT, ENC).
- Extract no longer creates subcircuit names with spaces when appending instance Scale factor to the subciruit name.
- Extract no longer assigns duplicate instance names when Save node highlight data is checked.
- DRC Setup and Extract Setup dialogs no have independent variable “Define” lists

Tanner EDA Tools Version 16.04

What's New in S-Edit v16.04

Bug Fixes

- Property type Double and Engineering notations are now exported correctly to VHDL.
- Fixed quoting problem in expressions in Spice export.

What's New in T-Spice v16.04

Bug Fixes

- Fixed an evaluation error for source, resistor, or capacitor controlling expressions which reference user-defined .param functions defined in subcircuits.
- Fixed calculations of derivative terms for the Transit Time (TT) and Knee Current (IK and IKR) terms when certain model parameters are in effect. The incorrect derivatives may contribute to convergence problems and AC solution differences.
- Fixed a simulation crash when .ic or .nodeset statements include inductor current assignments.
- Added support for capacitor **q=***expression* parameter for setting the charge equation.
- Modified the diode BVeff calculation to ensure that BV does not go below 10*Vt, correcting reverse breakdown current calculations to match HSPICE.
- Corrected a crash in the Mextram bipolar model code due to uninitialized data.

What's New in W-Edit v16.04

Bug Fixes

- The File > Image > Copy to clipboard command now supports both WMF and PNG formats. The PNG format avoids clipping problems exhibited by WMF format when zoomed in on a trace. Other output formats are also available by executing the "chart image -format <bmp,jpg,png,wmf,emf>" command directly.

What's New in L-Edit v16.04

Bug Fixes

- Fixed crash in L-Edit if array delta is 0 and interactive DRC is enabled.
- Fixed GDS Import into OA database which was creating unresolved cells after save and reopen.
- Hide All no longer hides special layers
- Fixed L-Edit crash when saving a design after placing a via (array) and a wire.
- Improved performance importing Verilog netlist into SDL.
- Improved performance of Ripup Nets in SDL.
- Fixed crash in writing Gerber with window trace option.
- Copy cell command with hierarchy now respects the locked property of the cells in the target library. A warning is given if the cell in the target library is locked when performing a copy.
- Fixed problem where an OA database cannot be saved on a shared drive if the user doesn't have full permissions.
- L-Edit no longer crashes when renaming a cell while in Edit In-Place mode.

- Pressing "A" over text label no longer shows the Tanner Internal Label layer.
- L-Edit now ignores the DrgEnbl flag rather than interpreting it as our Lock Layer flag when reading an OA database written by Cadence, as this flag is no longer used in Virtuoso. Since L-Edit does support locked layer, we will continue to save our locked layer setting in this flag.
- Rotate command in "Command Line Editing" is no longer giving an error.
- Added the ability to print in full detail, ignoring the Hide Instances and Hide Objects settings in Setup Application when printing. Click the Options button in the Print dialog, and select the “Show maximum detail” checkbox.

What's New in HiPer Verify v16.04

Bug Fixes

- There are no fixes in HiPer Verify v16.04.

What’s new in Tanner EDA Tools for Linux v16.04

- Fixed very slow operation when using the instance dialog in S-Edit. You will need to delete the .wine-tanner folder in your home directory in order for the fix to take effect.

Tanner EDA Tools Version 16.03

What's New in S-Edit v16.03

Bug Fixes

- Hot Spot now connects to a wire when placing instances using Duplicate operation.
- In "Redirect Instances" one can now select target "Interface:" and "View name".
- SPICE Simulation Setup > NetlistOption > WrapLines is now working correctly after the number is cleared.
- Fixed pin mismatch problems on Verilog import.
- Fixed problem where Verilog Import with Preserve Text option was creating a spice view.
- Fixed problem where Spice export after a Verilog import (preserve text mode) did not export all nets.
- Fixed a crash on saving a design after Verilog import.
- The value of $Cell is not evaluated the same in S-Edit v16 as v15. $Cell is a special variable, that expands to $Model if that variable exists. This allows aliasing to happen automatically on SPICE export. This was not working correctly in v15. Customers who don't want the aliasing, should use either ${cell} or $MasterCell instead of $Cell.
- Fixed pan and zoom while moving an object.
- Fixed crash in S-Edit when ports of different names are shorted by a netlabel, and one of the ports does not exist on the symbol.
- Fixed problem in conversion of Spice view to connectivity view that would interleave local and global pins. Local pins should come first, then global pins.

What's New in T-Spice v16.03

Bug Fixes

- Made corrections to the HiSIM_HV AC analysis calculations.
- Fixed a T-Spice crash for a particular schematic/netlist when run from S-Edit.
- Diode has convergence problems when BV and IK model parameter values results in a sqrt function being called with a negative argument. This has been fixed.
- Transient analysis results are incorrect after DC OP non-convergences. The problem was with the expli-stepping algorithm not restoring the original expli value under certain circumstances. This has been fixed.

What's New in W-Edit v16.03

Bug Fixes

- Extra return line is no longer inserted between each line of data when exporting chart data to a text file.

What's New in L-Edit v16.03

Bug Fixes

- Copy over an existing cell no longer gives "False cycle in hierarchy" error.

- Fixed problem where DRC error markers would disappear when clicking in a layout view, in an OA database after importing results into the Error Navigator.
- Changing parameters of several autogen cells at the same time no longer crashes.
- T-Cell parameters are now correctly copied when copying a cell that is in a delay read state in OpenAccess.
- Japanese layer names now appear correctly in the “On Layer” field of the Edit Properties dialog.
- Draw > Clipout no longer resets T-Cell parameters.
- Problem with object snapping when using basepoint is fixed.
- Problem where drawing purpose was created as a custom purpose on Virtuoso import is fixed.
- In Edit Objects dialog, box coordinates can now be displayed as "Top left corner and dimensions", "Top right corner and dimensions" and "Bottom right corner and dimensions" along with the previously available "Bottom left corner and dimensions".
- lxMPPTemplates are now correctly imported during Virtuoso import.
- Fixed problem where port alignment was not correct in autogen cells for some values.
- LCell_GetLock no longer returns any warning, compatible with v15.
- LCell_ClearGenerateLayers no longer gives warning when there are no generated layers, compatible with v15.
- LMacro_LoadEx1200 now works correctly.
- Layer Palette is now updated after LDisplay_Refresh() command.
- Arc edge of AA polygon now arcs correctly. This was only an issue if the arc was on the first edge of the AA polygon.
- In v16.00beta some T-Cells don't work similar to v15. Note that prior to version 16.00, dlls would be reloaded every time a T-Cell was invoked, which would reset all static variables. As of version 16.00, for performance reasons, L-Edit keeps dlls loaded in the .tdb file, so you may need to initialize certain parameters inside the generator. This has been added to the documentation.
- Enhance "help" command. The Tcl "help" command searches within other Tcl commands for particular strings. You can now type "help <string>" and search for that string, or "help all" and get all help. Just like S-Edit/W-Edit.
- "Delete hierarchy" no longer deletes locked cells.
- After Virtuoso import, "Setup > Design > Valid Vias” are now initialized when using layer purpose pairs in a TDB file.
- Deselecting an instance using ALT + RMB no longer hangs L-Edit if some layers are hidden.
- On OA import, invalid layers are no longer locked.
- Tools> Jump to InstanceName in schematic" is now working correctly.
- Fixed compatibility problems in Load Calibre DRC Results Database with new Calibre results.
- Fixed problem where T-Cells instances were not rendered completely after reopening an OA database.

What's New in HiPer Verify v16.03

Bug Fixes

- HiPer Verify no longer checks for case sensitivity conflicts on L-Edit layer names when running DRC or Extract from a command file, as this check is not necessary.
- Fixed internal error when extracting a design using cells with same name from different libraries and writing output as a flat netlist.
- LVS parsing now uses .param definitions, which are defined in top level, on subcircuit instances correctly.

Tanner EDA Tools Version 16.02

What's New in S-Edit v16.02

Bug Fixes

- Fixed problem in quoting of parameter expressions in Spice Export.
- Improved performance of first design save after design is opened. Subsequent design saves after first were already faster than first save.

What's New in T-Spice v16.02

Bug Fixes

- Corrected failure when processing Verilog-A duplicate parameter settings
- Corrected “Simulation file can’t be opened for writing…” error after a simulation failure
- Corrected how sweep variables affect param settings within the subcircuit hierarchy
- Added a warning message during Monte Carlo analysis to use the “.options monteinfo=2” command to enable all outputs
- In the “T-Spice v16.0 Model Documentation” PDF file, corrected the links that open each model’s manual

What's New in W-Edit v16.02

Bug Fixes

- Move Plot has been moved from the View menu to the Chart > Plot menu.

What's New in L-Edit v16.02

Bug Fixes

- Renaming a cell from the Library Navigator no longer opens the cell.
- Ctrl+S and Ctrl+W now work when no windows are open.
- DXF Export now writes out Special Layers if they are used in the design.
- Fixed problem calculating file paths in Gerber Export.
- Leading and trailing spaces are now trimmed from cell and view names when creating a new cell or view.
- Fixed crash that sometimes occurred when opening a tdb file with layout window maximized.
- When multiple instances of a cell are present, node highlighting an object in one instance no longer highlights all.
- L-Edit now reuses T-Cell dlls after load when regenerating multiple auto-gen cells, which caused global variables defined in such dll to retain their values. Fixed LComp, which uses global variables, to re-initialize all LComp global variables, before generating a new cell. T-Cell code that use global variables should reinitialize all globals in UPI_Entry_Point.

- When layers are hidden and DRC, Extract, Node Highlighting, or Generate Layers are run, the option to “Show All Layers and Start” has been removed and replaced with option to include/not include objects on hidden layers in the operation.
- Gerber Import is now able to import multilayer Gerber with each layer in a separate file.
- Fixed validation of fracture limit in GDS Export dialog.
- Fixed a problem where polygons created by the geometry engine would not be representable in OpenAccess under certain conditions, in particular when using the Merge option in “Convert Formatted Text to Layout”.

What's New in HiPer Verify v16.02

Bug Fixes

- Fixed problem in AREA() function of DENSITY command.
- Fixed parsing of RECTANGLES command.
- Fixed parsing of SHIFT command with implicit layers and variables.
- Fixed crash and internal error problems in Extract.
- Removed SCONNECT errors from listing under “Rules with Errors” in Summary Report, as they are already listed elsewhere.
- Fixed false antenna rule violations
- Fixed problem when switching "Show DRC Results" and "Show Extract Results" in Verification Error Navigator.

What's New in S-Edit v16.01

New Features

- TCL commands "undo clear" and "redo clear" have been implemented to clear the Undo and Redo lists. TCL command “design save all” has been implemented to save a design and all it’s libraries. These command can be scripted and assigned to a button to create a “Save” button that clears the undo list.
- Generate symbol now has an option to add annotate port properties to the symbol automatically.
- A SPICE option is now available to specify the end of a subcircuit. The SPICE.ENDDEFINITION property, if it exists, will be evaluated and exported at the end of the subcircuit definition. If it does not exist, ".ends" is used to end the definition.

Bug Fixes

- Ctrl+S shortcut key now works correctly when assigned to Save all changesRedo after Undoing can now be performed up to a point before design is Saved.
- S-Edit now displays correct values of small signal parameters for diodes.
- A non-string property is no longer written out if its value is overridden as blank.
- Fixed problem where generated symbols were 10 times larger than what was specified in the Generate Symbol dialog box.
- View name is now appended to cell name when writing Spice, when there are multiple views of a cell.
- Property with empty value is no longer exported.
- Unconnected pins in Verilog are no longer shorted after importing a Verilog netlist in S-Edit.
- We now snap Cadence ports to wire-ends and pins that are within original port graphics mbb.

What's New in T-Spice v16.01

Bug Fixes

- Repaired window resizing problems when T-Spice is launched from S-Edit.
- Verilog-AMS simulation performance has been greatly improved on many computer architectures.
- T-Spice simulations are now working for file paths that include international character sets.
- Verilog-AMS simulations will use the most recent installation of Aldec Riviera Pro installed in C:\Aldec or D:\Aldec, unless the user selects an installation path with the environment variable TANNER_ALDEC_DIR or the GUI setting at Simulation settings … > Verilog-AMS > Aldec Installation.
- The .lib and .include commands now work when the filename contains a lowercase drive designator (e.g. c:).
- The delay argument for source waveform BIT patterns is now functional.
- Model bin selection in combination with the global scale option has been fixed.
- MOS model 20 is now installed. MOS model 30 is no longer supported.
- Fixed fatal error when a library section is used in a .alter block after being removed using .dellib
- Fixed fatal error when there is a trailing carriage return in a line of a PWL file.
- Fixed unhandled exception when the subcircuit definition is missing and the modelname exists with the same name.

- Verilog-AMS simulations will use the most recent installation of Aldec Riviera Pro installed in C:\Aldec or D:\Aldec, unless the user selects an installation path with the environment variable TANNER_ALDEC_DIR.
- The Aldec path has been removed from T-Spice Simulation Settings dialog.

What's New in W-Edit v16.01

Reorder Traces in Stacked Plots

- CTRL-UP and CTRL-DOWN are now used to move selected curves up or down in stacked plots. CTRL-arrow no longer moves a plot, instead SHIFT+UP and SHIFT+DOWN will move plots up or down.

Bug Fixes

- Stacked plots no longer lose stacking when there is an update during the simulation.
- Cursor table was not updated when opened after cursors are placed on chart.

What's New in L-Edit v16.01

Measure Distance Tool

- A tool has been added to measure minimum distance between two objects. Measurements can also be made between two edges and an object and an edge. For objects in the same hierarchy level, select the objects and select Tools > Measure > Between Selections. For objects in different levels of hierarchy, one can select a reference object, then a target object, using push down to select an object in a lower level of hierarchy.

Selection of Objects by Intersection

- Objects can now be selected by intersection with the selection box. An option has been added in Setup Application to control whether intersections should be selected.

Geometry Check for Short Wire Segments

- A Geometry Check has been added for wires with segments less than half wire width. These can cause self-intersections, and can be ambiguous in the manufactured result.

New UPI Functions

- LFile_Open can no longer be used to open a GDS file. A new UPI function **LFile_ImportGDSII**, is available to import a GDS file into an existing design. A new function, **LFile_ImportCIF**, is available to import CIF into an existing design.

Bug Fixes

- Fixed problem where ports or labels in a tdb library could move to a different layer when the layer list of the library does not match the layer list of the toplevel design.

Selection/Deselection

- Edge deselection by mouse in Partly Enclosed mode, now deselects edges even when vertex is included.
- Fixed problem where deselect by mouse (Alt+ Right mouse click) did not work in some cases.

- Fixed problem where extended selection did not always work in some cases.
- Fixed problem in implicit edge selection. Also fixed when in Edit-In-Place.
- Undo of object stretch now keeps selected edges.
- Edges of polygons can now be selected when Selection Range is 0.
- Edit Range value now works correctly for polygons and wires.
- Fixed problem in selection after deletion while in Edit-In-Place.
- Selecting two adjacent edges then invoking Edit Object will select the vertex between the two edges in the Edit Object Dialog. This makes it very easy to select then delete a vertex.

Edit/Move

- Editing a 45 degree polygon or wire will no longer turn the object into an AA polygon or wire.
- Editing a vertical or horizontal edge of an all angle wire will no longer turn it all angle.
- Moving an edge and curved edges now preserves curve heights and moves the edge at the correct amount.
- Perpendicular Edge Move now works when the polygon includes a curved edge.
- Fixed a problem where wire got shorter instead of longer when editing.
- Fixed a problem where editing the second from end segment of an AA wire did not preserve location of endpoint vertex.
- Fixed a problem when editing an all angle edge passed through 45 degree angle.
- Rotating the polygon by 90 degree using Ctrl+R no longer results in off grid errors. We now snap to the manufacturing grid after any rotation.
- Fixed problems where the drawn vertex when drawing a polygon or wire would in some circumstances not be exactly on the snap point.

Misc

- Fixed problem where Delete Hierarchy deleted only first level of hierarchy and the cell itself.
- DXF Import now imports into the open toplevel design. It no longer creates a new design.
- Fixed problem where DXF import created a cell with blank cell name.
- DXF import now handles interpolated b-spline vertices.
- SDL Verilog import no longer splits out external connections into two nets.
- A reservation is now obtained for a cell before allowing it’s T-Cell code to be edited.
- Changing a layer in "New Port" dialog when port is first created now works.
- Fixed problems editing objects in a port.
- Fixed Persistent ruler not working work properly when set to “current layer”.
- Fixed a problem replacing overridden parameters when replacing multiple T-Cell instances. Parameter overrides are now preserved. Also fixed program freeze when replacing multiple T-Cell instances.
- Fixed crash on Cell > Flatten operation.

What's New in HiPer Verify v16.01

Bug Fixes

- Fixed a problem where DRC would hang inside the rule optimizer.
- // Characters are no longer treated as start of single line comment when inside double quotes.
- Fixed crashes while running DRC.

What's New in HiPer PX v16.01

- Fixed problem where HiPer PX aborts due to 45 degree objects in the layout.

Tanner EDA Tools Version 16.00

What's New in S-Edit v16.00

Verilog and Verilog-AMS Views

- Two new view types, Verilog and Verilog-AMS, are now available in S-Edit, in support of Verilog-AMS simulation. Verilog type views are intended for digital RTL or structural Verilog (netlists), whereas Verilog-AMS type views are intended for code that mixes Verilog-A and Verilog-D constructs in the same cell.

Improved Design Checks

- Design check now check for consistency of pins between the symbol view and schematic, spice, and Verilog views.

Miscellaneous Improvements

- A command, **View > Hide Docked Views**, has been added, which toggles hiding and showing of docked views. This command is made even more convenient when bound to a hot key.The library name is now printed in File > Hierarchy Report.
- Fixed problem of not highlighting some wire segments in Highlight Net.
- A warning is now issued when adding a library that is already part of the design.

Bug Fixes

- Fixes in Hierarchy Priority have been made in netlist export and Design checks. Design checks now respect Hierarchy Priority settings.
- Subcircuits in schematic view are no longer written to netlist when the Hierarchy Priority is set to veriloga.
- Verilog export is now able to export parameters.
- Veriloga views may now be created from symbol views.
- Symbol generation from Verilog views now creates ports for arrays with the correct array order.
- Libraries are no longer modified when a cell view is deleted from top level design.
- Copying a Spice or Verilog cell or view now renames the subcircuit/module name in the text to the new name.
- Problem in EDIF import which misplaced net labels resulting in dangling wires in certain circumstances is fixed.
- Verilog export now exports parameters in modules and instances.
- Various Spice import bugs have been fixed.
- Replace has been added to the Edit menu for text views.
- Erroneous "Window to activate not found" messages have been fixed.
- S-Edit no longer saves references to deleted cells, which would produce “missing cell” warnings when the design was subsequently opened.
- Fixed crash in S-Edit when annotating dc operating points.
- Text in Additional SPICE Commands is now exported to netlist correctly.
- S-Edit no long removes '@' character from instance names when importing Spice netlist.

Upgrade Notes

- The backslash character is now uniformly treated as an escape character, including when used inside a quoted string. In v15 a backslash inside a quoted string was not

treated as an escape character. Path separators should be written using either double-backslash or single forward slash.

What's New in T-Spice v16.00

Mixed Signal Simulation

- Verilog-AMS mixed signal simulation is now available, using T-Spice for the analog simulation and either Aldec Riviera Pro™ or Mentor® ModelSim® for the digital simulation.

Models

- New transistor models HiSIM2 and HiSIM_HV are now available.
- All Berkeley BSIM models and Philips models have been updated to the latest release.

Miscellaneous Improvements

- Added support for diode tunnel saturation current equations.
- T-Spice can be configured to play a sound or send an e-mail when simulations complete.
- Added device instance parameters delvto and mulu0 for BSIM3 and BSIM4 MOSFETs.
- Implemented plotting of numerous internal state variables for NXP/Philips models (MOS 9, PSP, Mestram, Juncap, etc.) The complete list is available through the T-Spice UI menu selection: Help > Models Supported by T-Spice…
- The ability to queue multiple simulation jobs in one operation is now available from the T-Spice GUI **Simulation > Batch Simulations…** menu.
- Input file parser does not stop after the first syntax error, but will continue until **.options maxsyntaxerror=n** (default n=5) errors have been encountered or all input files have been read.

Bug Fixes

- Verilog-AMS input files cannot have a full pathname which is longer than 132 characters, and T-Spice will now issue an error message if this limit is exceeded.
- Corrected the .**hdl** command behavior to search for input Verilog-AMS files relative to the current input file directory, followed by the main netlist directory, and then the **vasearch** and **search** option paths.
- The performance for reading very large input files and model libraries has been improved.
- A warning message will be issued, and the command ignored, when the **.global** is located within a .subckt declaration. The global command is only valid at the top level of the circuit hierarchy.
- Corrected an error when a Verilog-A module is referenced in a **.model** statement which is located within a **.subckt**.
- Corrected an erroneous “Unsupported model level 69” error when the PSP swgeo model parameter was assigned.
- Corrected the the .assert options start and stop which were not working.
- Fixed a crash when transient analysis was combined with outer sweeps and expression plotting.
- Expressions in the input file that are enclosed in parentheses, e.g. (cscaled * 5), are allowed and are treated the same as quoted expressions.
- Improved the convergence of circuits containing BJTs.

Upgrade Notes

- Support for External C Models has been discontinued. Users should transition to using Verilog-A models which have significantly greater capability, are an industry standard, and are portable across simulators.

What's New in W-Edit v16.00

Parametric and Scatter Plots

- A new chart type, **Parametric,** is available. A parametric plot allows one to plot one trace vs another using one trace as the x-axis. A **Scatterplot** may be created from a Parametric plot, which plots the datapoints without connecting them with a line.

Cursor Table

- A new cursor table in W-Edit, in a separate window from the plot, displays detailed information about traces on the plot at the crossing of a single cursor, or between two cursors. Information such as first and second derivative, min, max, average, peak-to-peak, RMS, number of samples, or a user defined expression, can be displayed in the table.
- Horizontal as well as vertical cursors are displayed in the cursor table.
- A new command, Edit > Select > Cursors. This can be used to easily select all toolbars and then delete them.

Stackable Plots

- Transient plots may now be displayed in a stacked format, where the min to max height of each curve is scaled to equal height, and the curves are then offset on the y axis one above the other. Right click on a plot and invoke **Plot Properties**, then set Type to **Stacked**.

Histograms

- Histograms are now filled.
- A Histogram can now be made for any trace.

Resizable and Movable plots and curves

- Plots are now resizable. To resize a plot, place the mouse over the x-axis of a plot and drag up to make the plot smaller, and down to make the plot larger. Plots below the one being resized will automatically resize proportionally to the chart size remains unchanged.
- Plots that contain selected curves can now be moved up/down using CTRL-up and CTRL-down arrow.
- Curves can now be Drag-and-dropped from one plot to another. The drag must be started on the legend.
- Curves may also be cut/copy/paste using the context sensitive menu.

Text Size and Font Control

- The size of all text elements on a plot are now individually controllable. Right Click on a plot and select **Chart Text**.

Legend Position

- The legend can now be placed above, below, left or right of the plot.

Axis Control

- Axis titles can now be user controlled.
- Axis can now be displayed in various user selected engineering units.
- The number of significant digits on X/Y-axis is now automatically adjusted as needed to provide sufficient resolution.

Miscellaneous Improvements

- A command, **View > Hide Docked Views**, has been added, which toggles hiding and showing of docked views. This command is made even more convenient when bound to a hot key.
- Markers can now be snapped to traces. This is done by having a single selected trace when the marker is created. Markers can be used in the cursor table or in measurements, as a substitute for a cursor. A new command “Draw Labeled Marker” places a marker and a label, with the label set to display the X and Y values at the position of the marker.
-
- Missing or invalid data points in a trace, for example due to convergence problems in a sweep, are marked by a triangle with an exclamation point inside.
- The line style and color of selected cursors, markers and text can now be set by the user. Choose **Setup > Selection Styles**.
- A duplicate of a chart may now be made using the Chart > Duplicate Chart command.
- New measure commands have been added for measuring gain margin and phase margin.
- A new parameter "- versus" has been added to the Measures... commands in the waveform calculator. When a simulation contains sweeps over one or more variables, the “versus” parameter is used to select one of these as the independent variable against which the measurement is taken. This can be used to create a new trace, for plotting a measured result against a sweep parameter.

Bug Fixes

- Fixed problems where expand and collapse traces would not work correctly.
- Plot Properties View Port settings for Min and Max are now respected.
- File > Export Chart Data now works for a AC simulation.
- Copy to clipboard now works on multiple traces
- Fixed problem where a Transient chart would sometimes open after a dc analysis.
- Charts now obey the "Show cursor tables in charts" default option.
- Trace color set from Trace navigator is now correctly used when trace is added to charts.
- Fixed crash in W-Edit when performing “Hide all but selected Simulations".

Upgrade Notes

- 'DC/Parametric' plot in v15 is now called 'X-Y'.
- Tanner Tools v16 uses Tcl 8.5.10

What's New in L-Edit Pro v16.00

OpenAccess

- L-Edit v16 supports OpenAccess databases, as well as Tanner’s TDB format. OpenAccess is the preferred choice for users wanting multi-user support or the ability to use foundry PDKs in OpenAccess format. TDB is the preferred choice for projects

with a single user and no needs for OA compatibility. OpenAccess databases have the ability to save data on a per cell basis, and thus offer fast save ability on large databases. TDB however is a more compact database, and is faster for full database read and write.

MultiUser

- Designs in OpenAccess will support multiple users accessing and modifying the same design at the same time. When you start to edit a cell, that cell will become reserved to prevent changes by other users. When you are done making changes, you save your changes to the database and release the reservation for the cell. To obtain the latest updates made by other users, there are Update cell and Update All commands. If you attempt to obtain a reservation on a cell that is already reserved, L-Edit can tell you who has the reservation. A new **Database** toolbar has buttons to **Toggle reserve of cell view file on disk…**, **Save Cell…**, **Save all cells…**, **Update cell…**, and **Update all…** buttons.

Improved Technology Control

- L-Edit has improved capability for CAD manager control of technology. OpenAccess databases can use the Attach or Reference mechanism to link to an external technology library which can be under the control of a CAD manager. OpenAccess or TDB designs can link to a Virtuoso technology file or another TDB file for technology management.
- L-Edit is able to export a Virtuoso Technology and Display file. Invoke **Setup > Export Technology.**

Improved Library Support and Cell Navigator

- L-Edit offers improved support for libraries, and a new cell navigator for easy navigation of cells and libraries. Similar to the S-Edit library navigator in appearance, many operations may be invoked directly from the new navigator, including many operations that can be executed on multiple cells simultaneously.
- The library Navigator is able to show modified cells, reserved cells and various other conditions by color. Use Right Click on the cell list, then choose Appearance > Color.

Layer-Purpose Pairs

- L-Edit now supports layer-purpose pairs. The **Setup Layers** dialog now contains the ability to create new purposes, and to set the purpose for a layer. Layer-purpose pairs may also be imported from various sources using **Setup > Technology**.
- Layer-Purpose pairs now have a “Valid” setting, visible on the **Setup Layers** dialog. This setting controls whether the layer is included in the layer palette; Valid layers are included, Invalid layers are excluded. When the layer palette is set to show all layers however, then both Valid and Invalid layers are included.

Vias

- Two new types of vias have been added to L-Edit, corresponding to Standard Vias and Custom Vias in OpenAccess. Standard Vias are defined based on a template of parameters, such as upper, lower, and cut layer, surround distances, number of rows and columns, etc. Custom Vias are defined as a reference to a cell, which could be either a plain cell with layout, or a generator cell.
- Vias may be designated as Valid for a particular technology. The list of valid vias is shown in Setup > Design > Valid Vias.
- A new command, Draw > Vias > Place Vias, with a button on the Drawing toolbar, provides an easy way to place vias. A dialog is presented with a name filter and a filter for selecting the Lower and Upper layers.

- Vias may be defined in a library for use in the main design. Vias from a library can be added to the list of valid vias and used in automatic via placement using the [and] keys.

Ports and Text Labels

- L-Edit now provides separate Text Label and Port objects. Previous versions of L-Edit provided a single object that served as both text labels and ports. Ports can now consist of box or polygon shapes, and a port may contain multiple shapes.

Replace Instances

- New Replace Instances operations have been implemented. Right click on a cell in the Cell Navigator and invoke **Replace Instances > Of This Cell…** or **Replace Instances > In Selected Cells…**.
- **Replace Instances > Of This Cell…** replaces instances of the selected with instances of a new cell, within a specified scope. The specified scope is either the active cell, the active cell and hierarchy, the library corresponding to the active cell, or all libraries. **Replace Instances > In Selected Cells…** replaces instances of one chosen cell with instances of another chosen cell, within the list of cells that are selected in the cell navigator. **Replace Instances** can also be invoked from the **Cell** menu.
- When performing Replace Instances, non-default parameter values on T-Cells will be transferred to the new instance, for those parameters that are in common between the old and the new cell.
- Replace Instances no longer requires confirmation for each cell when using the Abutment option.

Copy Cell

- A new Copy Cell command allows copying a cell from one library to another, with options to copy hierarchy, retarget instances of the old cell to the new cell, and delete originals.

Multi-Cell Operations

- Multi-Cell Operations now offer a unified selection of the scope on which to operate. The scope may be chosen from i) Selected objects, ii) Cell, iii) Cell and Hierarchy, iv) Library, v) All Libraries, as appropriate for the particular operation. The Multi-Cell operations include **Change Layers, Fracture Polygons, Snap to Manufacturing Grid**, **Clear Persistent Rulers**, **Assign GDSII Data Types**, **Replace Instances**, **Clear Generated Layers**, **Clear Error Layer.**
- Setup > Merge Layers has moved to Draw > Convert > Change layers.

Edit Objects

- The Edit Objects dialog now has a new **Via** tab for editing parameters of Standard Vias.

Mask Import/Export

- GDS Import now imports into and existing database. In cases of collisions with existing cells, the user is given a choice to override or not override cells in the database.
- GDS export now has 6 choices for the scope of cells to export, i) All cells, ii) Active cell, iii) Fabrication cell, iv) Selected cell, v) All cells from selected library, and vi) Cells selected in navigator. For any scope of selected cells, the hierarchy of cells can

be included or excluded for export, and also cells from selected libraries can be excluded for export.
- GDS Export now supports a layer map file for mapping of layer names to GDS numbers, instead of using mapping from Setup > Layers.
- Text in GDS files is now imported as labels rather than ports.
- GDS Export now writes the instance name using GDS property number 6.
- A GDS Export UPI function, LFile_ExportGDSII, is now able to set options and perform GDS export.
- The XRefLib name (now library name) is no longer appended to the cell name on GDS export.

Dockable Views and UI Improvements

- The Layer Palette, Libraries Navigator, Verification Navigator, SDL Navigator, Command Line, Aerial View, and Port tool are now dockable views. All dockable views can now be resized without undocking.
- A command, **View > Docking Views > Hide Docked Views**, has been added, which toggles hiding and showing of docked views. This command is made even more convenient when bound to a hot key.
- The command window is now used for logging of information, warning and error messages. It is recommended to have the command window open when working with OpenAccess designs, as many OpenAccess related messages are logged to this window.
- Layer pickers in dialogs now have enhanced capabilities to sort and filter the layer list.

SPR

- SPR will now reference cells from a standard cell library, rather than copying them into the main design.

Miscellaneous Improvements

- Speed of rendering “Highlight Layout” in SDL is significantly improved.
- The Generate Layers dialog now has a layer name filter.
- Layout Versus Layout (LVL) now supports OA databases. Comparisons can be done between TDB and TDB, OA and OA, and OA and TDB.
- The Design Navigator now displays cells grouped by library. Cells in libraries can be expanded to show their contents. Autogen cells are now in a group under their master.

Converting TDB to OA

- To convert a TDB database to OpenAccess, choose **File > Save Copy > OpenAccess Database…**. The save TDB to OpenAccess dialog offers four options for saving technology, i) Local (use technology from the tdb file and save locally in the newly created OA library) ii) Attach to an external OA library iii) Reference an external OA library, and iv) copy technology from an external OA library.

Bug Fixes

- Errors in T-Cell generation no longer present a message dialog for all autogens of the same T-Cell.
- T-Cell Generator cells are no longer written when exporting to GDS. These cells are always empty, as the actual geometry is contained in the autogen cells.
- DRC and layer generation now gives correct results when the layer name is a number.

- Double clicking on a TDB file now reliably opens the file correctly, and no longer gives an error message.
- Fixed problem where object snapping on large layout would cause to L-Edit to hang.
- When moving objects, Object Snapping no longer snaps to points in the selection.
- Fixed problem where Interactive DRC would become very slow with Shift-Move.
- Via cycle using the ‘ key now cycles correctly though vias for the current drawing layer.
- When drawing a wire, pressing the] key, will place a via and start another wire on the next layer up. When not drawing a wire, pressing the [or] key will now place a via and start drawing a wire.
- Replace Object With Guard Ring and Draw Guard Ring Around Selection now work correctly on wires.
- Fixes crashes on undo after various Draw > Wire Utilities operations.
- Fixed crashes on undo after Alignment operations.
- Fixed crashes on undo after Fillet/Chamfer operations.
- Zero width wires no longer give an “Unrecoverable error” message when performing a Fillet operation. They are ignored in Fillet operations.
- Fixed problem where Text Layout Generator would place the previous text string.
- Fixed problem where L-Edit would not retain the definition for some derived layers.
- Fixed problem where one cannot change the default options for Gate inter-connection and Bulk contact arrangement in HiPer DevGen MOSFET setup
- In SDL, Diode pin names are now DP and DM, not DP and DN.
- L-Edit no longer gives "invalid conversion from 'int' to 'LWireConfigBits'" error for T-Cell code generated by T-Cell builder.

Upgrade Notes

File Compatibility

- Files saved by L-Edit v16 cannot be read into previous versions of L-Edit. It is recommended that you create a backup of your v15 or earlier database before saving in v16. L-Edit will automatically create a backup of a pre-v16 database when saving in v16.

UPI

- The UPI function LCell_GetName has been deprecated. One of the following functions should now be used: LCell_GetFullName, LCell_GetCellName, LCell_GetViewName, LCell_GetLibName, LCell_GetPresentationName, LCell_GetCanonicalName.
- There are two new object types in L-Edit v16, Labels and Electrical Ports. UPI macros and T-Cells will need to be updated to process these objects.

Designs with Xref files

- In L-Edit v15 and prior, designs that used libraries would save a local copy of cells from libraries in the main design. When the library was missing, the main design could still render the layout completely, by using the local copy of the missing library’s cells. L-Edit v16 no longer uses a local copy, so if a library is missing, cells from that library are displayed with an X, indicating they are unresolved. If you have a v15 file that uses libraries, you should have those libraries when opening the design in v16. If the libraries are missing, you can open the design in v15 and use Cell > Examine Xref Cells… to unlink cells from libraries and then they will open in v16.

Converting TDB to OpenAccess

- OpenAccess does not support object data types. When saving a TDB file to OpenAccess, object data types will be discarded. A warning will be issued when object data types differ from layer data types.

- All instances must be named in OpenAccess. When saving a TDB file to OpenAccess, unnamed instances will be automatically assigned instance names.

Copy Across

- Copying cells across TDB files is no longer allowed, except in the case of copying from a library to the toplevel design.

Save as L-Edit v15.x Tanner File, or other previous versions

- L-Edit v16 has changed the way libraries are saved, and new features such as Standard Vias, Custom Vias, layer purpose pairs, electrical ports, and text labels have been introduced. Save as v15.x or previous version will preserve mask layout, but some conversion in the way features are represented may take place due to different representations in the two versions. Conversion may also occur when opening a v15 tdb file in L-Edit v16 and saving as v15.x, as round trip conversion of all features is not always possible. Save As v15.x should be used as a one way path to get data back into a previous version of L-Edit, but should not be used in a round trip workflow involving a mixture of L-Edit v15 and L-Edit v16.

Conversion of vias in v15 to v16

When opening a v15 tdb file in v16, viadefs are created in the following situations:

- “Contact” cells are converted to stdvia viadefs if the contact cell contains only a Via Layer, Lower Layer, Upper Layer, and up to two Other Layers, and none of the layers are fracturable. If the contact cell is the Setup > Design > Vias list, then the stdvia viadef is placed in the Setup > Design > Valid Vias list.
- Customvia viadefs are created for cells in the Setup > Design > Vias list that are not identifiable as stdvias, and then the customvia viadef is placed into the ValidVias list.
- Customvia viadefs are created for “contact” cells whose parameters do not match geometry (ie. geometry was manually edited after creation) and are in the Setup > Design > Vias list. The customvia viadef is then placed into the ValidVias list.

What's New in HiPer Verify v16.00

Miscellaneous Improvements

Command Editor

- A command **Find Rule By Name** has been added to the context menu of the DRC rule command file editor. This command finds the entered DRC rule anywhere within the tree of command files of the active file, even if the rule is in another file. The command searches within the set of active DEFINEs so that if a rule is defined multiple times within different DEFINE blocks, the correct appearance will be found.

Calibre Commands

- HiPer Verify has improved performance in Boolean, Coincident Edge, Rectangle Enclosure, and Net Area Ratio operations.
- The Or Edge command has been implemented.
- The Endpoint option of Touch Edge has been implemented.
- The SEQUENTIAL option is now supported in the GROW command.

Dracula Commands

- Support "PARAM RES" and "PARAM CAP" in Dracula deck

Bug Fixes

Calibre Commands

- Fixed problem in SIZE operation with INSIDE OF option.
- Fixed crash in SIZE operation.
- Missing and false errors in RECTANGLE ENCLOSURE are fixed.
- Errors and crash in Boolean operations are fixed.
- Errors in TOUCH EDGE and COIN EDGE are fixed.
- HiPer now finds a violation of ENCLOSURE rule that was previously missed.
- Fixed false errors in ENCLOSURE command.
- Fixed problem computing edge layer results in INT operation.
- Fixed error in ENCLOSE RECTANGLE operation.
- Fixed several false errors on hierarchical layout, where flat layout shows no errors.
- Fixed crash in DRC when array exceeded a certain size.
- The SVRF MESSAGE command is now supported. The message is written to the summary report.

Dracula Commands

- Fixed EXT command when two layers are the same. Treat as single layer operation.

Standard DRC

- Fixed problem in Standard DRC where layer name is a number.

Command File Parser/Optimizer

- HiPer syntax check now gives an error when two rules with the same name are found, rather than a warning.
- Fixed problems where Generate Layers would report that syntax errors are found, but then no syntax errors would be reported on F6 syntax check.
- Fixed problem in command file parser caused by double quotes around a variable name in an expression.
- Fixed false connectivity error in rule deck reported by parser.
- Fixed problem in Optimizer removing a lyer too soon.

LVS

- Problem in LVS caused by blank line in Spice model file has been fixed.
- LVS now correctly handles filenames without extension.
- Fixes and improvements are made to handling of options when running LVS from the command line. LVS no longer crashes if options not passed correctly.

Additional Information

Supported System Requirements

Microsoft® Windows Windows 7, Windows 8, and Windows 8.1.
Red Hat® Linux 5 or Red Hat® Linux 6.
Intel® Pentium® 4 processor or Pentium 4 equivalent with SSE support
1 GB RAM
425 MB of available disk space with an additional 100 MB during installation
A video card with at least 64 MB of memory
3 button mouse

Recommended System Requirements

Microsoft® Windows 7 64-bit
Dual Core Intel® Xeon® 2.66 GHz or better processor for desktops
Intel® Core™ 2 Duo 2.00 GHz or better processor for laptops
It is recommended to get a computer with at least 2 cores and the fastest processor speed you can afford. Tanner Tools can take advantage of 2 cores/processors but not more. It is also recommended to get the fastest RAM you can afford.
4 GB RAM (more memory recommended if you use HiPer Verify)
1 GB of available disk space with an additional 100 MB during installation
A video card with at least 256 MB of dedicated memory
Microsoft® Intellimouse
1280 x1024 Resolution - True Color (24-bit)

Installation

Install Tanner EDA Tools from the Windows operating system. To begin, insert the distribution CD into your CD-ROM drive. The setup program should start automatically; if it does not, then you should navigate to the main CD directory from a file browser window, and double click SETUP.EXE to run setup. The Tanner EDA Tools setup program will provide information on how to proceed.

Administrator Privileges are required to install Tanner EDA Tools v16. Power users are not able to install Tanner EDA Tools. On some Windows Vista machines, the following error will appear when installing, even if you are logged in as an administrator: “Error 1925. You do not have sufficient privileges to complete this installation for all users of the machine. Log on as an administrator and then retry this installation.” If this occurs, the right-click on setup.exe on the installation CD and select option Run As Administrator. This will bring you Tanner EDA Tools Setup window and the installation will proceed.

Starting Tanner EDA programs from the Windows Start menu, when logged in as a different user than the user who performed the installation, will sometimes result in a message from Windows requesting insertion of the installation CD. Inserting the CD and following the instructions will complete the installation for this user, and the message will not appear again. If you install just T-Spice and want to run Verilog-A, you must also install Minimalist GNU for Windows using Custom Installation.

Uninstallation

If the oaFSLockD.exe process used for OpenAccess database locking is running, the software will not be able to uninstall properly. You can use Windows Task Manager to kill oaFSLockD.exe manually before uninstalling the software, or if an error is encountered while uninstalling.

OpenAccess

Every machine using OpenAccess should have port number 16725 open. When L-Edit starts it launches a lock daemon, oafslockd.exe, which opens a TCP port to listen on. The port number is 16725. On modern versions of Windows, the first time a new version of L-Edit starts (really a new version of oafslockd.exe), the operating system will present a dialog asking if you want to open this port. If you answer "No", then the port is blocked and other machines that try to connect to this machine will incur a 30 second timeout. Not all versions of Windows and Linux will present a dialog asking to open port 16725, in which case you may have to open the port manually.

Licensing

Tanner EDA Tools is licensed software; to use the program, you must have a license from Mentor Graphics. Tanner EDA Tools will verify the license either from License Server, installed on your company network, or from a hardware lock attached to your computer's parallel port. Tanner EDA Tools is available in node- or network-locked licensing.

This version of Tanner EDA Tools uses the SentinelLM version 7.3.0.6 License Server.

When installing a .tlu license file, the Tanner Tools license installer will remove expired licenses from the lservrc file.

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