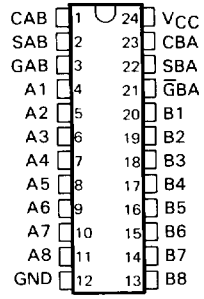
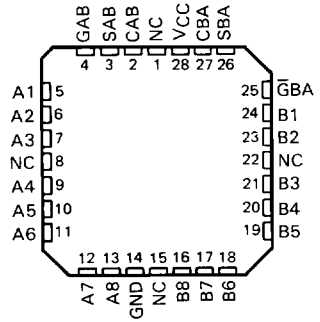
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs to A Bus**
- **Included Among the Package Options Are Compact 24-Pin 300-mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS651, 'AS651	3-State	3-State	Inverting
'ALS652, 'AS652	3-State	3-State	True
'ALS653	Open-Collector	3-State	Inverting
'ALS654	Open-Collector	3-State	True

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . NT PACKAGE
(TOP VIEW)



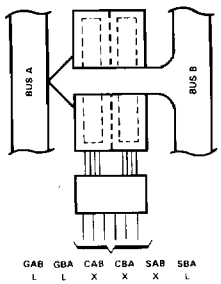
SN54ALS', SN54AS' . . . FC PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



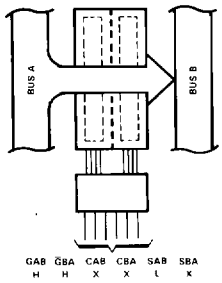
NC – No internal connection

description

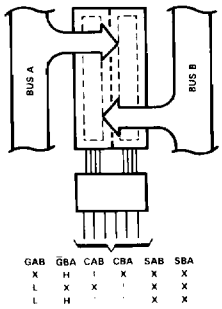
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{\text{G}}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.



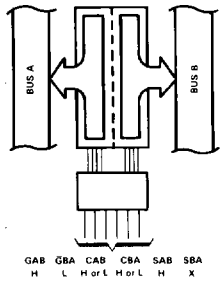
REAL-TIME TRANSFER BUS B TO BUS A



REAL-TIME TRANSFER BUS A TO BUS B



STORAGE FROM A AND/OR B



TRANSFER STORED DATA TO A AND/OR B

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Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The -1 versions of the SN74ALS651 through SN74ALS654 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS651 through SN54ALS654.

The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

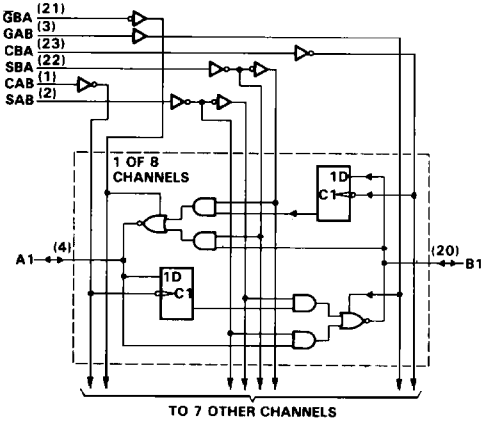
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS651, 'ALS653 'AS651	'ALS652, 'ALS654 'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H		H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

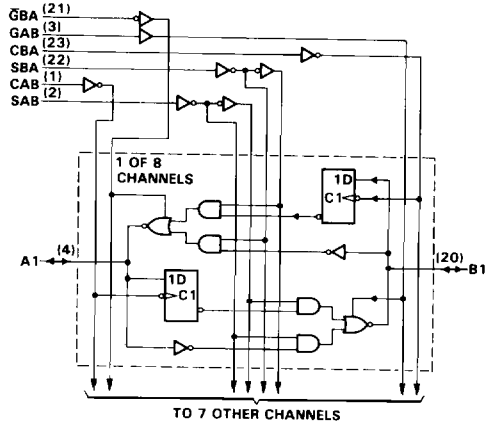
*The data output functions may be enabled or disabled by various signals at the GAB and $\overline{G}$BA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic diagrams (positive logic)

'ALS651, 'AS651, 'ALS653



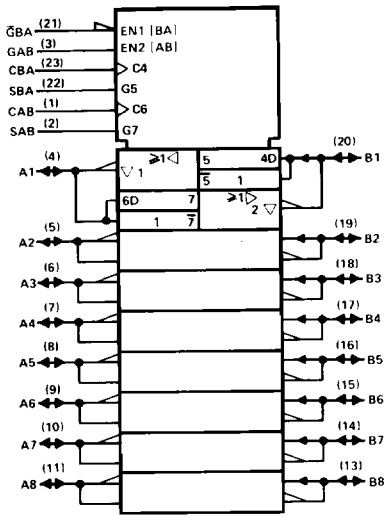
'ALS652, 'AS652, 'ALS654



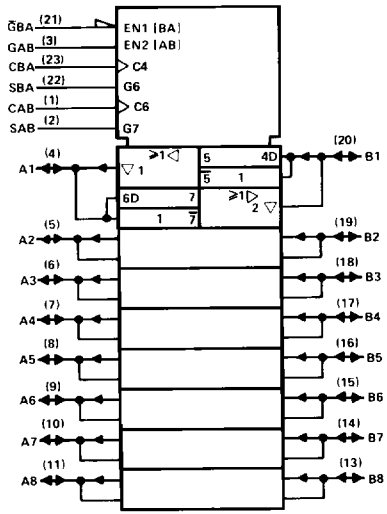
Pin numbers shown are for JT and NT packages.

logic symbols

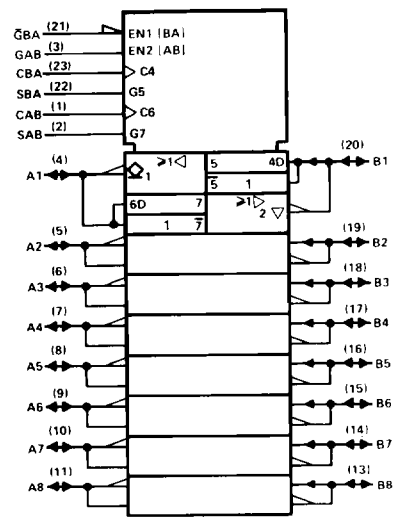
'ALS651, 'AS651



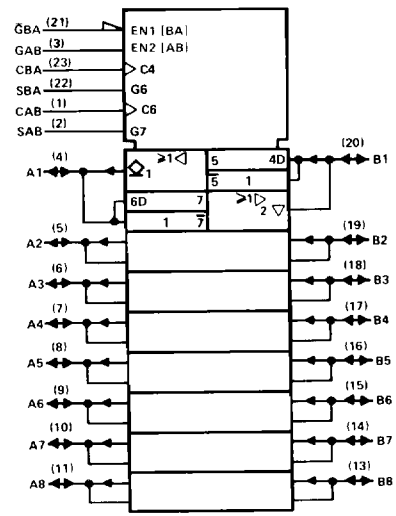
'ALS652, 'AS652



'ALS653



'ALS654



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS651, SN54ALS652 . . . . . −55 °C to 125 °C
SN74ALS651, SN74ALS652 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CBA or CAB high							ns
		CBA or CAB low							
t_{su}	Setup time before CAB↑ or CBA↑	A or B							ns
t_h	Hold time after CAB↑ or CBA↑	A or B							ns
T_A	Operating free-air temperature		−55		125	0		70	°C

† The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS651-1 and SN74ALS652-1 only.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS651	V_{CC} = 5.5 V	Outputs high		52			52		mA
			Outputs low		57			57		
			Outputs disabled		58			58		
	'ALS652		Outputs high		60			60		
			Outputs low		68			68		
			Outputs disabled		68			68		

‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS651			SN74ALS651			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		10			10		ns
t_{PHL}				12			12		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				15			15		
t_{PZH}	$\overline{G}$BA	A		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$BA	A		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

'ALS652 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS652			SN74ALS652			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		8			8		ns
t_{PHL}				8			8		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				12			12		
t_{PZH}	$\overline{G}$BA	A		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$BA	A		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and A I/O ports . . . . . 7 V
B I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS653, SN54ALS654 . . . . . −55 °C to 125 °C
SN74ALS653, SN74ALS654 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CBA or CAB high							ns
		CBA or CAB low							
t_{su}	Setup time before CAB↑ or CBA↑	A or B							ns
t_h	Hold time after CAB↑ or CBA↑	A or B							ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS653-1 and SN74ALS654-1 only.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.75 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_O¶	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS653	V_{CC} = 5.5 V	Outputs high		52			52		mA
			Outputs low		57			57		
			Outputs disabled		58			58		
	'ALS654		Outputs high		60			60		
			Outputs low		68			68		
			Outputs disabled		68			68		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS653 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, (A outputs) R1 = R2 = 500 Ω, (B outputs) T_A = MIN to MAX						UNIT
			SN54ALS653			SN74ALS653			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA	A		24			24		ns
t_{PHL}				15			15		
t_{PLH}	CAB	B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A	B		10			10		ns
t_{PHL}				12			12		
t_{PLH}	B	A		24			24		ns
t_{PHL}				10			10		
t_{PLH}	SBA‡ (with B high)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SBA‡ (with B low)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SAB‡ (with A high)	B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SAB‡ (with A low)	B		15			15		ns
t_{PHL}				15			15		
t_{PLH}	$\overline{G}$BA	A		24			24		ns
t_{PHL}				17			17		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

'ALS654 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, (A outputs) R1 = R2 = 500 Ω, (B outputs) T_A = MIN to MAX						UNIT
			SN54ALS654			SN74ALS654			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA	A			24			24	ns
t_{PHL}					15			15	
t_{PLH}	CAB	B			11			11	ns
t_{PHL}					13			13	
t_{PLH}	A	B			8			8	ns
t_{PHL}					8			8	
t_{PLH}	B	A			24			24	ns
t_{PHL}					10			10	
t_{PLH}	SBA‡ (with B high)	A			26			26	ns
t_{PHL}					15			15	
t_{PLH}	SBA‡ (with B low)	A			26			26	ns
t_{PHL}					15			15	
t_{PLH}	SAB‡ (with A high)	B			16			16	ns
t_{PHL}					16			16	
t_{PLH}	SAB‡ (with A low)	B			15			15	ns
t_{PHL}					12			12	
t_{PLH}	$\overline{G}$BA	A			24			24	ns
t_{PHL}					17			17	
t_{PZH}	GAB	B			19			19	ns
t_{PZL}					22			22	
t_{PHZ}	GAB	B			12			12	ns
t_{PLZ}					14			14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS651, SN54AS652 . . . . . −55 °C to 125 °C
SN74AS651, SN74AS652 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				48			64	mA
f_{clock}			0		75	0		90	MHz
t_w	Pulse duration	CBA or CAB high	6			5			ns
		CBA or CAB low	7			6			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	7			6			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.5			−0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS651	V_{CC} = 5.5 V	Outputs high		110	185		110	185	mA
			Outputs low		120	195		120	195	
			Outputs disabled		130	195		130	195	
	'AS652		Outputs high		120	195		120	195	
			Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS651		SN74AS651		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SABt	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

2 ALS AND AS CIRCUITS

'AS652 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS652		SN74AS652		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SABt	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PHL}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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