PAL20X10A Series

20L10A, 20X10A 20X8A, 20X4A

Features/Benefits

- XOR gates on registered outputs
- Efficient implementation of counters
- Register preload
- Power-up reset
- Security fuse

Ordering Information

PAL20X10A C NS STD

- PROGRAMMABLE ARRAY LOGIC
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  - X = XOR Registered
  - L = Combinatorial Active Low
- NUMBER OF OUTPUTS
- HIGH SPEED
- OPERATING CONDITIONS
  - C = Commercial
- PACKAGE
  - NS = Plastic SKINNYDIP
  - JS = Ceramic SKINNYDIP
  - NL = Plastic Leaded Chip Carrier
  - SG = Small-Outline Gull-wing
- PROCESSING
  - STD = Standard
  - XXXX = Other

PAL20X10A Series

	ARRAY INPUTS	OUTPUTS		t_{PD}* (ns)	I_{CC} (mA)
		COMBINATORIAL	REGISTERED		
PAL20L10A	20	10	0	30	165
PAL20X10A	20	0	10	30	180
PAL20X8A	20	2	8	30	180
PAL20X4A	20	6	4	30	180

Description

The PAL20X10A Series offers Exclusive-OR (XOR) gates preceding each register. The XOR gate has as its inputs two sums, each of two product terms. The XOR gate is very efficient for counting applications.

The PAL device transfer function is the familiar Boolean sum of products. The PAL device consists of a programmable AND array driving a fixed OR array. Product terms with all bits programmed (disconnected) assume the logical high state, and product terms with both true and complement of any signal connected assume the logical low state.

Variable Input/Output Pin Ratio

The register devices have ten dedicated input lines, and each combinatorial output is an I/O pin. The combinatorial device has twelve dedicated input lines, and only eight of the ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied directly to VCC or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with programmable three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any combination of device inputs or output feedback. The output provides a bidirectional I/O pin in the combinatorial configuration, and may be configured as a dedicated input if the buffer is always disabled.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops which are loaded on the low-to-high transition of the clock input.

Polarity

All outputs are active low.

Preload and Power-Up Reset

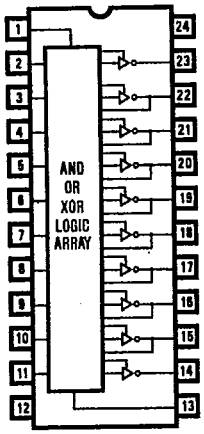
The 20X10A Series offers register preload for device testability. The registers can be preloaded from the outputs by using supervoltages in order to simplify functional testing. The 20X10A Series also offers Power-Up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

Packages

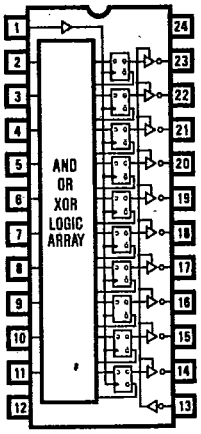
The commercial PAL20X10A Series is available in the plastic SKINNYDIP (NS), ceramic SKINNYDIP (JS), plastic leaded chip carrier (NL), and small outline (SG) packages.

DIP/SO Pinouts

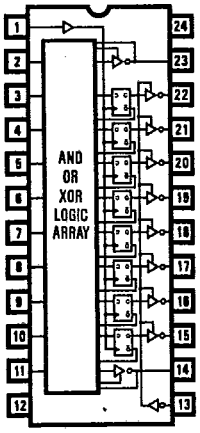
20L10A



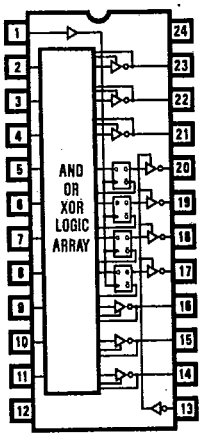
20X10A



20X8A

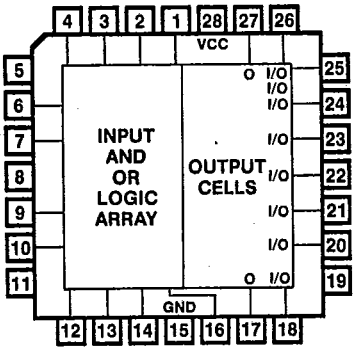


20X4A

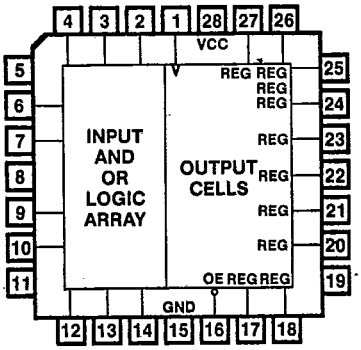


PLCC Pinouts

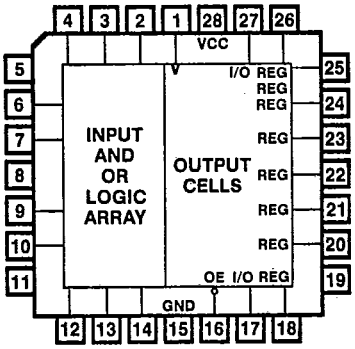
20L10A



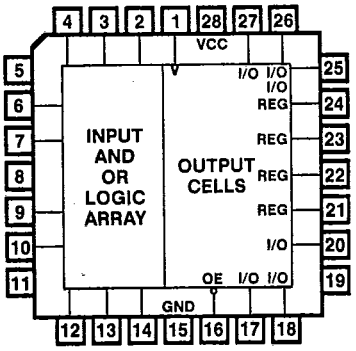
20X10A



20X8A



20X4A



ADV MICRO PLA/PLE/ARRAYS 96 DE 0257526 0027172 0

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7.0 V	−0.5 V to 12.0 V
Input voltage	−1.5 V to 5.5 V	−1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature		−65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1] MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	25	15		ns
		High	15	7		
t_{su}	Set up time from input or feedback to clock	20X10A, 20X8A, 20X4A	30	20		ns
t_h	Hold time		0	−15		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}[3]			V_O = 2.4 V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	20X10A,20X8A,20X4A		140	180	mA
			20L10A		115	165	

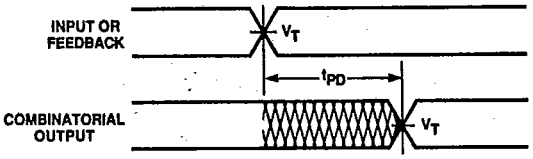
1. The PAL20X10A Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

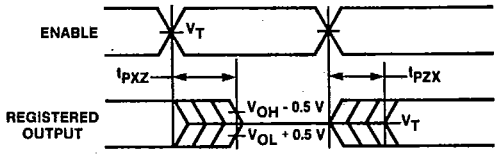
SYMBOL	PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output		20L10A, 20X8A, 20X4A	$R_1 = 200\ \Omega$, $R_2 = 390\ \Omega$		23	30	ns
t_{CLK}	Clock to output or feedback					10	15	ns
t_{PZX}	Pin 13 to output enable except 20L10A					11	20	ns
t_{PXZ}	Pin 13 to output disable except 20L10A					10	20	ns
t_{EA}	Input to output enable		20L10A, 20X8A, 20X4A			19	30	ns
t_{ER}	Input to output disable		20L10A, 20X8A, 20X4A			15	30	ns
f_{MAX}	Maximum frequency	External	20L10A, 20X8A, 20X4A		22.2	32		MHz
		No feedback			25	45		

ADV MICRO PLA/PLE/ARRAYS 96 DE 0257526 0027174 3

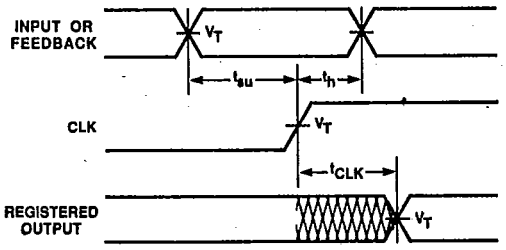
Switching Waveforms



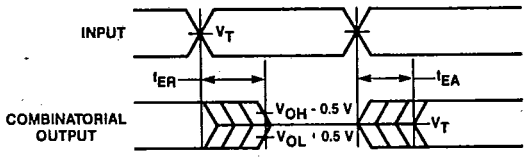
Combinatorial Output



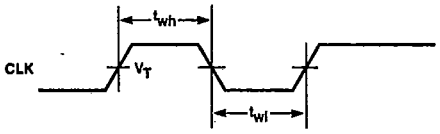
Pin 13 to Output Disable/Enable



Registered Output



Input to Output Disable/Enable



Clock Width

5

Key to Timing Diagrams

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Switching Test Load
(refer to page 5-164)

Programmers/Development Systems
(refer to Programmer Reference Guide, page 3-81)

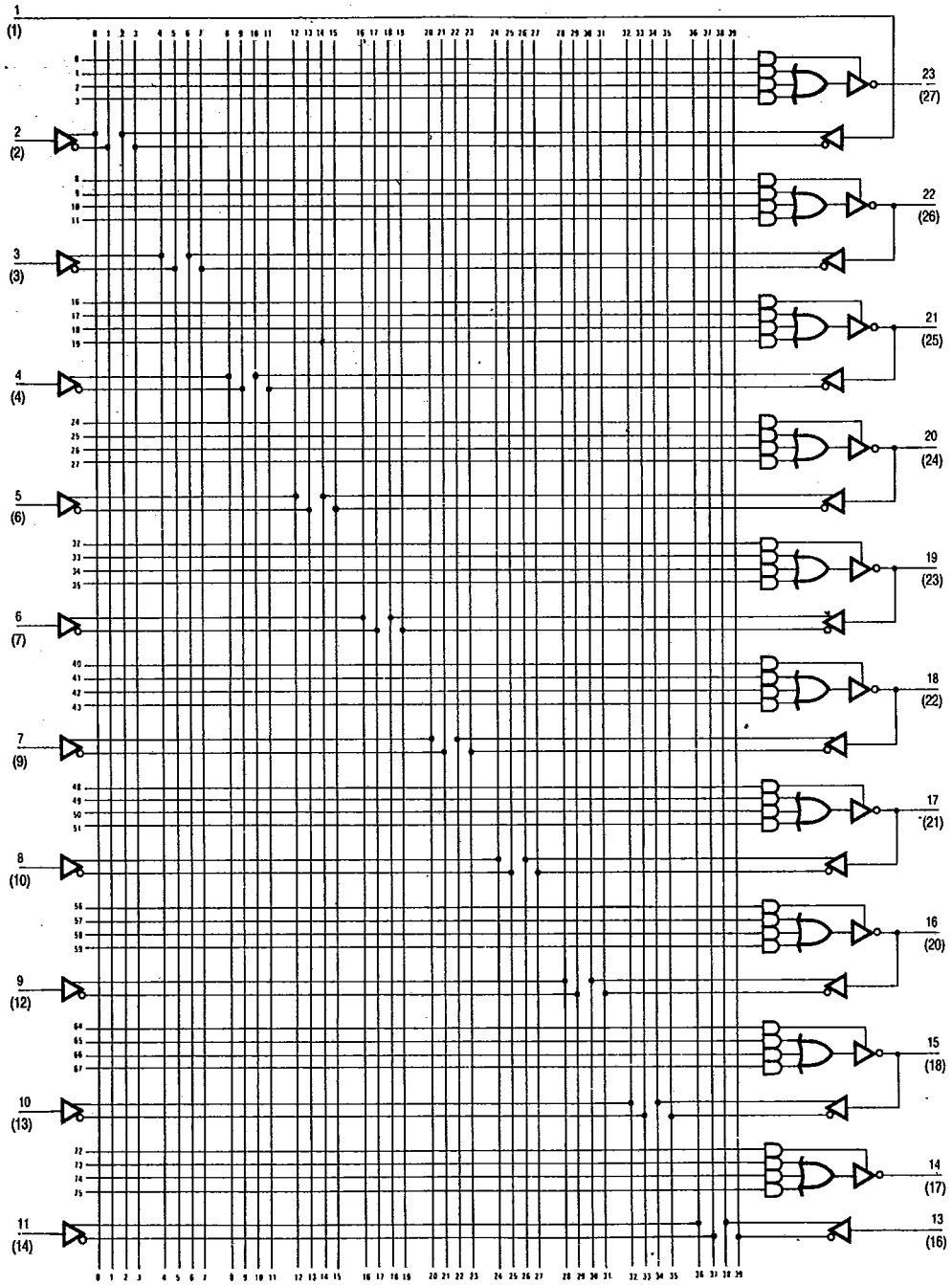
Register Preload Waveform
(refer to page 5-164)

Power-Up Reset Waveform
(refer to page 5-164)

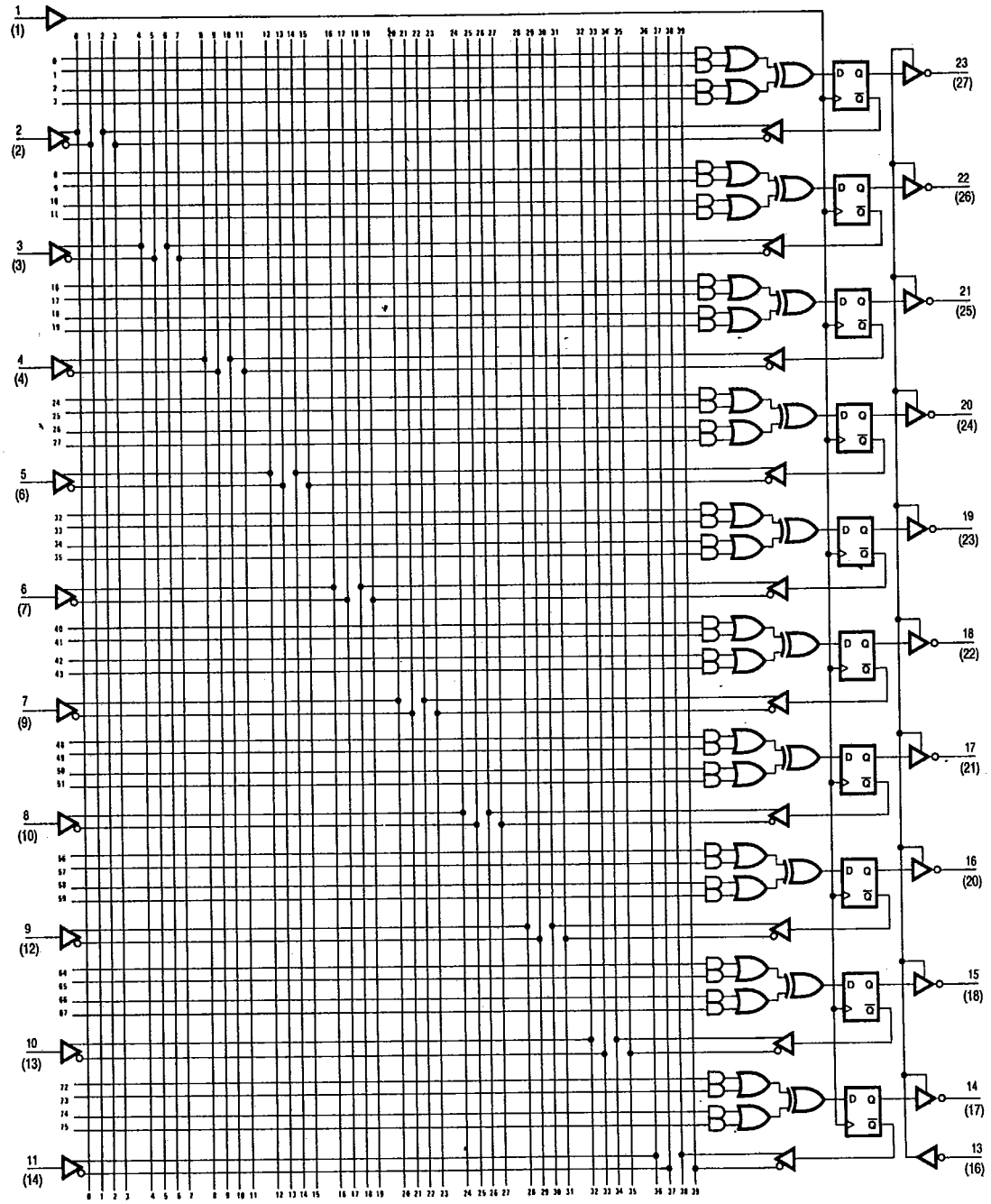
Schematic of Inputs and Outputs
(refer to page 5-164)

Package Drawings
(refer to PAL Device Package Outlines, page 3-179)

20L10


1
(1)
2
(2)
3
(3)
4
(4)
5
(6)
6
(7)
7
(9)
8
(10)
9
(12)
10
(13)
11
(14)
23
(27)
22
(26)
21
(25)
20
(24)
19
(23)
18
(22)
17
(21)
16
(20)
15
(18)
14
(17)
13
(16)

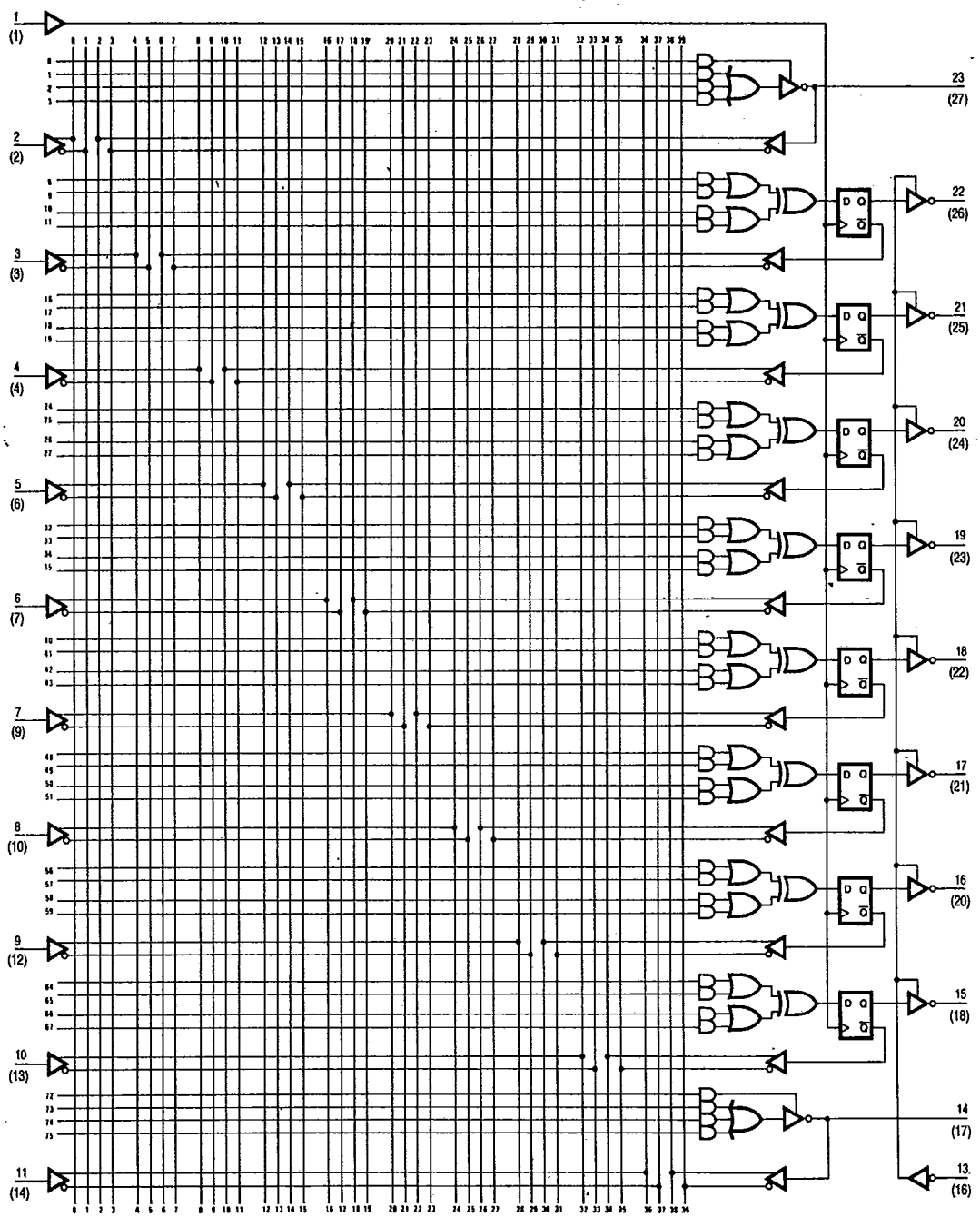
20X10


1 (1)
2 (2)
3 (3)
4 (4)
5 (6)
6 (7)
7 (9)
8 (10)
9 (12)
10 (13)
11 (14)
23 (27)
22 (26)
21 (25)
20 (24)
19 (23)
18 (22)
17 (21)
16 (20)
15 (18)
14 (17)
13 (16)
D Q
Q̄

5

T-46-13-47

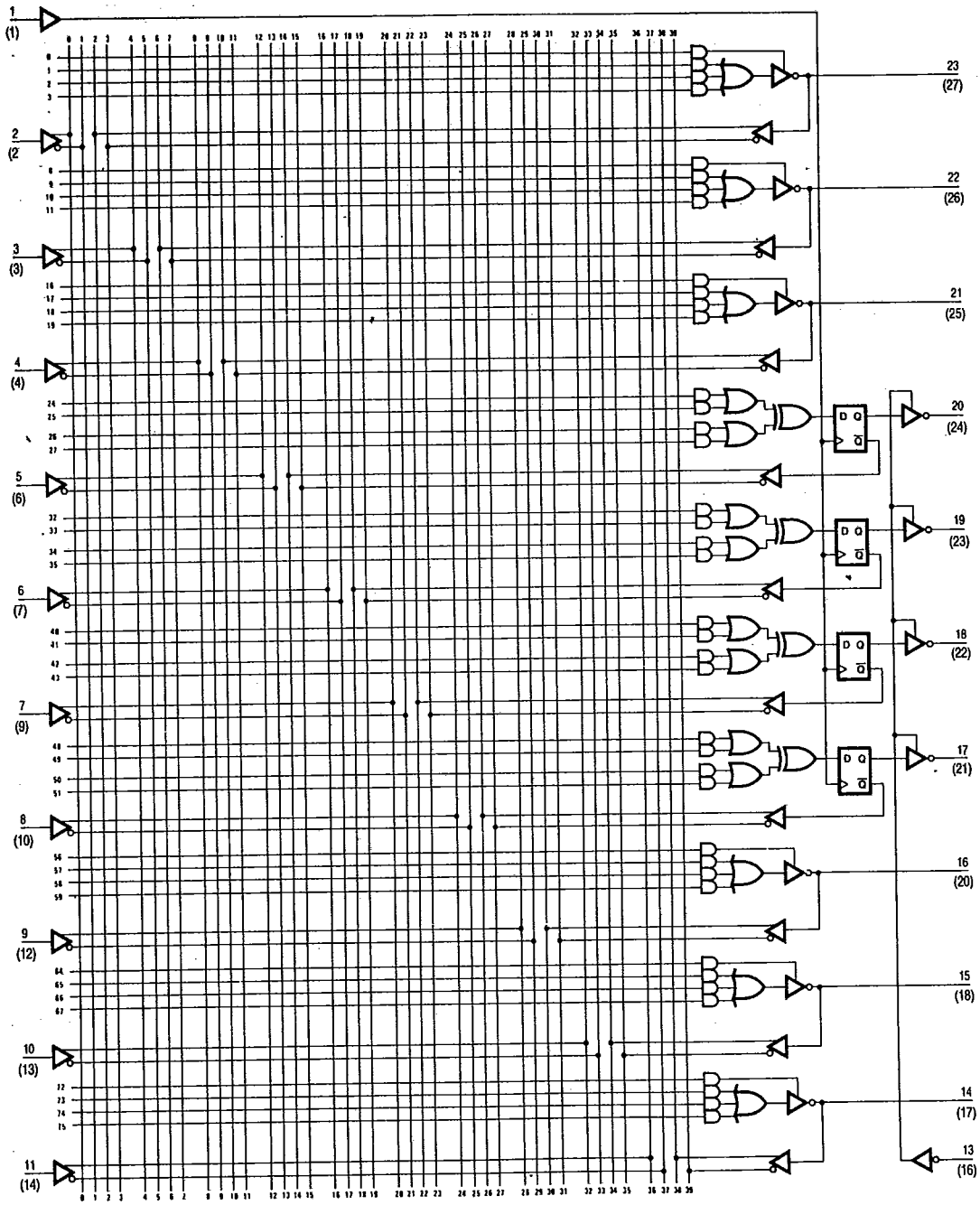
20X8



0257526 ADV MICRO PLA/PLE/ARRAYS 96D 27179 D

20X4

T-46-13-47



ADV MICRO PLA/PLE/ARRAYS 96 DE 0257526 0027179 2

5