

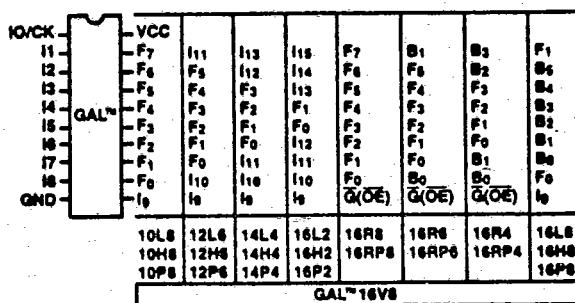
VP16V8E PRELIMINARY**GENERIC ARRAY LOGIC****FEATURES**

- Replaces all series 20 bipolar PAL* devices - Output Drive 24 mA IOL
- High performance CMOS technology -
 - Low Power: 90 mA Max Active 70 mA Max Standby
 - High Speed: 25 ns Access Max 35 ns Access Max
- EE Technology -
 - Reconfigurable Logic
 - Reprogrammable Fuses
 - 100% Testable

- Electronic signature word available to user - User-programmable ID code for inventory control
- User-programmable revision identification
- Security cell prevents logic copying
- Register Preload for complete testability
- Power-on reset of all registers
- High-speed programming algorithm
- JEDEC approved TTL compatible pin-out

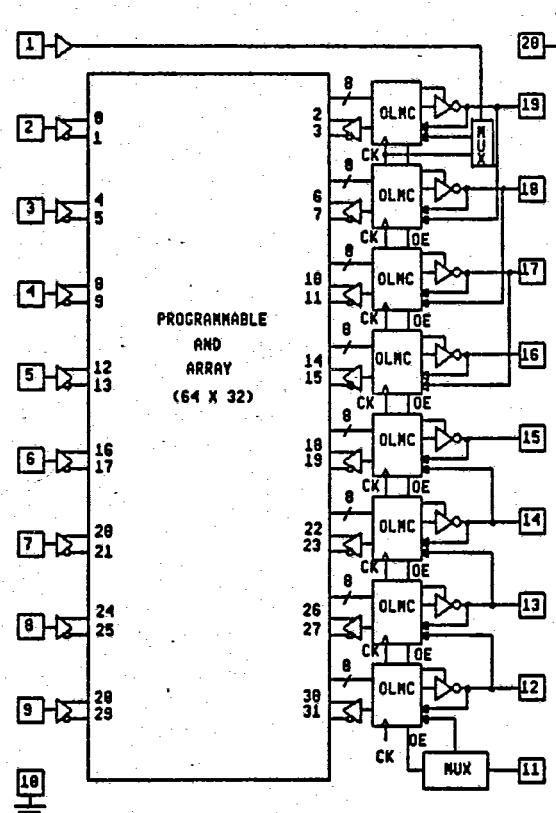
FUNCTIONAL BLOCK DIAGRAM**PIN NAMES**

I ₀ -I ₁₅	INPUT	G (OE)	OUTPUT ENABLE
CK	CLOCK INPUT		
B ₀ -B ₅	BI-DIRECTIONAL	V _{CC}	POWER (+5V)
F ₀ -F ₇	OUTPUT	GND	GROUND

PIN CONFIGURATION

GAL is a trademark of
Lattice Semiconductor

*PAL is a registered
trademark of Monolithic
Memories Inc.



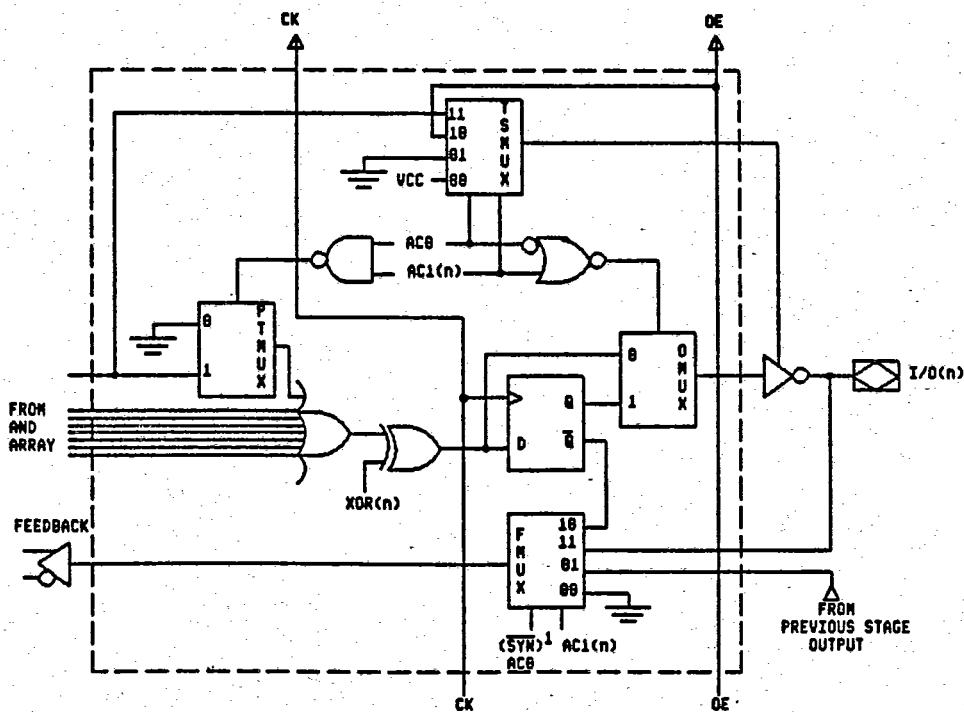
DESCRIPTION

The VTI Electrically Erasable GAL device, VP16V8E, combines a high performance CMOS process with electrically erasable floating gate technology. This proven programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

Unique test circuitry and reprogrammable fuses allow complete ac, dc, fuse and functionality testing during manufacture. Therefore, VTI guarantees 100% field

programmability and functionality of the GAL devices. In addition, electronic signature is available to provide positive device identification. A security circuit is built in, providing the user's proprietary circuit with copy protection.

The GAL device fuse map is logically equivalent to the industry standard PAL devices and is programmed with readily available hardware and software tools. VTI guarantees 100 erase/write cycles and data retention exceeding 10 years.



Output Logic Macrocell(n)

PRELIMINARY VP16V8E

OUTPUT LOGIC MACROCELL

The outputs of the AND array are fed into an output logic macrocell, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable can be connected to all outputs. Alternatively, separate inputs or product terms can be used to provide individual output enable controls. The output logic macrocell provides the designer with maximal output flexibility in matching signal requirements, thus potentially providing more functions than possible with existing 20-pin devices.

The various configurations of the output logic macrocell are controlled by programming certain cells (SYN, ACO, AC1(n), and the XOR(n) polarity bits) within the 82-bit architecture control word. The SYN bit determines whether or not a device will have registered output capability or will have purely combinational outputs. It also

replaces the ACO bit in the two outermost macrocells, OLMC (12) and OLMC (19). When first setting up the device architecture, this is the first bit to choose.

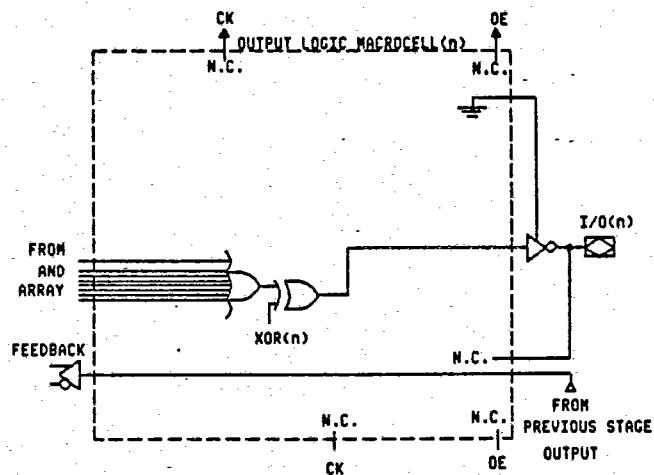
Architecture control bit ACO and the eight AC1(n) bits direct the outputs to be wired always on, always off (as an input), to have a common OE term (pin 11), or to be 3-state controlled separately from a product term. The architecture control bits also determine the source of the array feedback term through the FMUX, and select either combinational or registered outputs.

The five valid macrocell configurations are shown in each of the macrocell equivalent diagrams. In all cases, the eight XOR(n) bits individually determine each output's polarity. The truth table associated with each diagram shows the bit values of SYN, ACO, and AC1(n) that set the macrocell to the configuration shown.

Dedicated Input Mode

SYN	ACO	AC1(n)	FUNCTION
1	0	1	INPUT MODE (i.e. 10L8, 14P4)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 11 ARE DATA INPUTS.
THE OUTPUT BUFFER IS DISABLED.



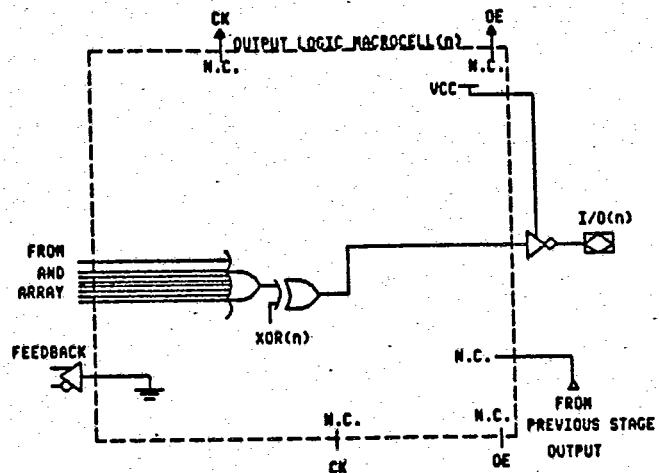
**Dedicated Combinational Output**

SYN	AC0	AC1(n)	FUNCTION
1	0	0	ALL OUTPUTS COMBINATIONAL (i.e. 10LB, 12HB)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 11 ARE DATA INPUTS.

ALL OUTPUTS ARE COMBINATIONAL AND
ALWAYS ACTIVE.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

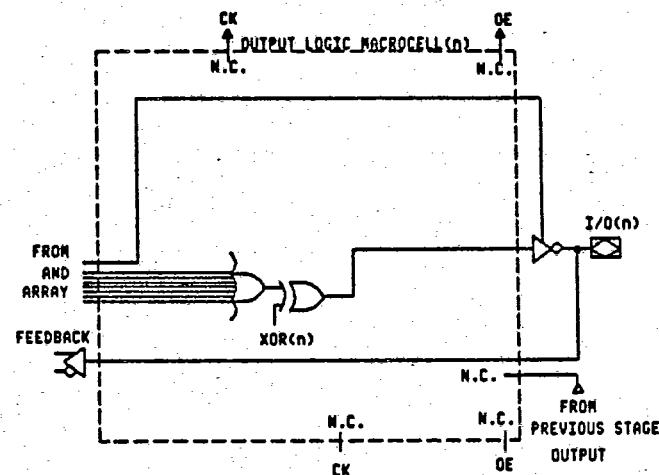
**Combinational Output**

SYN	AC0	AC1(n)	FUNCTION
1	1	1	ALL OUTPUTS COMBINATIONAL (i.e. 16LB, 16HB)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 11 ARE DATA INPUTS.

ALL OUTPUTS ARE COMBINATIONAL.

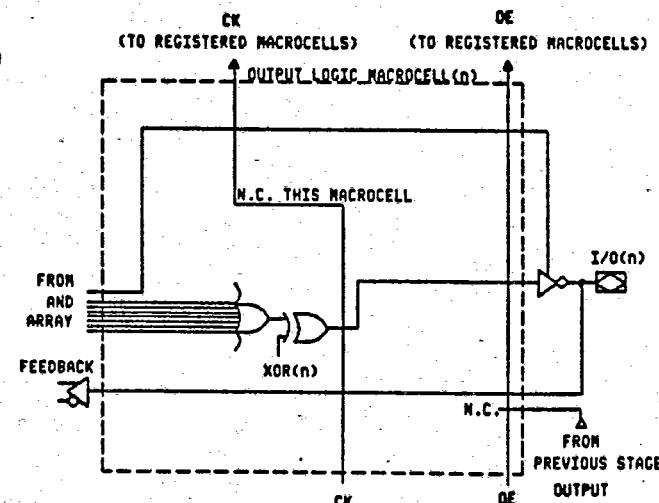
XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

**Combinational Output In a Registered Device**

SYN	AC0	AC1(n)	FUNCTION
0	1	1	COMBINATIONAL OUTPUT IN A REGISTERED DEVICE

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

IN THIS ARCHITECTURE MODE,
PIN 1 = CK, PIN 11 = OE. THIS MACROCELL
IS COMBINATIONAL, BUT AT LEAST ONE
OF THE OTHERS IS REGISTERED OUTPUT.

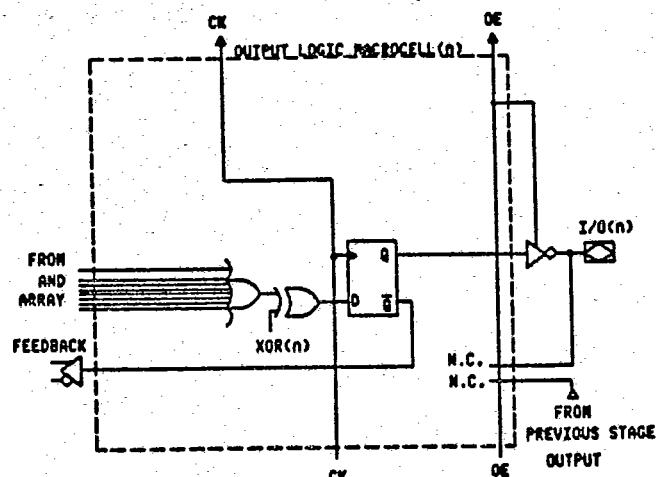




Registered Active High or Low Output

SYN	AC0	AC1(n)	FUNCTION
			OUTPUT REGISTERED (i.e. 16R8)
			IN THIS ARCHITECTURE MODE, PIN 1 = CK, PIN 11 = OE.

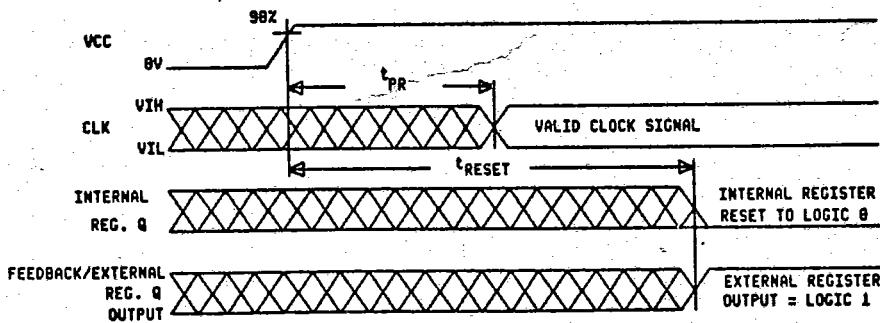
XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH



POWER-UP RESET

Circuitry within the VP16V8E provides a reset signal to all registers during power-up. All internal registers will have the Q outputs set LOW after a specified time (t_{RESET}). As a result, the state on the registered output pins, if they are enabled through OE, will always be HIGH on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the VP16V8E. First, the VCC rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.





ABSOLUTE MAXIMUM RATINGS

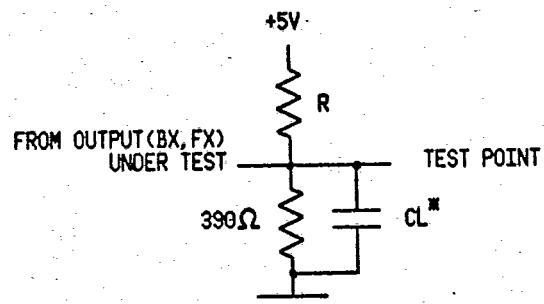
Storage temperature	-65° to +125° C
Ambient Temperature under bias	0° to +70° C
Input voltage on any pin relative to VSS Operating	-2.5 to +6.0 V
Supply voltage, VCC, with respect to VSS	-0.5 to +7 V
Off-state output voltage on any pin relative to VSS	-2.5 to +6.0 V

Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).

AC TEST CONDITIONS

Input Pulse Level	GND to 3.0 V
Input Rise and Fall Times (10% to 90% points)	5.0 ns
Input Timing Reference Level	1.5 V
Output Timing Reference Level	1.5 V
Output Load	See Figure

3-state levels are measured 0.5 V from steady-state active level.



* CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (TA = 25°C, F = 1 MHz)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C _I	Input Capacitance	12	pF	V _{CC} = 5.0V, V _I = 2.0V
C _F	Output Capacitance	15	pF	V _{CC} = 5.0V, V _F = 2.0V
C _B	Bidirectional Pin Cap	15	pF	V _{CC} = 5.0V, V _B = 2.0V

OPERATING RANGE

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T _A	Ambient temperature	-55		125	0		75	°C

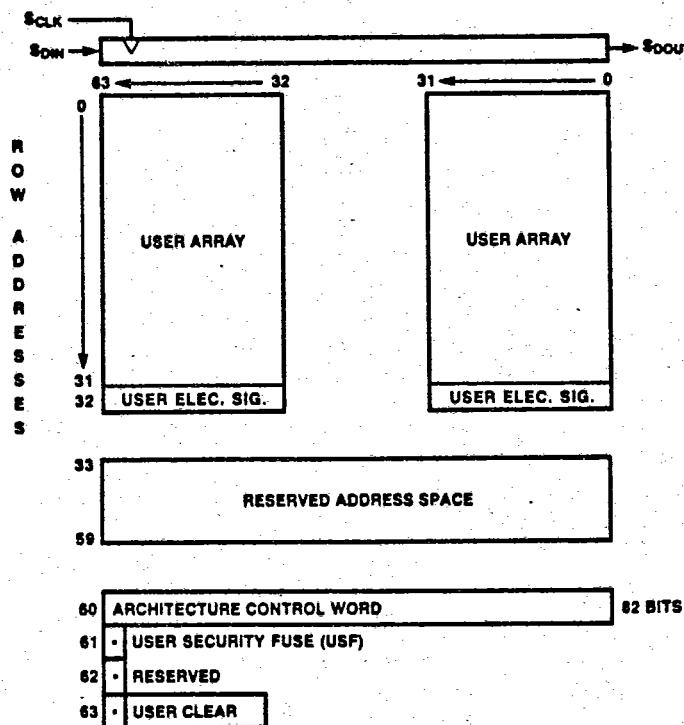


ROW ADDRESS MAP BLOCK DIAGRAM

There are a total of 36 unique row addresses available to the user when programming the 16V8 GAL devices. Row addresses 0-31 each contain 64 bits of input-term data. This is the user array where the custom logic pattern is programmed. Row 32 is the user electronic signature word. It has 64 bits available for any user-defined purpose. Rows 33-59 are reserved by the manufacturer and are not available to users.

Row 60 contains the architecture and output polarity information. The 82 bits within this word are programmed to configure the device for a specific application. Row 61 contains a one-bit security cell which, when programmed, prevents the user array from being read. Row 63 is the row which is addressed to perform a bulk erase of the device, resetting it back to a generic state. Each of these functions is described in the following sections.

ROW ADDRESS MAP BLOCK DIAGRAM





ARCHITECTURE CONTROL WORD DIAGRAM

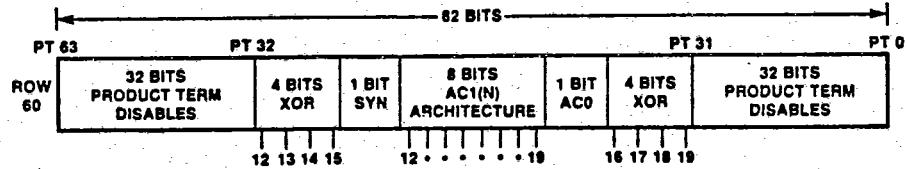
All configurations of the VP16V8E devices are controlled by programming cells within the 82-bit architecture control word which resides at row 60. The location of specific bits within the architecture control word is shown in the control word diagram. The function of the SYN, ACO and AC1(n) bits have been explained in the output logic macrocell description. The eight polarity bits determine each output's polarity individually by selecting the correct logic. The numbers below the XOR and AC1(n) bits in the architecture control word diagram show the device output pin number controlled by the polarity bits.

USER SIGNATURE WORD

A user signature word is provided with every VP16V8E device. It resides at row address 32 and contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user identification codes, revision numbers, or inventory control numbers. This signature data is always available to the user independent of the state of the security cell.

USER SECURITY CELL

Row address 61 contains the user security cell (one bit). The user security cell is provided on all VP16V8E devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the user array (rows 0-31). The cell can be erased only in conjunction with the user array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.





OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in normal machine operation. This is because, in system operation, certain events occur that may throw the logic into an illegal state, for example power-up line voltage glitches, brown-outs, etc. To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (legal or illegal) state into the registers. The machine can then be sequenced and the outputs tested for the correct subsequent state conditions.

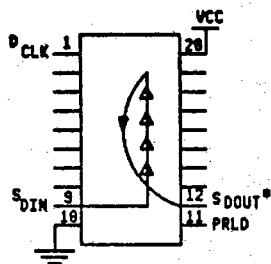
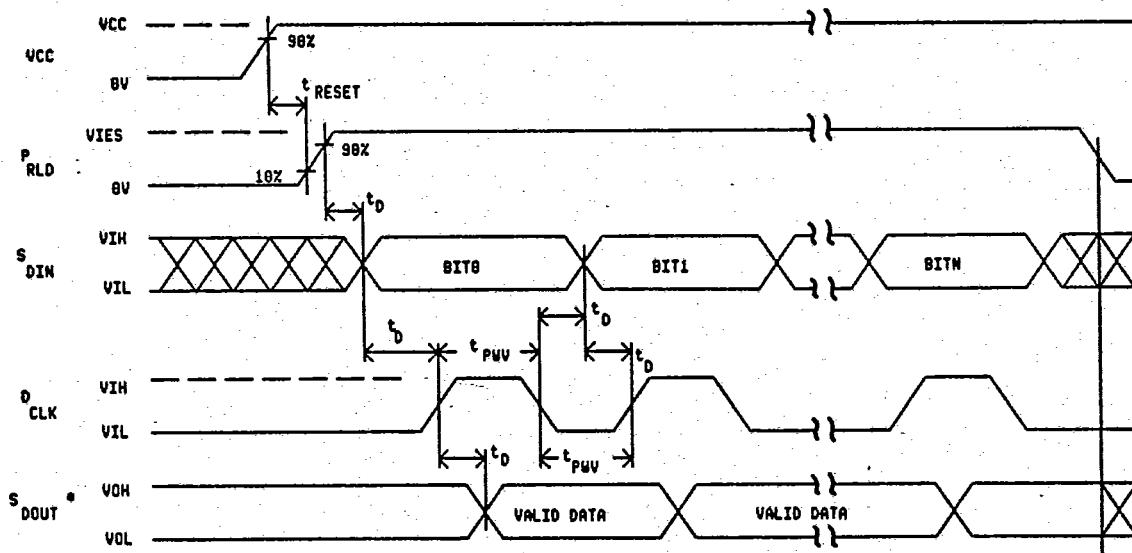
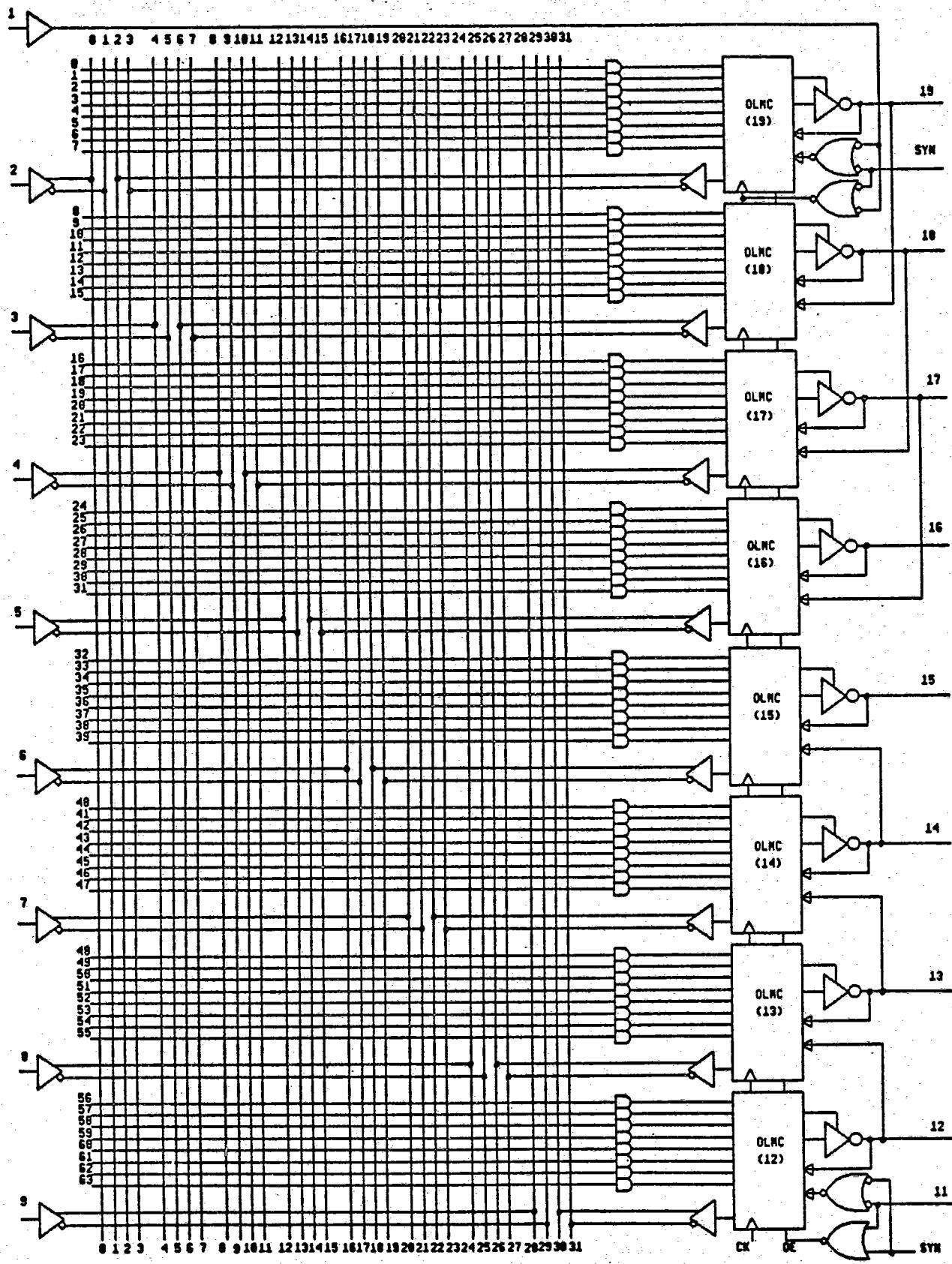


Fig.1 - Output Register Preload Pinout



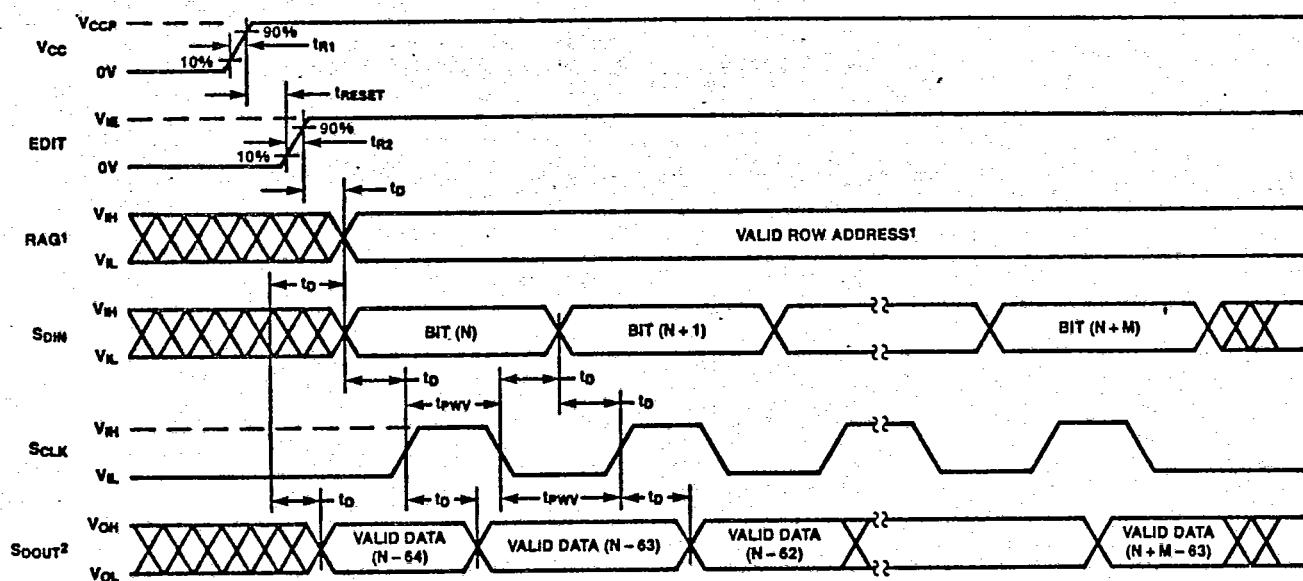
* NOTE - The SDOUT output buffer is an open drain output.

LOGIC DIAGRAM VP16V8E





SHIFT REGISTER I/O TIMING

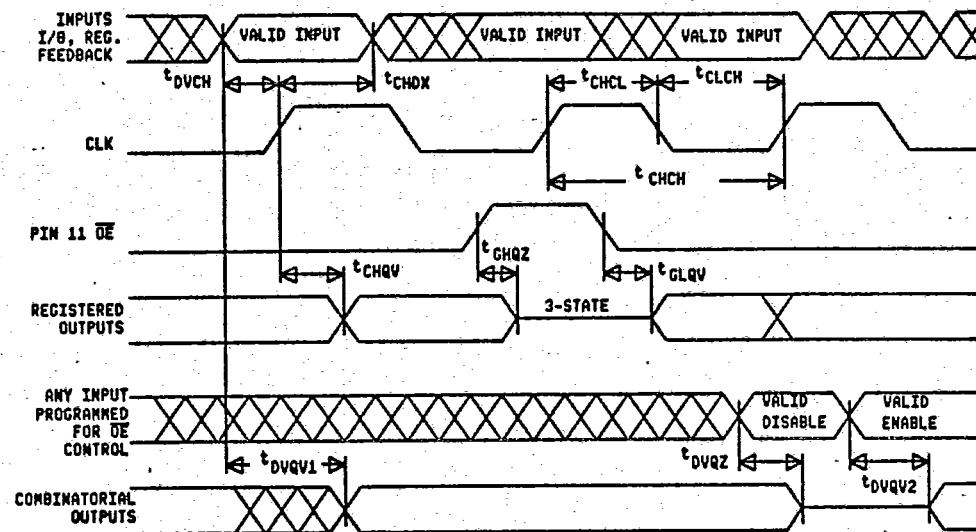


DC CHARACTERISTICS (TA = 0 to +70 °C, VDD = 5 V ±5%)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN.	MAX.	UNITS	
I _H , I _{IL}	Input Leakage Current		GND ≤ V _{IN} ≤ V _{CC} MAX		—	±10	µA	
I _{BZH} , I _{BZL}	Bidirectional Pin Leakage Current		GND ≤ V _{IN} < V _{CC} MAX		—	±10	µA	
I _{FZL} , I _{FZH}	Output Pin Leakage Current		GND ≤ V _{IN} ≤ V _{CC} MAX		—	±10	µA	
I _{CC}	Operating Power Supply Current		F = 15 MHz V _{CC} = V _{CC} MAX	COM'L	—	90	mA	
				MIL	—	120	mA	
I _{OS} ¹	Output Short Circuit		V _{CC} = 5.0V V _{OUT} = GND	—	-30	-130	mA	
I _{SB}	Standby Power Supply Current		V _{CC} = V _{CC} MAX	COM'L	—	70	mA	
				MIL	—	95	mA	
V _{OL}	Output Low Voltage	V _{CC} = V _{CC} MIN	I _{OL} = 24 mA ²	COM'L	—	0.5	V	
			I _{OL} = 12 mA	MIL	—	0.5	V	
V _{OH}	Output High Voltage	V _{CC} = V _{CC} MIN	I _{OH} = -3.2 mA	COM'L	2.4	—	V	
			I _{OH} = -2.0 mA	MIL	2.4	—	V	
V _{IH}	Input High Voltage				2.0	V _{CC} + 1	V	
V _{IL}	Input Low Voltage				—	0.8	V	

¹One output at a time for a maximum duration of one second.²I_{OL} is 24 mA for one pin active at a time. I_{OL} = 16 mA for all outputs active in parallel.

TIMING DIAGRAM



AC CHARACTERISTICS (TA = 0 to +70°C, VDD = 5 V ±5%)

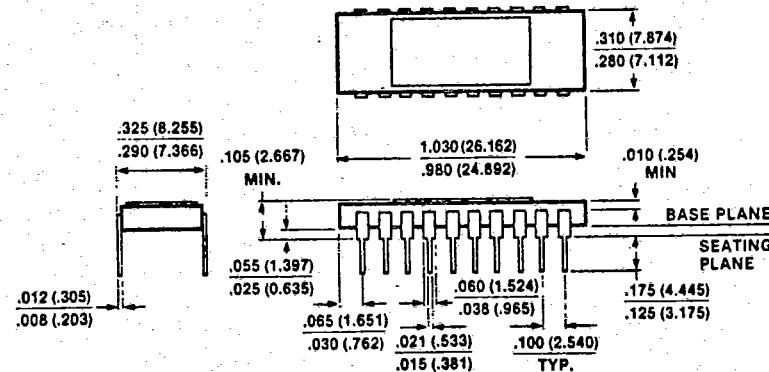
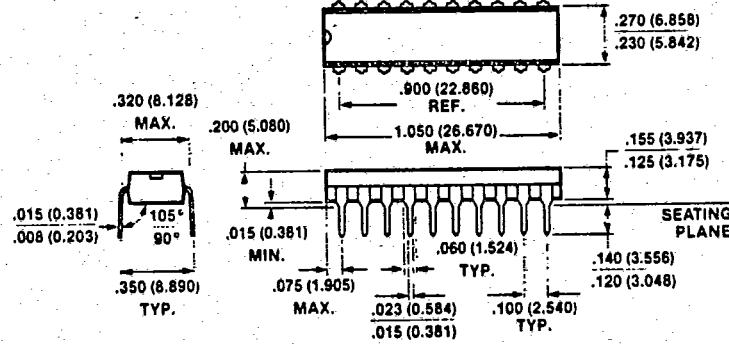
SYMBOL	PARAMETER	VP16V8E-25		VP16V8E		UNITS	TEST CONDITIONS ¹	
		MIN.	MAX.	MIN.	MAX.		R(Ω)	C _L (pF)
T _{DVQV1}	Delay from Input to Active Output	—	25	—	35	ns	200	50
T _{DVQV2}	Product Term Enable Access Time to Active Output	—	25	—	35	ns	Active High R = ∞ Active Low R = 200	50
T _{DVQZ} ²	Product Term Disable to Outputs Off	—	25	—	35	ns	From V _{OH} R = ∞ From V _{OL} R = 200	5
T _{GHQZ} ²	Pin 11 Output Enable High to Outputs Off	—	20	—	25	ns	From V _{OH} R = ∞ From V _{OL} R = 200	5
T _{GLOV}	Pin 11 Output Enable Access Time	—	20	—	25	ns	Active High R = ∞ Active Low R = 200	50
T _{CHQV}	Clock High to Output Valid Access Time	—	15	—	25	ns	200	50
T _{DVCH}	Input or Feedback Data Setup Time	20	—	30	—	ns	—	—
T _{CHDX}	Input or Feedback Data Hold Time	0	—	0	—	ns	—	—
T _{CHCH}	Clock Period (T _{DVCH} + T _{CHQV})	35	—	55	—	ns	—	—
T _{CHCL}	Clock Width High	15	—	20	—	ns	—	—
T _{CLCH}	Clock Width Low	15	—	20	—	ns	—	—
f _{MAX}	Maximum Frequency SYNCH. ASYNCH.	—	28.5 40.0	—	18.1 28.5	MHz	200	50

¹ Refer also to AC Test Conditions. 23-state levels are measured 0.5V from steady-state active level.

USER BULK ERASE MODE

By addressing row 63 during a programming cycle, a user clear function performs a bulk erase of the user array, the XOR cells, and the architecture word. In addition, the user electronic signature word and security cell are erased. This mode essentially resets a previously configured device to its generic state.

Bulk erase occurs by first applying VCCP to pin 20 and selecting the edit mode by applying VIE to pin 2, the EDIT select pin. Bulk erase is selected by addressing row 63 with SDIN at VIH. The bulk erase cycle is then begun by performing a programming pulse cycle. The edit mode must be exited and reentered before verifying that the array has been erased.

20-PIN SIDE-BRAZED CERAMIC DUAL IN-LINE**20-PIN PLASTIC DUAL IN-LINE**



ORDER INFORMATION

VP16V8E PC	35 ns	Commercial
VP16V8E DC		0 to 70 C
VP16V8E CC		
VP16V8E-25 PC	25 ns	Commercial
VP16V8E-25 DC		0 to 70 C
VP16V8E-25 CC		

NOTES:

PC suffix = Plastic dual in-line package

DC suffix = Cerdip dual in-line package

CC suffix = Side-brazed ceramic dual in-line package

SOFTWARE VENDOR

Source	Software Type	Systems Supported
Data I/O	ABEL Rev 1.13	IBM PC & Compatibles VAX VALID
Assisted Technology	CUPL	IBM PC & Compatibles VAX Valid

PROGRAMMER VENDOR

Vendor	Programmer Model(s)	VTI GAL Personality Module	VTI Socket Adapter
Data I/O 10525 Willows Rd, N.E. P.O. Box 97046 Redmond, WA, 98073 (206) 881-6444	29B	LOGIC PAK	303A-009
Stag Microsystems, 528-5 Weddell Dr., Sunnyvale, CA, 94089	PPZ Universal	N/A	N/A

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PRELIMINARY VP16V8E

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Fort Lauderdale, 305-429-8200
Melbourne, 305-725-1480

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INDIANA

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MARYLAND

Baltimore, 301-995-0003

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MICHIGAN

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Grand Rapids, 616-243-0912

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Fairfield, 201-575-5300

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