



512K × 8 CMOS FLASH MEMORY

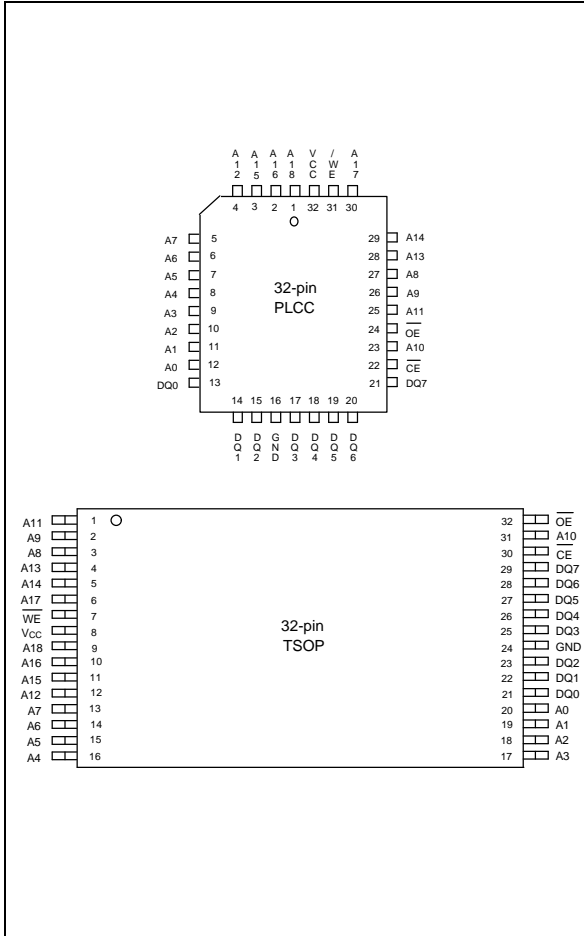
GENERAL DESCRIPTION

The W29C040 is a 4-megabit, 5-volt only CMOS page mode EEPROM organized as 512K × 8 bits. The device can be written (erased and programmed) in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W29C040 results in fast write (erase/program) operations with extremely low current consumption compared to other comparable 5-volt flash memory products. The device can also be written (erased and programmed) by using standard EPROM programmers.

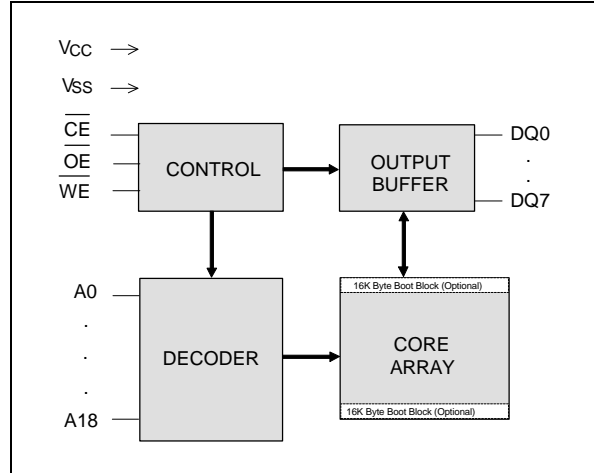
FEATURES

- Single 5-volt write (erase and program) operations
- Fast page-write operations
 - 256 bytes per page
 - Page write (erase/program) cycle: 5 mS (typ.)
 - Effective byte-write (erase/program) cycle time: 19.5 μS
 - Optional software-protected data write
- Fast chip-erase operation: 50 mS
- Two 16 KB boot blocks with lockout
- Typical page write (erase/program) cycles: 1K/10K (typ.)
- Read access time: 90/120 nS
- Ten-year data retention
- Software and hardware data protection
- Low power consumption
 - Active current: 25 mA (typ.)
 - Standby current: 20 μA (typ.)
- Automatic write (erase/program) timing with internal V_{PP} generation
- End of write (erase/program) detection
 - Toggle bit
 - Data polling
- Latched address and data
- All inputs and outputs directly TTL compatible
- JEDEC standard byte-wide pinouts
- Available packages: TSOP and PLCC

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | PIN NAME |
|-----------------|---------------------|
| A0-A18 | Address Inputs |
| DQ0-DQ7 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| \overline{WE} | Write Enable |
| Vcc | Power Supply |
| GND | Ground |



FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W29C040 is controlled by \overline{CE} and \overline{OE} , both Chip of which have to be low for the host to obtain data from the outputs. \overline{CE} is used for device selection. When \overline{CE} is high, the chip is de-selected and only standby power will be consumed. \overline{OE} is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either \overline{CE} or \overline{OE} is high.

Refer to the read cycle timing waveforms for further details.

Page Write Mode

The W29C040 is written (erased/programmed) on a page basis. Every page contains 256 bytes of data. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded will be erased to "FF hex" during the write operation of the page.

The write operation is initiated by forcing \overline{CE} and \overline{WE} low and \overline{OE} high. The write procedure consists of two steps. Step 1 is the byte-load cycle, in which the host writes to the page buffer of the device.

Step 2 is an internal write (erase/program) cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the byte-load cycle, the addresses are latched by the falling edge of either \overline{CE} or \overline{WE} , whichever occurs last. The data are latched by the rising edge of either \overline{CE} or \overline{WE} , whichever occurs first. If the host loads a second byte into the page buffer within a byte-load cycle time (TBLC) of 200 μ S after the initial byte-load cycle, the W29C040 will stay in the page load cycle. Additional bytes can then be loaded consecutively. The page load cycle will be terminated and the internal write (erase/program) cycle will start if no additional byte is loaded into the page buffer. A8 to A18 specify the page address. All bytes that are loaded into the page buffer must have the same page address. A0 to A7 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

In the internal write cycle, all data in the page buffers, i.e., 256 bytes of data, are written simultaneously into the memory array. The typical write (erase/program) time is 5 mS. The entire memory array can be written in 10.4 seconds. Before the completion of the internal write cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

Software-protected Data Write

The device provides a JEDEC-approved optional software-protected data write. Once this scheme is enabled, any write operation requires a three-byte command sequence (with specific data to a specific address) to be performed before the data load operation. The three-byte load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29C040 is shipped with the software data protection enabled. To enable the software data protection scheme, perform the three-byte command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-byte command sequence cycle. Once enabled, the software data protection



will remain enabled unless the disable commands are issued. A power transition will not reset the software

data protection feature. To reset the device to unprotected mode, a six byte command sequence is required. For information about specific codes, see the Command Codes for Software Data Protection in the Table of Operating Modes. For information about timing waveforms, see the timing diagrams below.

Hardware Data Protection

The integrity of the data stored in the W29C040 is also hardware protected in the following ways:

- (1) Noise/Glitch Protection: A \overline{WE} pulse of less than 15 nS in duration will not initiate a write cycle.
- (2) Vcc Power Up/Down Detection: The write operation is inhibited when Vcc is less than 2.5V.
- (3) Write Inhibit Mode: Forcing \overline{OE} low, \overline{CE} high, or \overline{WE} high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.
- (4) Vcc power-on delay: When Vcc has reach its sense level, the device will automatically time-out 10 mS before any write (erase/program) operation.

Chip Erase Modes

The entire device can be erased by using a six-byte software command code. See the Software Chip Erase Timing Diagram.

Boot Block Operation

There are two boot blocks (16K bytes each) in this device, which can be used to store boot code. One of them is located in the first 16K bytes and the other is located in the last 16K bytes of the memory. The first 16K or last 16K of the memory can be set as a boot block by using a seven-byte command sequence.

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout); other memory locations can be changed by the regular programming method. Once the boot block programming lockout feature is activated, the chip erase function will be disabled. In order to detect whether the boot block feature is set on the two 16K blocks, users can perform a six-byte command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "00002 hex" (for the first 16K bytes) or "7FFF2 hex" (for the last 16K bytes). If the output data is "FF hex," the boot block programming lockout feature is activated; if the output data is "FE hex," the lockout feature is inactivated and the block can be programmed.

To return to normal operation, perform a three-byte command sequence to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Data Polling (DQ7)- Write Status Detection

The W29C040 includes a data polling feature to indicate the end of a write cycle. When the W29C040 is in the internal write cycle, any attempt to read DQ7 of the last byte loaded during the page/byte-load cycle will receive the complement of the true data. Once the write cycle is completed. DQ7 will show the true data. See the \overline{DATA} Polling Timing Diagram.



Toggle Bit (DQ6)- Write Status Detection

In addition to data polling, the W29C040 provides another method for determining the end of a write cycle. During the internal write cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the write cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation. See Toggle Bit Timing Diagram.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-byte command sequence can be used to access the product ID. A read from address "00000 hex" outputs the manufacturer code "DA hex." A read from address "00001 hex" outputs the device code "46 hex." The product ID operation can be terminated by a three-byte command sequence.

In the hardware access mode, access to the product ID is activated by forcing \overline{CE} and \overline{OE} low, \overline{WE} high, and raising A9 to 12 volts.

TABLE OF OPERATING MODES

Operating Mode Selection

Operating Range: 0 to 70° C (Ambient Temperature), $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $V_{HH} = 12V$

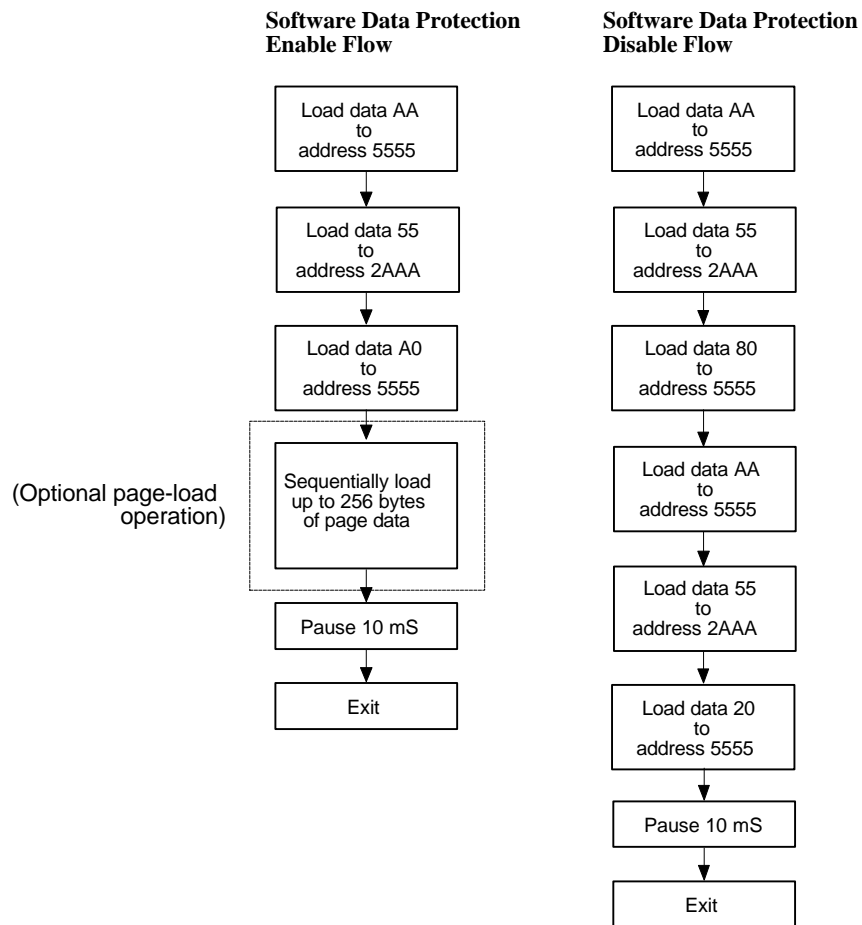
| MODE | PINS | | | | |
|----------------|-----------------|-----------------|-----------------|---|-------------------------------|
| | \overline{CE} | \overline{OE} | \overline{WE} | ADDRESS | DQ. |
| Read | V _{IL} | V _{IL} | V _{IH} | A _{IN} | Dout |
| Write | V _{IL} | V _{IH} | V _{IL} | A _{IN} | Din |
| Standby | V _{IH} | X | X | X | High Z |
| Write Inhibit | X | V _{IL} | X | X | High Z/DOUT |
| | X | X | V _{IH} | X | High Z/DOUT |
| Output Disable | X | V _{IH} | X | X | High Z |
| Product ID | V _{IL} | V _{IL} | V _{IH} | A0 = V _{IL} ; A1–A18 = V _{IL} ; A9 = V _{HH} | Manufacturer Code DA (Hex) |
| | V _{IL} | V _{IL} | V _{IH} | A0 = V _{IH} ; A1–A18 = V _{IL} ; A9 = V _{HH} | Device Code 46 (Hex) |



Command Codes for Software Data Protection

| BYTE SEQUENCE | TO ENABLE PROTECTION | | TO DISABLE PROTECTION | |
|---------------|----------------------|------|-----------------------|------|
| | ADDRESS | DATA | ADDRESS | DATA |
| 0 Write | 5555H | AAH | 5555H | AAH |
| 1 Write | 2AAAH | 55H | 2AAAH | 55H |
| 2 Write | 5555H | A0H | 5555H | 80H |
| 3 Write | - | - | 5555H | AAH |
| 4 Write | - | - | 2AAAH | 55H |
| 5 Write | - | - | 5555H | 20H |

Software Data Protection Acquisition Flow



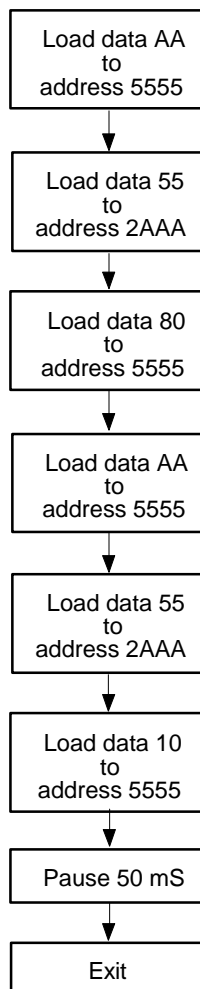
Notes for software program code:
 Data Format: DQ7–DQ0 (Hex)
 Address Format: A14–A0 (Hex)



Command Codes for Software Chip Erase

| BYTE SEQUENCE | ADDRESS | DATA |
|---------------|---------|------|
| 0 Write | 5555H | AAH |
| 1 Write | 2AAAH | 55H |
| 2 Write | 5555H | 80H |
| 3 Write | 5555H | AAH |
| 4 Write | 2AAAH | 55H |
| 5 Write | 5555H | 10H |

Software Chip Erase Acquisition Flow



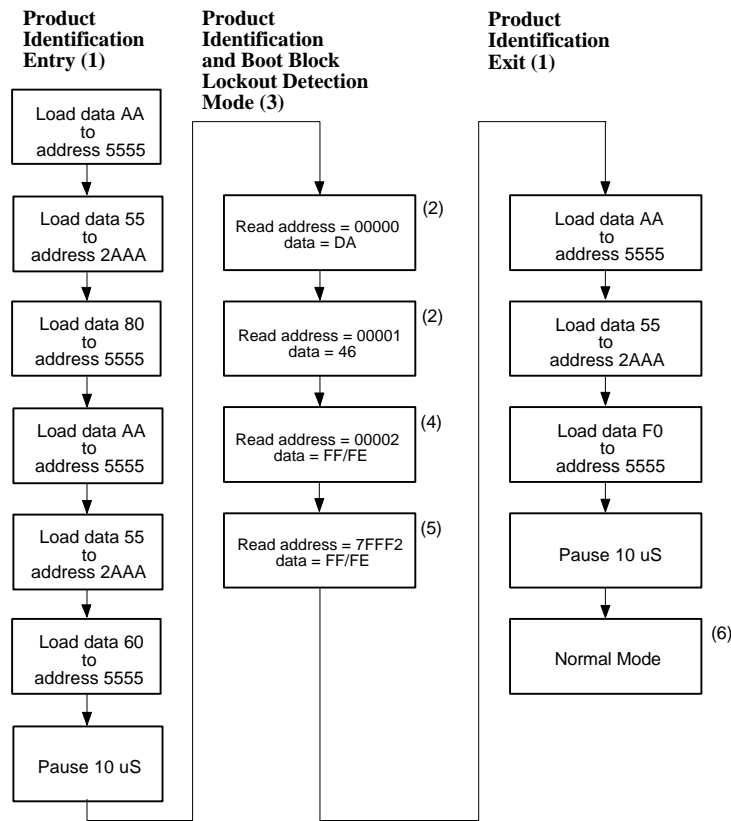
Notes for software chip erase:
 Data Format: DQ7–DQ0 (Hex)
 Address Format: A14–A0 (Hex)



Command Codes for Product Identification and Boot Block Lockout Detection

| BYTE SEQUENCE | ALTERNATE PRODUCT (7) IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY | | SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY | | SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION EXIT | |
|---------------|---|------|--|------|---|------|
| | ADDRESS | DATA | ADDRESS | DATA | ADDRESS | DATA |
| 0 Write | 5555 | AA | 5555H | AAH | 5555H | AAH |
| 1 Write | 2AAA | 55 | 2AAAH | 55H | 2AAAH | 55H |
| 2 Write | 5555 | 90 | 5555H | 80H | 5555H | F0H |
| 3 Write | - | - | 5555H | AAH | - | - |
| 4 Write | - | - | 2AAAH | 55H | - | - |
| 5 Write | - | - | 5555H | 60H | - | - |
| | Pause 10 μS | | Pause 10 μS | | Pause 10 μS | |

Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

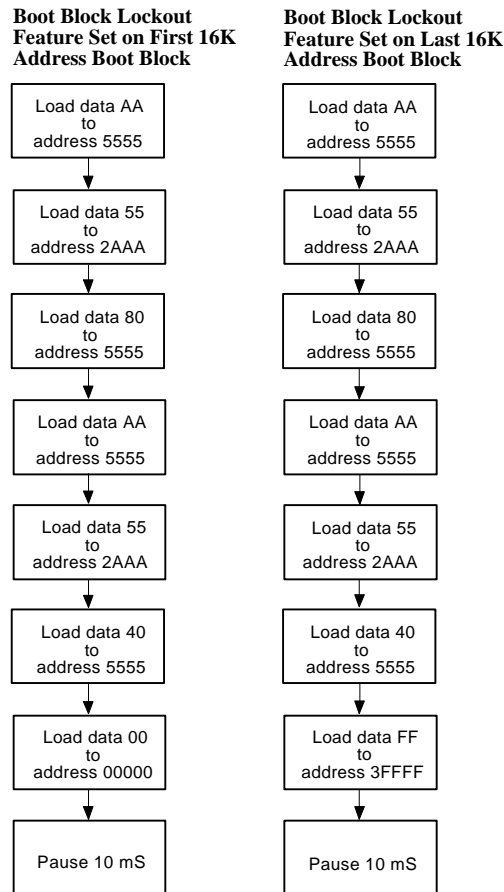
- (1) Data Format: DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)
- (2) A1–A18 = VIL; manufacture code is read for A0 = VIL; device code is read for A0 = VIH.
- (3) The device does not remain in identification and boot block (address 0002 Hex/7FFF2 Hex respond to first 16K/last 16K) lockout detection mode if power down.
- (4), (5) If the output data is "FF Hex," the boot block programming lockout feature is activated; if the output data "FE Hex," the lockout feature is inactivated and the block can be programmed.
- (6) The device returns to standard operation mode.
- (7) This product supports both the JEDEC standard 3 byte command code sequence and original 6 byte command code sequence. For new designs, Winbond recommends that the 3 byte command code sequence be used.



Command Codes for Boot Block Lockout Enable

| BYTE SEQUENCE | BOOT BLOCK LOCKOUT FEATURE SET ON FIRST 16K ADDRESS BOOT BLOCK | | BOOT BLOCK LOCKOUT FEATURE SET ON LAST 16K ADDRESS BOOT BLOCK | |
|---------------|--|------|---|------|
| | ADDRESS | DATA | ADDRESS | DATA |
| 0 Write | 5555H | AAH | 5555H | AAH |
| 1 Write | 2AAAH | 55H | 2AAAH | 55H |
| 2 Write | 5555H | 80H | 5555H | 80H |
| 3 Write | 5555H | AAH | 5555H | AAH |
| 4 Write | 2AAAH | 55H | 2AAAH | 55H |
| 5 Write | 5555H | 40H | 5555H | 40H |
| 6 Write | 00000H | 00H | 3FFFFH | FFH |
| | Pause 10 mS | | Pause 10 mS | |

Boot Block Lockout Enable Acquisition Flow



Notes for boot block lockout enable:

1. Data Format: DQ7–DQ0 (Hex)
2. Address Format: A14–A0 (Hex)
3. If you have any questions about this command sequence, please contact the local distributor or Winbond Electronics Corp.



DC CHARACTERISTICS

Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|--|------------------|------|
| Power Supply Voltage to Vss Potential | -0.5 to +7.0 | V |
| Operating Temperature | 0 to +70 | °C |
| Storage Temperature | -65 to +150 | °C |
| D.C. Voltage on Any Pin to Ground Potential Except A9 | -0.5 to VDD +1.0 | V |
| Transient Voltage (<20 nS) on Any Pin to Ground Potential | -1.0 to VDD +1.0 | V |
| Voltage on A9 and \overline{OE} Pin to Ground Potential | -0.5 to 12.5 | V |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VDD = 5.0V ±10%, Vss = 0V, TA = 0 to 70° C)

| PARAMETER | SYM. | TEST CONDITIONS | LIMITS | | | UNIT |
|-------------------------------------|------|---|--------|------|------|------|
| | | | MIN. | TYP. | MAX. | |
| Power Supply Current | ICC | $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all DQs open Address inputs = V_{IL}/V_{IH} , at f = 5 MHz | - | - | 50 | mA |
| Standby VDD Current (TTL input) | ISB1 | $\overline{CE} = V_{IH}$, all DQs open Other inputs = V_{IL}/V_{IH} | - | 2 | 3 | mA |
| Standby VDD Current (CMOS input) | ISB2 | $\overline{CE} = V_{DD} - 0.3V$, all DQs open | - | 20 | 100 | μA |
| Input Leakage Current | ILI | VIN = GND to VDD | - | - | 10 | μA |
| Output Leakage Current | ILO | VIN = GND to VDD | - | - | 10 | μA |
| Input Low Voltage | VIL | - | - | - | 0.8 | V |
| Input High Voltage | VIH | - | 2.0 | - | - | V |
| Output Low Voltage | VOL | IOL = 2.0 mA | - | - | 0.45 | V |
| Output High Voltage | VOH1 | IOH = -400 μA | 2.4 | - | - | V |
| Output High Voltage CMOS | VOH2 | IOH = -100 μA; VCC = 4.5V | 4.2 | - | - | V |



Power-up Timing

| PARAMETER | SYMBOL | TYPICAL | UNIT |
|-----------------------------|------------------------|---------|------|
| Power-up to Read Operation | T _{PU. READ} | 100 | μS |
| Power-up to Write Operation | T _{PU. WRITE} | 10 | mS |

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

| PARAMETER | SYMBOL | CONDITIONS | MAX. | UNIT |
|-----------------------|-----------------|----------------------|------|------|
| DQ Pin Capacitance | C _{DQ} | V _{DQ} = 0V | 12 | pF |
| Input Pin Capacitance | C _{IN} | V _{IN} = 0V | 6 | pF |

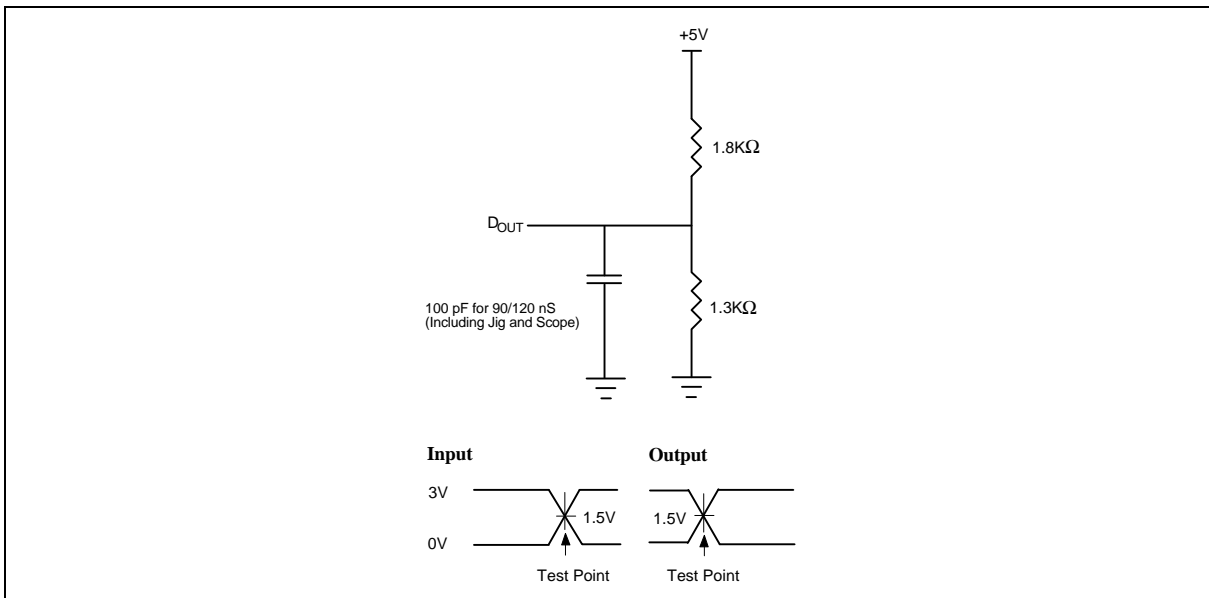
AC CHARACTERISTICS

AC Test Conditions

(V_{DD} = 5.0V ±10% for 90,120 nS)

| PARAMETER | CONDITIONS |
|---------------------------|--|
| Input Pulse Levels | 0V to 3V |
| Input Rise/Fall Time | <5 nS |
| Input/Output Timing Level | 1.5V/1.5V |
| Output Load | 1 TTL Gate and C _L = 100 pF for 90/120/150 nS |

AC Test Load and Waveform





AC Characteristics, continued

Read Cycle Timing Parameters(V_{DD} = 5.0V ±10% for 90,120 and 150 nS, V_{SS} = 0V, T_A = 0 to 70° C)

| PARAMETER | SYM. | W29C040-90 | | W29C040-12 | | UNIT |
|--|------|------------|------|------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | TRC | 90 | - | 120 | - | nS |
| Chip Enable Access Time | TCE | - | 90 | - | 120 | nS |
| Address Access Time | TAA | - | 90 | - | 120 | nS |
| Output Enable Access Time | TOE | - | 40 | - | 50 | nS |
| $\overline{\text{CE}}$ High to High-Z Output | TCHZ | - | 25 | - | 30 | nS |
| $\overline{\text{OE}}$ High to High-Z Output | TOHZ | - | 25 | - | 30 | nS |
| Output Hold from Address change | TOH | 0 | - | 0 | - | nS |

Byte/Page-write Cycle Timing Parameters

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|--------|------|------|------|------|
| Write Cycle (erase and program) | TWC | - | - | 10 | mS |
| Address Setup Time | TAS | 0 | - | - | nS |
| Address Hold Time | TAH | 50 | - | - | nS |
| $\overline{\text{WE}}$ and $\overline{\text{CE}}$ Setup Time | TCS | 0 | - | - | nS |
| $\overline{\text{WE}}$ and $\overline{\text{CE}}$ Hold Time | TCH | 0 | - | - | nS |
| $\overline{\text{OE}}$ High Setup Time | TOES | 0 | - | - | nS |
| $\overline{\text{OE}}$ High Hold Time | TOEH | 0 | - | - | nS |
| $\overline{\text{CE}}$ Pulse Width | TCP | 70 | - | - | nS |
| $\overline{\text{WE}}$ Pulse Width | TWP | 70 | - | - | nS |
| $\overline{\text{WE}}$ High Width | TWPH | 100 | - | - | nS |
| Data Setup Time | TDS | 50 | - | - | nS |
| Data Hold Time | TDH | 0 | - | - | nS |
| Byte Load Cycle Time | TBLC | - | - | 150 | μS |

Notes:

All AC timing signals observe the following guideline for determining setup and hold times:

- (1) High level signal's reference level is V_{IH}
- (2) Low level signal's reference level is V_{IL}



AC Characteristics, continued

DATA Polling Characteristics (1)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|------------------|------|------|------|------|
| Data Hold Time | T _{DH} | 10 | - | - | nS |
| $\overline{\text{OE}}$ Hold Time | T _{OEH} | 10 | - | - | nS |
| $\overline{\text{OE}}$ to Output Delay (2) | T _{OE} | - | - | - | nS |
| Write Recovery Time | T _{WR} | 0 | - | - | nS |

Notes:

- (1) These parameters are characterized and not 100% tested.
- (2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

Toggle Bit Characteristics (1)

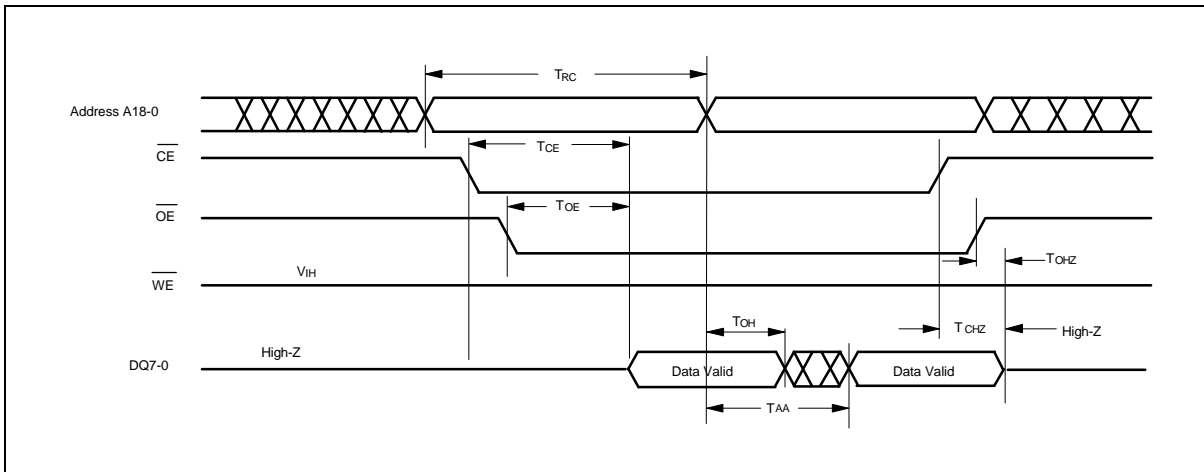
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|-------------------|------|------|------|------|
| Data Hold Time | T _{DH} | 10 | - | - | nS |
| $\overline{\text{OE}}$ Hold Time | T _{OEH} | 10 | - | - | nS |
| $\overline{\text{OE}}$ to Output Delay (2) | T _{OE} | - | - | - | nS |
| $\overline{\text{OE}}$ High Pulse | T _{OEHP} | 150 | - | - | nS |
| Write Recovery Time | T _{WR} | 0 | - | - | nS |

Notes:

- (1) These parameters are characterized and not 100% tested.
- (2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

TIMING WAVEFORMS

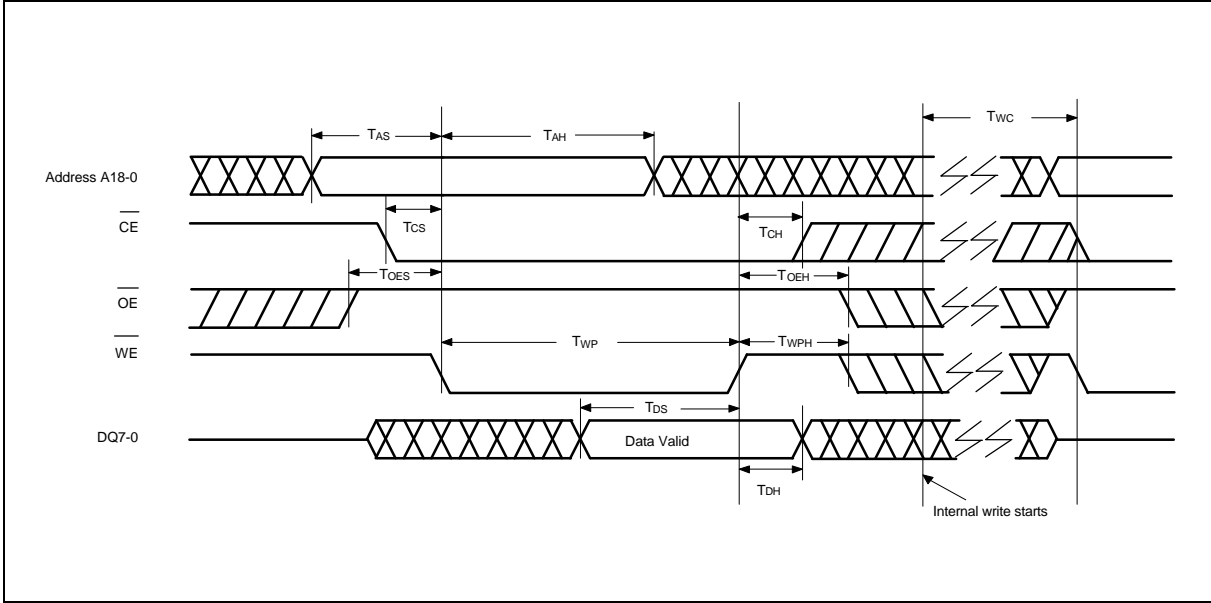
Read Cycle Timing Diagram



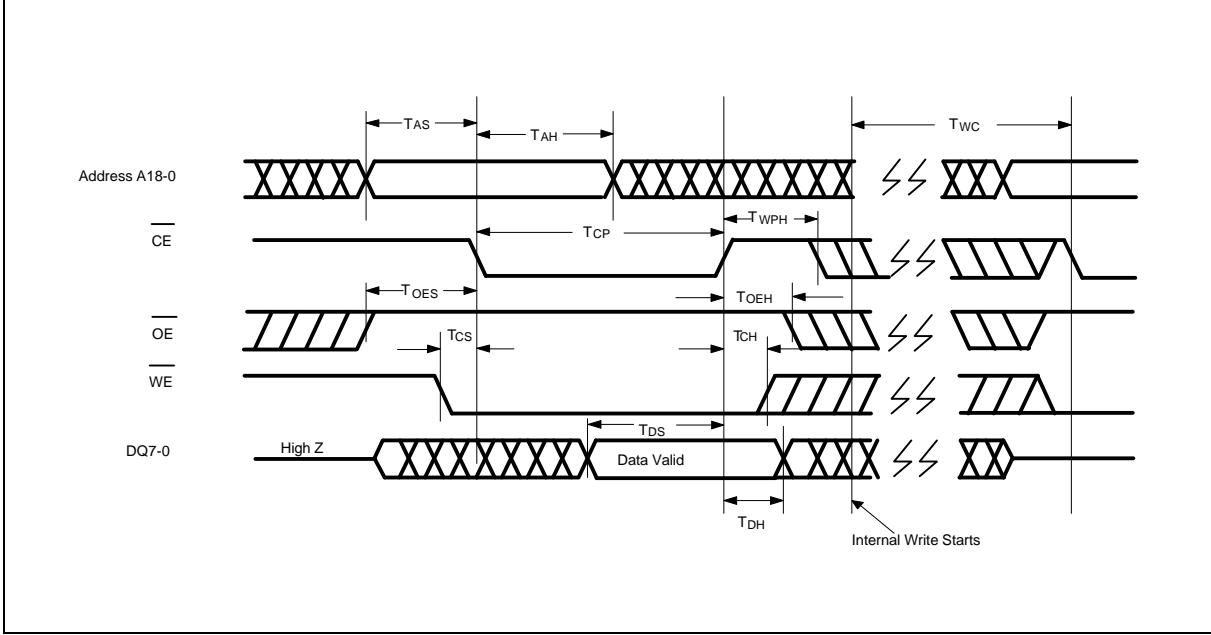


Timing Waveforms, continued

\overline{WE} Controlled Write Cycle Timing Diagram



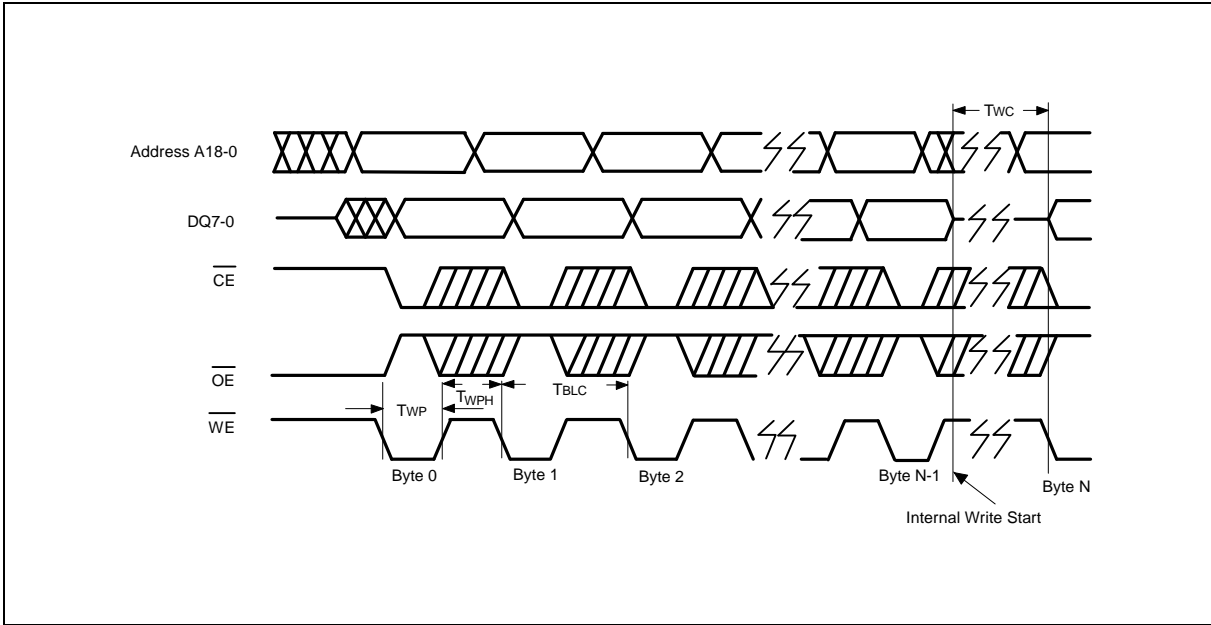
\overline{CE} Controlled Write Cycle Timing Diagram



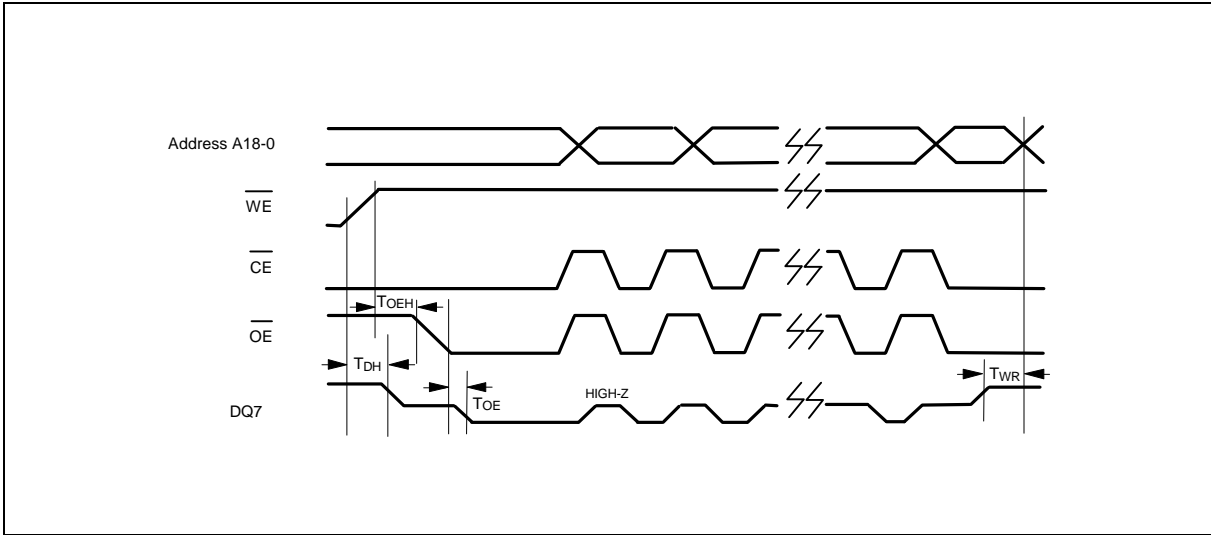


Timing Waveforms, continued

Page Write Cycle Timing Diagram



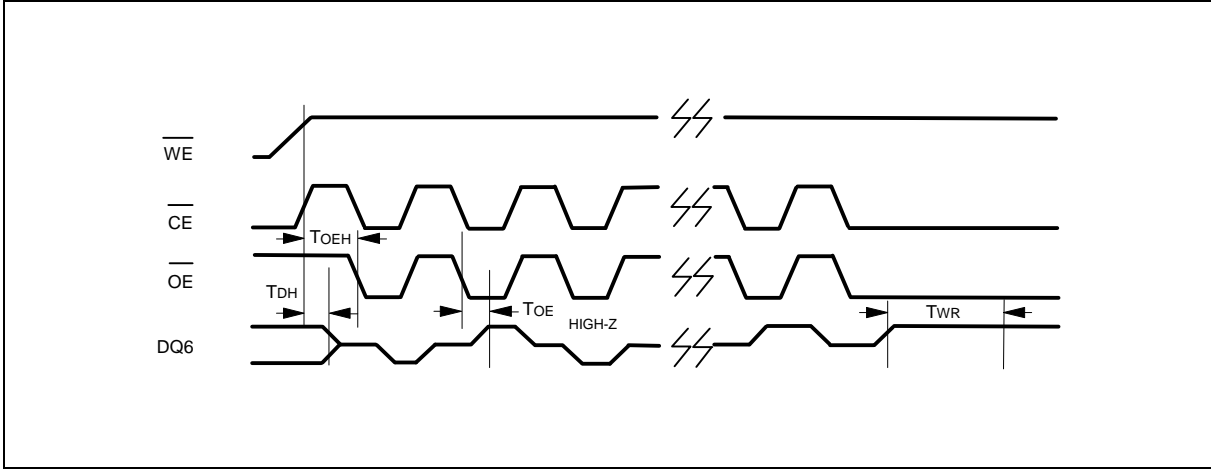
DATA Polling Timing Diagram



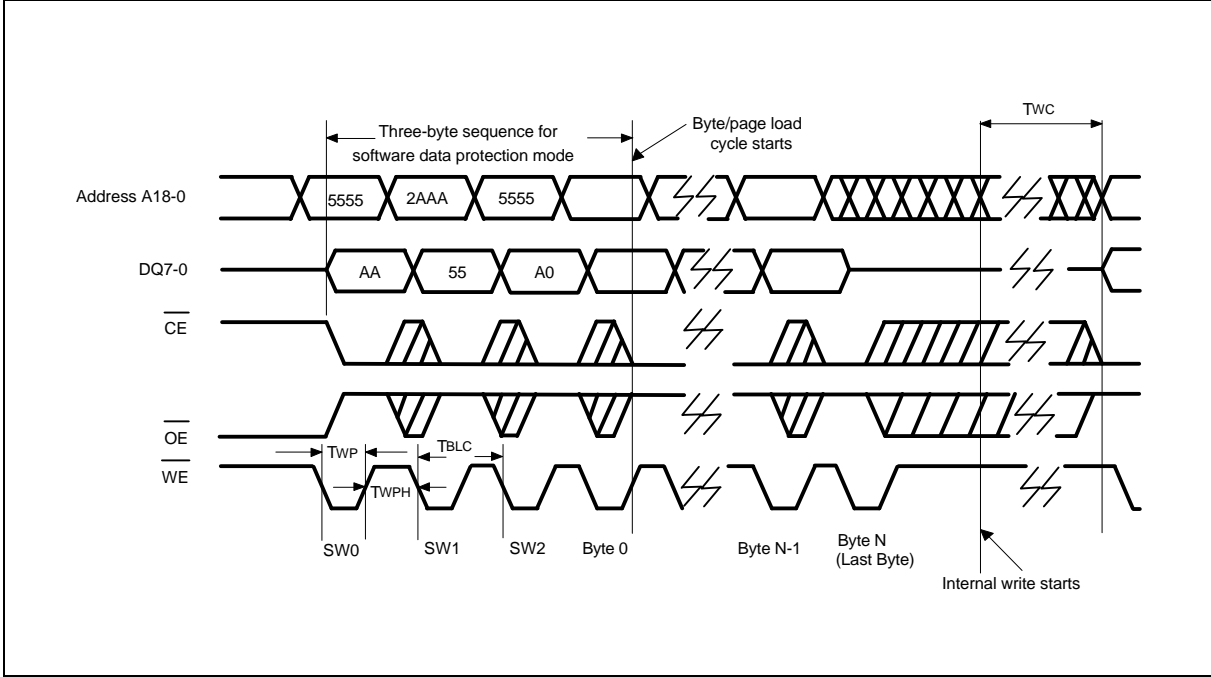


Timing Waveforms, continued

Toggle Bit Timing Diagram



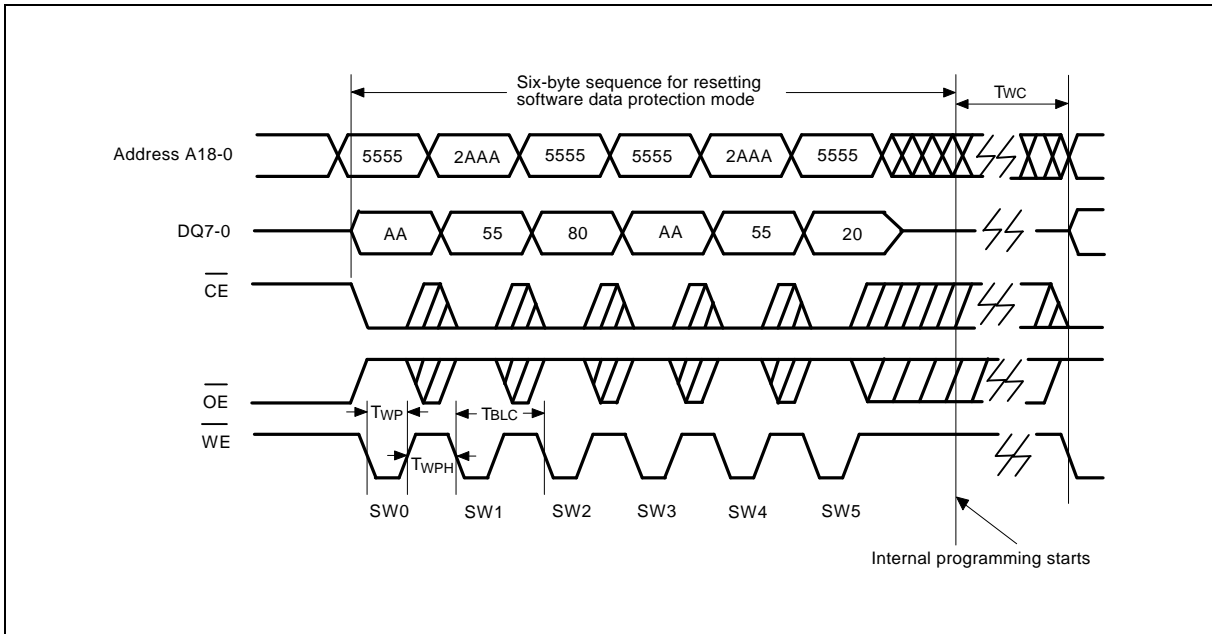
Page Write Timing Diagram Software Data Protection Mode



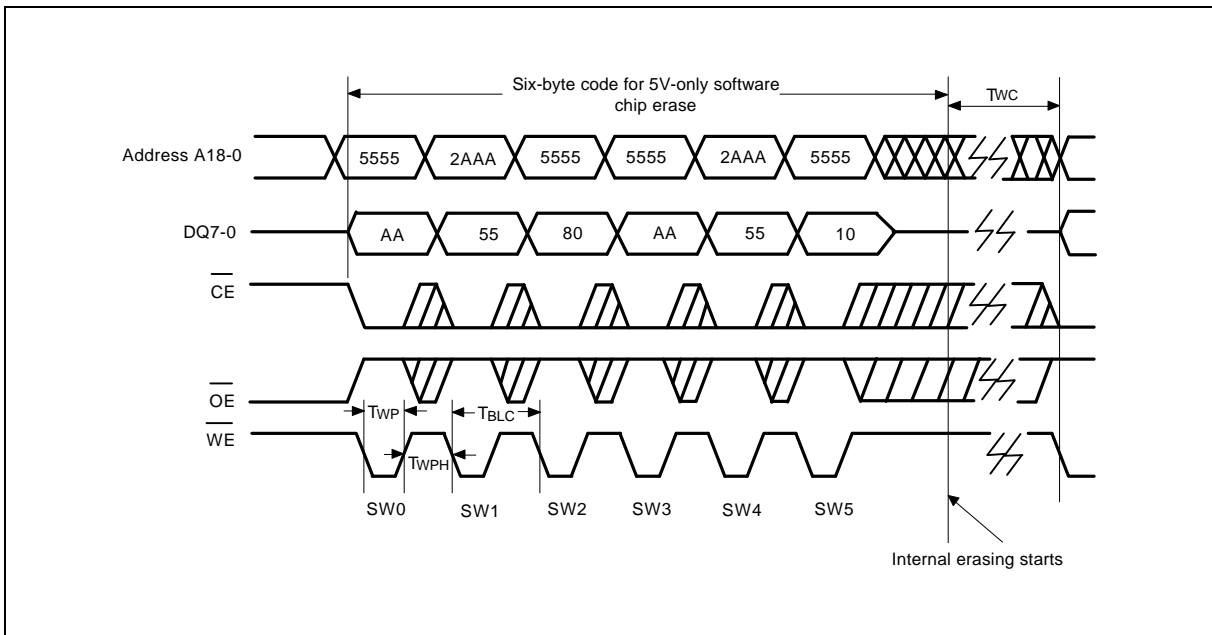


Timing Waveforms, continued

Reset Software Data Protection Timing Diagram



5 Volt-only Software Chip Erase Timing Diagram





ORDERING INFORMATION

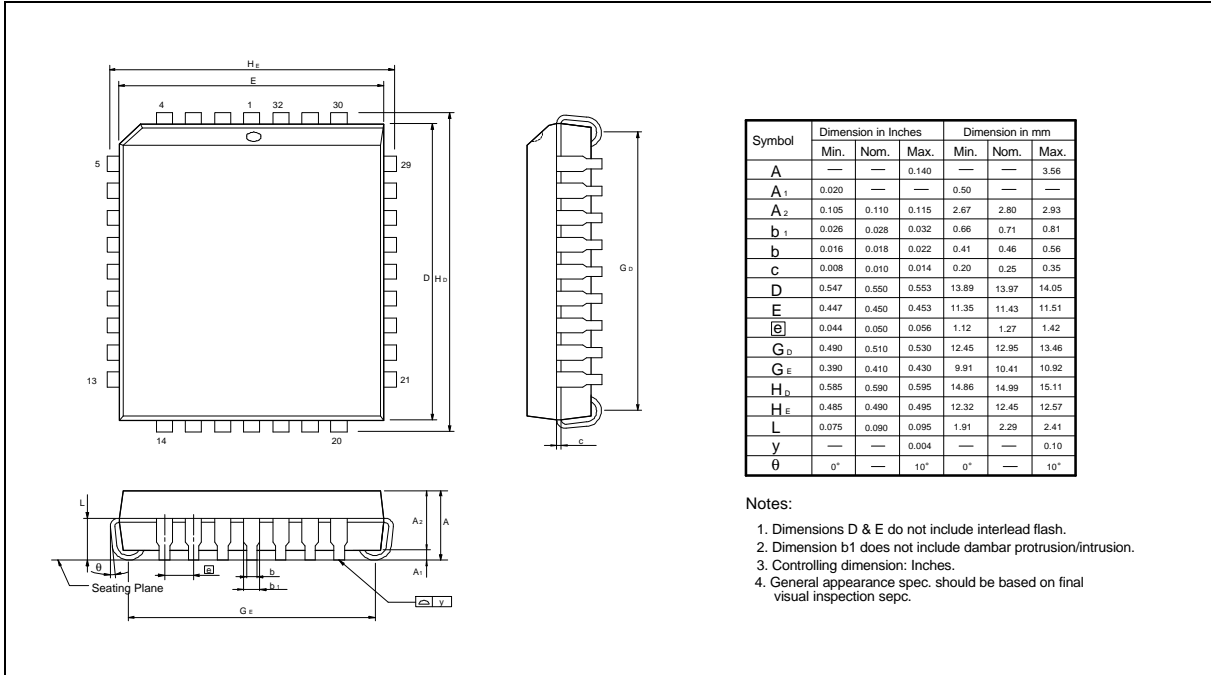
| PART NO. | ACCESS TIME (nS) | POWER SUPPLY CURRENT MAX. (mA) | STANDBY V _{DD} CURRENT MAX. (mA) | PACKAGE | CYCLING |
|--------------|------------------|--------------------------------|---|---------------|---------|
| W29C040T-90 | 90 | 50 | 100 | Type one TSOP | 1K |
| W29C040T-12 | 120 | 50 | 100 | Type one TSOP | 1K |
| W29C040P-90 | 90 | 50 | 100 | 32-pin PLCC | 1K |
| W29C040P-12 | 120 | 50 | 100 | 32-pin PLCC | 1K |
| W29C040T-90B | 90 | 50 | 100 | Type one TSOP | 10K |
| W29C040T-12B | 120 | 50 | 100 | Type one TSOP | 10K |
| W29C040P-90B | 90 | 50 | 100 | 32-pin PLCC | 10K |
| W29C040P-12B | 120 | 50 | 100 | 32-pin PLCC | 10K |

Notes:

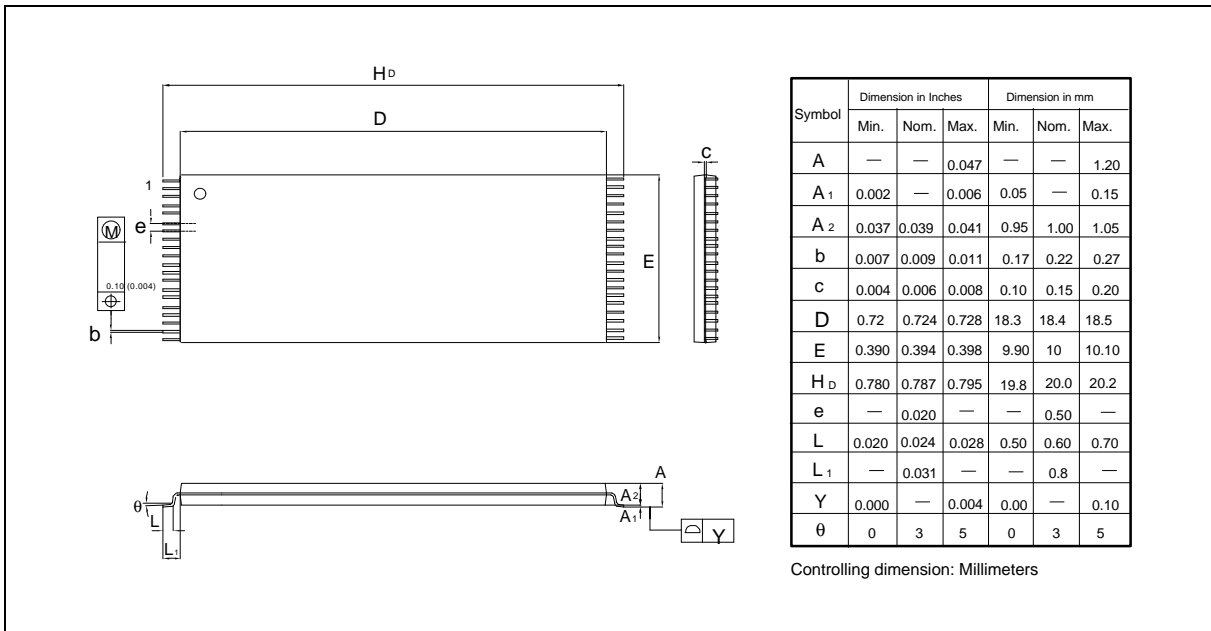
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin PLCC



40-pin TSOP





VERSION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---------|-----------|--------------|---|
| A1 | Apr. 1997 | - | Initial Issued |
| A2 | Nov. 1997 | 4, 8 | Correct the address from 3FFF2 to 7FFF2 |
| | | 9 | Correct the boot block from 8K to 16K |
| | | 15 | Modify page write cycle timing diagram waveform |
| | | 1, 18 | Delete cycling 100K item |
| | | 6 | Add. pause 10 mS |
| | | 7 | Add. pause 50 mS |
| | | 8 | Correct the time from 10 mS to 10 μ S |
| A3 | June 1998 | 4 | Correct power-on delay from 5 mS to 10 mS |
| | | 11 | Correct TPU.WRITE (Typ.) from 5 mS to 10 mS |
| A4 | Oct. 1998 | 20 | Correct 40-pin TSOP package drawing by 32-pin TSOP |
| | | 9 | Correct the address from 3FFFF to 7FFFF |
| A5 | May 1999 | 1, 12, 18 | Modify TACC: 90/120/150 nS \rightarrow 90/120 nS binning |
| | | 1, 2, 18, 19 | Modify package: PDIP/SOP/PLCC/TSOP \rightarrow PLCC/TSOP |



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5796096
<http://www.winbond.com.tw/>
Voice & Fax-on-demand: 886-2-27197006

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.

Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.

Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798

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