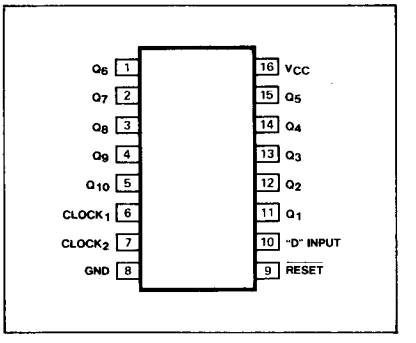
## DESCRIPTION

The 8273, 10-Bit Shift Register is an array of binary elements interconnected to perform the serial-in, parallel-out shift function. This device utilizes a common buffered reset and operates from either a positive or negative edge clock pulse. Clock 1 is triggered by a negative going clock pulse and Clock 2 is triggered by a positive going clock pulse. The unused clock input performs the inhibit function. The circuit configuration is arranged as a single serial input register with ten true parallel outputs.

## PIN CONFIGURATION




## ORDERING CODE (See Section 9 for further Package and Ordering Information)

| PACKAGES | COMMERCIAL RANGES $V_{CC}$=5V±5%; $T_A$=0°C to +75°C | MILITARY RANGES $V_{CC}$=5V±5%; $T_A$=−55°C to +125°C |
|---|---|---|
| Plastic DIP | N8273N | |
| Ceramic DIP | N8273F | S8273F |
| Flatpak | | S8273W |

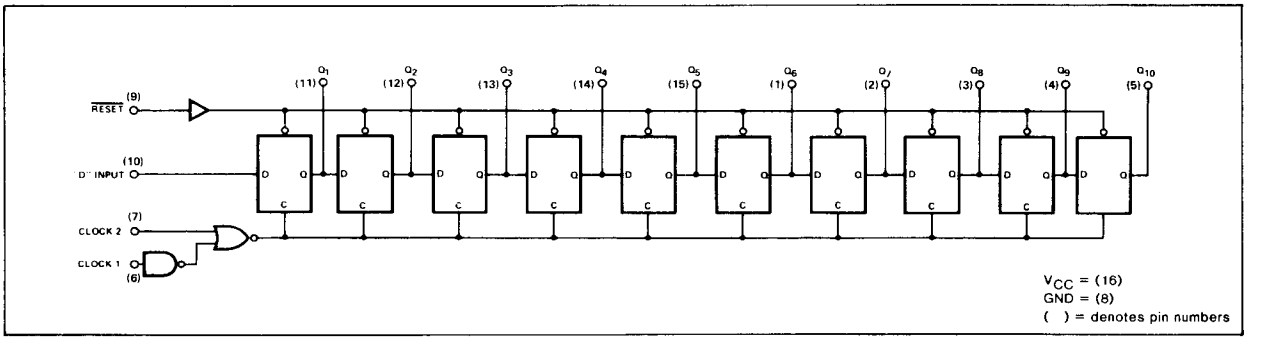
## MODE SELECT—FUNCTION TABLE

| INPUT | RESET | CLOCK 1 | CLOCK 2 | OUTPUTS $Q_n$ |
|---|---|---|---|---|
| H | H | ↓ | L | H |
| L | H | ↓ | L | L |
| H | H | H | ↑ | H |
| L | H | H | ↑ | L |
| H | H | ↓ | H | $Q_{n-1}$ |
| L | H | ↓ | H | $Q_{n-1}$ |
| H | H | L | ↑ | $Q_{n-1}$ |
| L | H | L | ↑ | $Q_{n-1}$ |
| X | L | X | X | L |

NOTE

The unused clock input performs the INHIBIT function.
$\overline{RESET}$ = 0  Q = 0

## LOGIC DIAGRAM






This Material Copyrighted By Its Respective Manufacturer

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE [b]

| PARAMETER | | TEST CONDITIONS | 8273 | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{OH}$ | Output HIGH voltage | $V_{CC}$ = 4.75V, $I_{OH}$ = −500μA | 2.6 | | V |
| $V_{OL}$ | Output LOW voltage | $V_{CC}$ = 4.75V, $I_{OL}$ = 9.6mA | | 0.4 | V |
| $I_{IH}$ | Input HIGH current | $V_{CC}$ = 5.25V, $V_{IN}$ = 4.5V | | 40 | μA |
| $I_{IL}$ | Input LOW current | $V_{CC}$ = 5.25V, $V_{IN}$ = 0.4V | | −1.6 | mA |
| $V_{BD}$ | Input breakdown voltage | $V_{CC}$ = 5.25V, IN = 10mA | 5.5 | | V |
| $I_{OS}$ | Output short circuit current | $V_{CC}$ = 5.25V, $V_{OUT}$ = OV | −20 | −70 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = 5.25V | | 103 | mA |

## AC CHARACTERISTICS: $T_A$ = 25°C (See Section 4 for Waveforms and Conditions)

| PARAMETER | | TEST CONDITIONS | 8273 $C_L$ = 18pF $R_1$ = ∞Ω $R_2$ = 150Ω | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | Figure 1 | 25 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$CP_1$ to output | $CP_2$ = OV, Figure 1 | | 40<br>40 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$CP_2$ to output | $CP_1$ = 4.5V, Figure 1 | | 40<br>40 | ns<br>ns |
| $t_{PHL}$ | Propagation delay<br>Reset to output | Figure 2 | | 50 | ns |

## AC SET-UP REQUIREMENTS: $T_A$ = 25° C (See Section 4 for Waveforms and Conditions)

| PARAMETER | | TEST CONDITIONS | 8273 | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_W$ | $CP_1$ pulse width | Figure 1 | 25 | | ns |
| $t_s$ | Setup time Data to $CP_1$ | Figure 1 | 15 | | ns |
| $t_h$ | Hold time Data to $CP_1$ | Figure 1 | 15 | | ns |
| $t_W$ | $CP_2$ pulse width | Figure 1 | 20 | | ns |
| $t_s$ | Setup time Data to $CP_2$ | Figure 1 | 10 | | ns |
| $t_h$ | Hold time Data to $CP_2$ | Figure 1 | 10 | | ns |



This Material Copyrighted By Its Respective Manufacturer

## AC WAVEFORMS

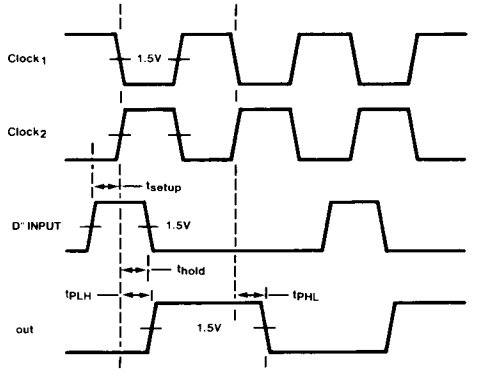



Figure 1

RESET PULSE WIDTH,
RESET TO OUTPUT DELAY AND
RESET TO CLOCK RECOVERY TIME

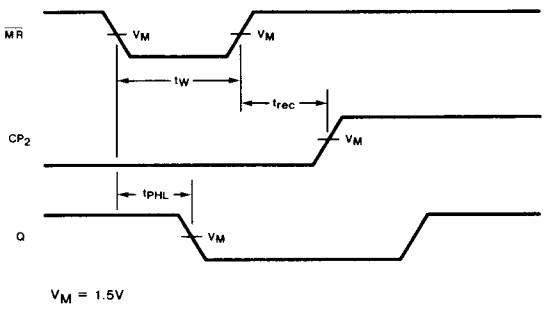



Figure 2



This Material Copyrighted By Its Respective Manufacturer