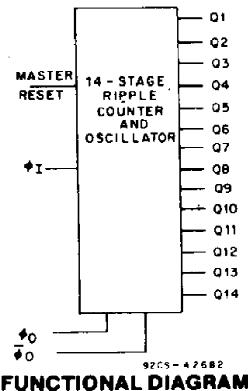


# CD54/74AC7060, CD54/74AC7061 CD54/74ACT7060, CD54/74ACT7061



## 14-Stage Binary Counter with Oscillator

### Type Features:

- On-board oscillator
- Buffered inputs
- Common reset
- Negative-edge clocking
- Typical  $f_{MAX} = 200$  MHz @  $V_{CC} = 5$  V,  $C_L = 50$  pF
- AC/ACT7060 Enabling Reset disables oscillator
- AC/ACT7061 oscillator continues to run when Reset is enabled

The RCA-CD54/74AC7060 and CD54/74AC7061 and the CD54/74ACT7060 CD54/74ACT7061 each consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A Master Reset input is provided which resets the counter to the all-0's state and disables the oscillator in the 7060. In the 7061 the oscillator continues to run when the Master Reset is enabled. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in the binary order on the negative transition of  $\phi I$  (and  $\phi O$ ). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse line permits much slower rise and fall slew rates.

In order to achieve a symmetrical waveform in the oscillator section, the ACT7060 and 7061 input pulse switchpoints are the same as in the AC7060 and 7061 except the MR input in the ACT7060 and 7061 has TTL switching levels.

The CD74AC/ACT7060 and the CD74AC/ACT7061 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to +70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C). The CD54AC/ACT7060 and the CD54-AC/ACT7061, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

### Family Features:

- Exceeds 2-kV ESD protection-MIL-STD-883, Method 3015
- SCR-latchup-resistant CMOS process and circuit design
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- $\pm 24$ -mA output drive current (Q1, Q2, and Q3)
  - Fanout to 15 FAST<sup>\*</sup> ICs
  - Drives 50-ohm transmission lines

<sup>\*</sup>FAST is a registered trademark of Fairchild Semiconductor Corp.

**TRUTH TABLE**

$\phi I$	MR	OUTPUT STATE
	L	No Change
	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)

L = low level (steady state)

X = don't care

# CD54/74AC7060, CD54/74AC7061

# CD54/74ACT7060, CD54/74ACT7061

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE, ( $V_{cc}$ ) .....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{ik}$ (for $V_i < -0.5$ V or $V_i > V_{cc} + 0.5$ V) .....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{ok}$ (for $V_o < -0.5$ V or $V_o > V_{cc} + 0.5$ V) .....	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{cc} + 0.5$ V) .....	$\pm 50$ mA
DC $V_{cc}$ OR GROUND CURRENT ( $I_{cc}$ or $I_{GND}$ ) .....	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES E) .....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES E) .....	Derate Linearly at $8 \text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M) .....	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M) .....	Derate Linearly at $6 \text{ mW}/^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ ) .....	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s max. ....	$+265^\circ\text{C}$
Unit inserted into PC board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only .....	$+300^\circ\text{C}$

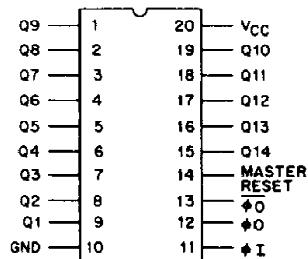
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range)	$V_{cc}$ *		
AC Types	1.5	5.5	
ACT Types	4.5	5.5	V
DC Input or Output Voltage	$V_i, V_o$	0	$V_{cc}$
Operating Temperature	$T_A$	-55	$^\circ\text{C}$
Input Rise and Fall Slew Rate at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	dt/dv†	0	
		50	
		0	ns/V
		20	
		0	
		10	

†Applicable for MR. Schmitt input on  $\phi I$  line permits slower slew rates.

\*Unless otherwise specified, all voltages are referenced to ground.

**TERMINAL ASSIGNMENT**

# CD54/74AC7060, CD54/74AC7061 CD54/74ACT7060, CD54/74ACT7061

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTIC	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS		
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		+25		-40 to +85		-55 to +125				
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V		
			3	2.1	—	2.1	—	2.1	—			
			5.5	3.85	—	3.85	—	3.85	—			
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V		
			3	—	0.9	—	0.9	—	0.9			
			5.5	—	1.65	—	1.65	—	1.65			
Output High Voltage V <sub>OH</sub> All Outputs	V <sub>IH</sub> or V <sub>IL</sub>	-0.05 -0.05 -0.05	1.5 3 4.5	1.4 2.9 4.4	— — —	1.4 2.9 4.4	— — —	1.4 2.9 4.4	— — —	V		
	φ <sub>o</sub> , φ̄ <sub>o</sub> (Pins 12, 13)	V <sub>IH</sub> or V <sub>IL</sub>	-2 -12	3 4.5	2.58 3.94	— —	2.48 3.8	— —	2.4 3.7			
		V <sub>IH</sub> or V <sub>IL</sub>	-4 -24 #*	3 4.5 75 50	2.58 3.94 — —	— — 3.85 —	2.48 3.8 — —	— — — 3.85	2.4 3.7 — —			
Q1, Q2, Q3	V <sub>IH</sub> or V <sub>IL</sub>	-1.3 -8	3 4.5	2.58 3.94	— —	2.48 3.8	— —	2.4 3.7	— —	V		
	φ <sub>o</sub> , φ̄ <sub>o</sub> (Pins 12, 13)	V <sub>IH</sub> or V <sub>IL</sub>	6 12	3 4.5	— —	0.36 0.36	— —	0.44 0.44	— —			
		V <sub>IH</sub> or V <sub>IL</sub>	12 24 #*	3 4.5 75 50	— 0.36 — —	0.36 — — —	— 0.44 1.65 —	— — — —	0.50 0.50 — 1.65			
Q4 thru Q14	V <sub>IH</sub> or V <sub>IL</sub>	4 8	3 4.5	— —	0.36 0.36	— —	0.44 0.44	— —	0.50 0.50	V		
	Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or Gnd		5.5	—	±0.1	—	±1	—			
									±1			
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or Gnd	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-Ω transmission-line-drive capability at +85°C; 75 ohms at +125°C.

**Technical Data**

**CD54/74AC7060, CD54/74AC7061  
CD54/74ACT7060, CD54/74ACT7061**

**STATIC ELECTRICAL CHARACTERISTICS: ACT Series**

CHARACTERISTIC	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS		
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		+25		-40 to +85		-55 to +125				
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage MR Only	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—			
Low-Level Input Voltage MR Only	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8			
Output High Voltage All Outputs	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05    4.5	4.4	—	4.4	—	4.4	—			
Φ <sub>0</sub> , Φ <sub>0</sub> (Pins 12, 13)	V <sub>IH</sub> or V <sub>IL</sub>	-12    4.5	3.94	—	3.8	—	3.7	—				
Q1, Q2, Q3	V <sub>IH</sub> or V <sub>IL</sub>	-24    5.5 #* { -75    5.5 -50    5.5	3.94	—	3.8	—	3.7	—				
Q4 thru Q14	V <sub>IH</sub> or V <sub>IL</sub>	-8    4.5	3.94	—	3.8	—	3.7	—				
Output Low Voltage All Outputs	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05    4.5	—	0.1	—	0.1	—	0.1			
Φ <sub>0</sub> , Φ <sub>0</sub> (Pins 12, 13)	V <sub>IH</sub> or V <sub>IL</sub>	12    4.5	—	0.36	—	0.44	—	0.50				
Q1, Q2, Q3	V <sub>IH</sub> or V <sub>IL</sub>	24    4.5 #* { 75    5.5 50    5.5	—	0.36	—	0.44	—	0.50				
Q4 thru Q14	V <sub>IH</sub> or V <sub>IL</sub>	8    4.5	—	0.36	—	0.44	—	0.50				
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or Gnd	5.5	—	±0.1	—	±1	—	±1	μA		
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or Gnd	0    5.5	—	8	—	80	—	160			
Additional Supply Current per Input Pin, TTL Inputs High Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA		

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\* Test verifies a minimum 50-Ω transmission-line-drive capability at +85°C, 75 ohms at +125°C.

# CD54/74AC7060, CD54/74AC7061 CD54/74ACT7060, CD54/74ACT7061

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTIC	V <sub>cc</sub> (V)	AMBIENT TEMPERATURE—°C				UNITS	
		-40 to +85		-55 to +125			
		MIN.	MAX.	MIN.	MAX.		
Input Pulse Width	tw	1.5	55	—	63	ns	
		3.3*	6.1	—	7		
		5†	4.4	—	5		
Reset Pulse Width	tw	1.5	44	—	50	ns	
		3.3	4.9	—	5.6		
		5	3.5	—	4		
Reset Removal Time	t <sub>REM</sub>	1.5	44	—	50	ns	
		3.3	4.9	—	5.6		
		5	3.5	—	4		
Minimum Input Pulse Frequency	f <sub>MAX</sub>	1.5	9.1	—	8	MHz	
		3.3	81	—	71		
		5	114	—	100		

\*3.3 V: min. is @ 3 V.

†5 V: min. is @ 4.5 V.

SWITCHING CHARACTERISTICS: AC Series, t<sub>l</sub>, t<sub>r</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTIC	V <sub>cc</sub> (V)	AMBIENT TEMPERATURE—°C				UNITS	
		-40 to +85		-55 to +125			
		MIN.	MAX.	MIN.	MAX.		
Propagation Delays: φI to Q1	t <sub>PLH</sub>	1.5	—	230	—	254	
	t <sub>PHL</sub>	3.3*	7.2	25	7	28	
		5†	5.3	18.5	5.1	20.3	
Qn to Qn + 1	t <sub>PLH</sub>	1.5	—	68	—	75	
	t <sub>PHL</sub>	3.3	2.2	7.6	2.1	8.4	
		5	1.5	5.5	1.5	6	
MR to Qn	t <sub>PLH</sub>	1.5	—	262	—	288	
	t <sub>PHL</sub>	3.3	8.3	29.3	8.1	32.2	
		5	6	21	5.8	23	
Power Dissipation Capacitance	C <sub>PD\$</sub>	—	—	114 Typ.	—	114 Typ.	
Input Capacitance	C <sub>I</sub>	—	—	—	10	—	
				—	10	—	

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V†5 V: min. is @ 5.5 V  
max. is @ 4.5 V§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.

$$P_D = C_{PD} V_{cc}^2 f_I + \sum (C_L V_{cc}^2 f_O) \text{ where } f_I = \text{input frequency}$$

f<sub>O</sub> = output frequencyC<sub>L</sub> = output load capacitanceV<sub>cc</sub> = supply voltage.

## PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTIC	V <sub>cc</sub> (V)	AMBIENT TEMPERATURE—°C				UNITS	
		-40 to +85		-55 to +125			
		MIN.	MAX.	MIN.	MAX.		
Input Pulse Width	tw	5*	4.4	—	5	ns	
		5	3.5	—	4		
		5	4.4	—	5		
Reset Pulse Width	tw	5	3.5	—	4	—	
Reset Removal Time	t <sub>REM</sub>	5	4.4	—	5	—	
Minimum Input Pulse Frequency	f <sub>MAX</sub>	5	114	—	100	—	

\*Min. is @ 4.5 V.

# CD54/74AC7060, CD54/74AC7061

# CD54/74ACT7060, CD54/74ACT7061

SWITCHING CHARACTERISTICS: ACT Series,  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTIC	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE—°C				UNITS	
		-40 to +85		-55 to +125			
		MIN.	MAX.	MIN.	MAX.		
Propagation Delays: $\phi_I$ to Q1	$t_{PLH}$	5*	5.3	18.5	5.1	20.3	ns
	$t_{PHL}$		1.5	5.5	1.5	6	
	$t_{PLH}$		6.3	22.1	6.1	24.3	
Qn to Qn + 1	$t_{PLH}$	5	—	—	—	—	—
MR to Qn	$t_{PLH}$	5	—	—	—	—	—
Power Dissipation Capacitance	$C_{PD\$}$	—	114 Typ.	114 Typ.	—	—	—
Input Capacitance	$C_I$	—	—	10	—	10	pF

\*Min. is @ 5.5 V  
max. is @ 4.5 V

\$ $C_{PD}$  is used to determine the dynamic power consumption, per flip-flop.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency}$$

$f_o$  = output frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.

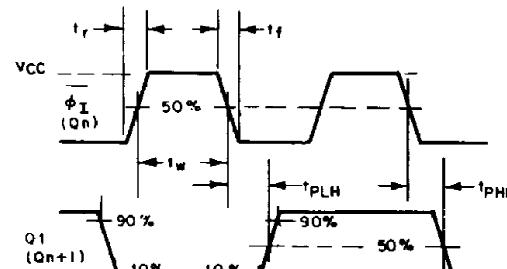
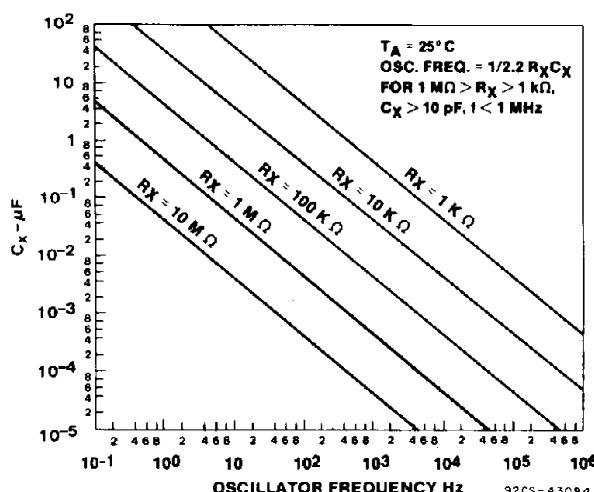
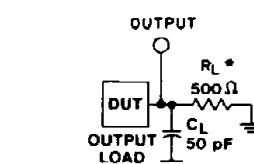
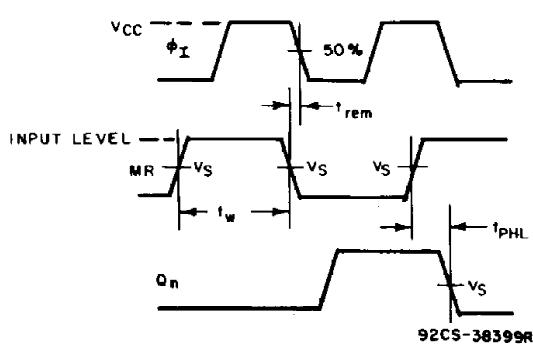
Fig. 1 - Frequency on on-board oscillator as a function of  $C_x$  and  $R_x$ .

Fig. 2 - Input pulse pre-requisite times and propagation delays for both AC and ACT types.



\*FOR AC SERIES ONLY: WHEN  
 $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

Fig. 3 - Master Reset pre-requisite and propagation delays.

	CD54/74AC	CD54/74ACT
MR Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_s$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_s$	0.5 $V_{CC}$	0.5 $V_{CC}$