DUAL FORWARD-CONDUCTING P-GATE THYRISTORS PROGRAMMABLE OVERVOLTAGE PROTECTORS

TISP61521 SLIC Protector

Overvoltage Protection for High Voltage Negative Rail Ringing SLICs

Dual Voltage-Programmable Protectors
- **Supports Battery Voltages Down to -150 V**
- **Low 3 mA max. Gate Triggering Current**
- **High 150 mA min. Holding Current**

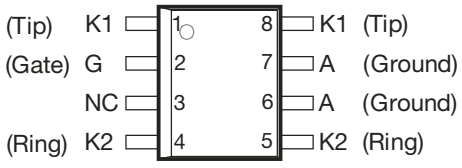
Rated for International Surge Wave Shapes

Voltage Waveshape	Standard	I_{TSP} A
2/10	GR-1089-CORE	170
1.2/50	ITU-T K.22 VDE 0878	50
1.2/50	IEC 61000-4-5	100
10/160	FCC Part 68 Type A	50
0.5/700	I3124	40
10/700	ITU-T K.20, VDE 0433 IEC 61000-4-5	40
9/720	FCC Part 68 Type B	40
10/560	FCC Part 68 Type A	35
10/1000	GR-1089-CORE	30

Functional Replacements for

Device Type	Package Type	Functional Replacement
LCP1511D, LCP1521	8-pin Small-Outline	TISP61521DR-S

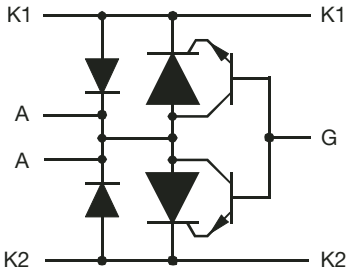
D Package (Top View)



MD6XANB

NC - No internal connection
Terminal typical application names shown in parenthesis

Device Symbol



Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage, V_{GG}, applied to the G terminal. SD6XAEB

..... UL Recognized Components

How To Order

Device	Package	Carrier	Order As
TISP61521	D (8-pin Small-Outline)	Embossed Tape Reeled	TISP61521DR-S

Description

The TISP61521 is a dual forward-conducting buffered p-gate overvoltage protector. It is designed to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The TISP61521 limits voltages that exceed the SLIC supply rail voltage. The TISP61521 parameters are specified to allow equipment compliance with Bellcore GR-1089-CORE, Issue 1 and ITU-T recommendation K.20.

WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

APRIL 2001 REVISED JULY 2008
*RoHS Directive 2002/95/EC Jan. 27, 2003 including Annex.

Description (continued)

The SLIC line driver section is typically powered from 0 V (ground) and a negative voltage in the region of -20 V to -150 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. The protection voltage will then track the negative supply voltage and the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector will switch into a low voltage on-state condition. As the overvoltage subsides, the high holding current of TISP61521 crowbar helps prevent d.c. latchup.

These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and in normal system operation they are virtually transparent. The TISP61521 buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction. The TISP61521 is available in an 8-pin plastic small-outline surface mount package.

Absolute Maximum Ratings, T_J = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, V_{GK} = 0, -40 °C ≤ T_J ≤ 85 °C (see Note 1)	V_{DRM}	-175	V
Repetitive peak gate-cathode voltage, V_{KA} = 0, -40 °C ≤ T_J ≤ 85 °C (see Note 1)	V_{GKRM}	-162	V
Non-repetitive peak on-state pulse current (see Note 2)			
2/10 µs (GR-1089-CORE, 2/10 µs voltage waveshape)		170	
1/20 µs (K.22, VDE0878, 1.2/50 voltage waveshape)		50	
8/20 µs (IEC 61000-4-5, combination wave generator, 1.2/50 voltage, 8/20 current)		100	
10/160 µs (FCC Part 68, 10/160 µs voltage waveshape)		50	
0.2/310 µs (I3124, 0.5/700 µs voltage waveshape)	I_{TSP}	40	A
5/310 µs (VDE 0433, 10/700 µs voltage waveshape)		40	
5/310 µs (ITU-T K.20/21, K.44 10/700 µs voltage wave shape)		40	
5/320 µs (FCC Part 68, 9/720 µs voltage waveshape)		40	
10/560 µs (FCC Part 68, 10/560 µs voltage waveshape)		35	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage waveshape)		30	
Non-repetitive peak on-state current, 50 Hz (see Notes 2 and 3)			
0.01 s	I_{TSM}	15	A
1 s		5	
Non-repetitive peak gate current, 10 ms half-sine wave, cathodes commoned (see Notes 1 and 2)	I_{GSM}	+2	A
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. These voltage ratings are set by the -150 V maximum supply voltage plus the 12 V diode overshoot (V_{GKRM}) and the 25 V SCR overshoot (V_{DRM}).
2. Initially, the protector must be in thermal equilibrium. The surge may be repeated after the device returns to its initial conditions. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case, the Ground terminal current will be twice the rated current value of an individual terminal pair).
3. Values for V_{GG} = -48 V. For values at other voltages, see Figure 2.

Recommended Operating Conditions

Component		Min	Typ	Max	Unit
C1	Gate decoupling capacitor	100	220		nF
R_S	series resistor for GR-1089-CORE, 2/10, 10/360 and 10/1000 first-level surge survival	25			Ω
	series resistor for GR-1089-CORE, 2/10, 10/360 and 10/1000 first-level and 2/10 second-level surge survival	40			Ω
	series resistor for K.20, K.21 and K.45 coordination with a 400 V primary protector	10			Ω
	series resistor for K.44 4 kV 10/700 surge survival	60			Ω
	series resistor for FCC Part 68 Type A 10/160 and 10/560 surge survival	20			Ω
	series resistor for FCC Part 68 Type B 9/720 surge survival	0			Ω
	series resistor for VDE 0433 2 kV 10/700 surge survival	10			Ω
	series resistor for VDE 0878 2 kV 1.2/50 surge survival	0			Ω
	series resistor for IEC 6100-4-5 4 kV, 10/700, class 5, long distance balanced circuits surge survival with a 400 V primary protector	10			Ω
	series resistor for IEC 6100-4-5 1.2/50-8/20 combination generator, classes 0 to 5 (500 V to 4 kV maximum), short distance balanced circuits surge survival.	0			Ω

Electrical Characteristics, T_J = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_D	Off-state current	$V_D = V_{DRM}$, V_{GK} = 0	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
$V_{GK(BO)}$	Gate-cathode impulse breakover voltage	V_{GG} = -48 V, C_G = 220 nF 10/700, I_{TM} = -30 A, R_S = 10 Ω 1.2/50, I_{TM} = -30 A, R_S = 10 Ω 2/10, I_{TM} = -38 A, R_S = 62 Ω,				7 10 25	V
V_F	Forward voltage	I_F = 5 A, t_w = 500 μs				2	V
V_{FRM}	Peak forward recovery voltage	10/700, I_F = 30 A, R_S = 10 Ω 1.2/50, I_F = 30 A, R_S = 10 Ω 2/10, I_F = 38 A, R_S = 62 Ω,				5 7 12	V
I_H	Holding current	I_T = -1 A, di/dt = 1A/ms, V_{GG} = -100 V		-150			mA
I_{GKS}	Gate reverse current	$V_{GG} = V_{GK} = V_{GKRM}$, V_{KA} = 0	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
I_{GT}	Gate trigger current	I_T = -3 A, $t_{p(g)} \geq$ 20 μs, V_{GG} = -100 V				3.0	mA
V_{GT}	Gate-cathode trigger voltage	I_T = -3 A, $t_{p(g)} \geq$ 20 μs, V_{GG} = -100 V				2.0	V
C_{KA}	Cathode-anode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 4)	V_D = -3 V			100	pF
			V_D = -48 V			50	pF

NOTE 4: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

APRIL 2001 REVISED JULY 2008

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	T_A = 25 °C, EIA/JESD51-3 PCB, EIA/JESD51-2 environment, P_{TOT} = 1.7 W			170	°C/W

Parameter Measurement Information

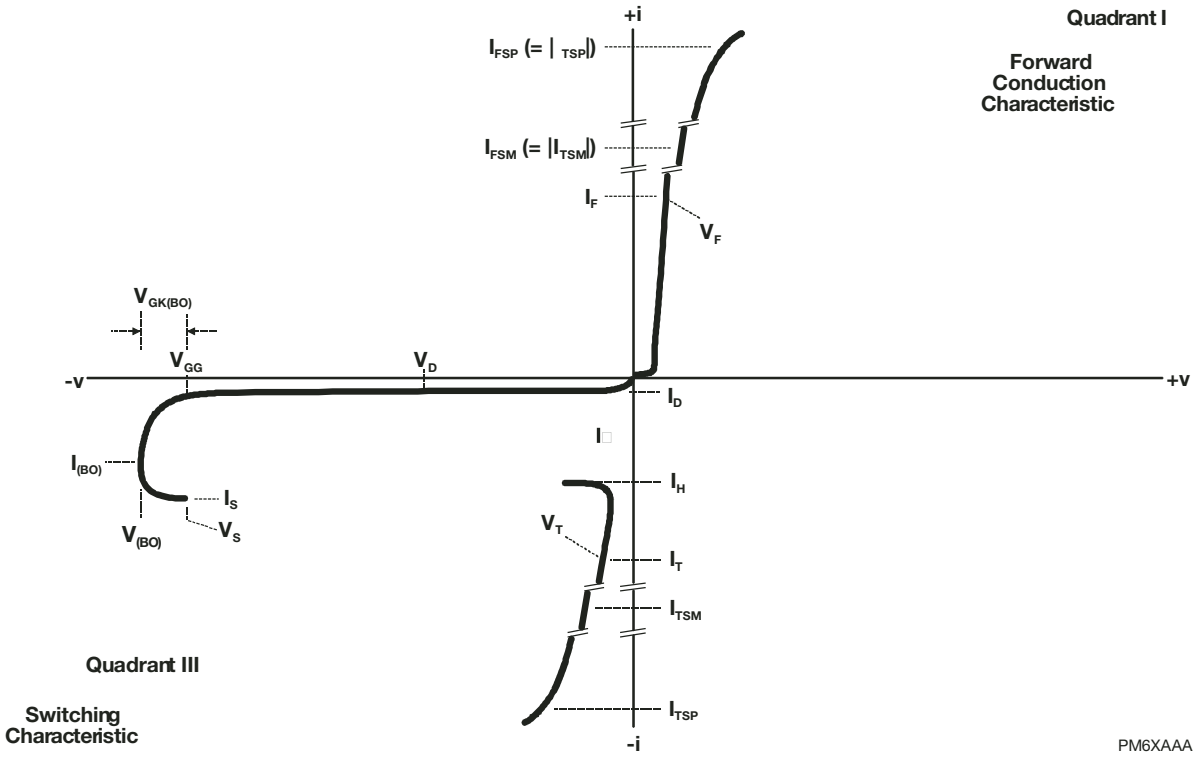


Figure 1. Voltage-Current Characteristic
Unless Otherwise Noted, All Voltages are Referenced to the Anode

Thermal Information

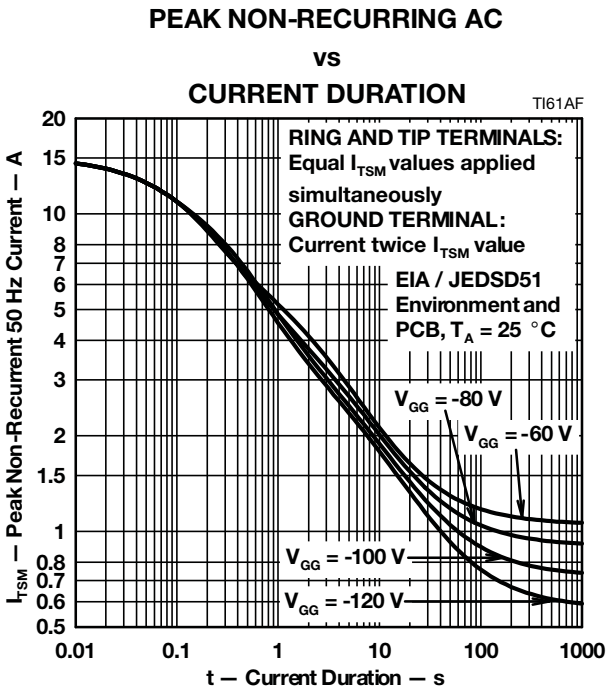


Figure 2. Non-Repetitive Peak On-State Current against Duration

APPLICATIONS INFORMATION

Gated Protectors

This section covers three topics. First, it is explained why gated protectors are needed. Second, the voltage limiting action of the protector is described. Third, an example application circuit is described.

Purpose of Gated Protectors

Fixed voltage thyristor overvoltage protectors have been used since the early 1980s to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. As the SLIC was usually powered from a fixed voltage negative supply rail, the limiting voltage of the protector could also be a fixed value. The TISP1072F3 is a typical example of a fixed voltage SLIC protector.

SLICs have become more sophisticated. To minimize power consumption, some designs automatically adjust the driver supply voltage to a value that is just sufficient to drive the required line current. For short lines, the supply voltage would be set low, but for long lines, a higher supply voltage would be generated to drive sufficient line current. The optimum protection for this type of SLIC would be given by a protection voltage which tracks the SLIC supply voltage. This can be achieved by connecting the protection thyristor gate to the SLIC V_{BATH} supply, Figure 3. This gated (programmable) protection arrangement minimizes the voltage stress on the SLIC, no matter what value of supply voltage.

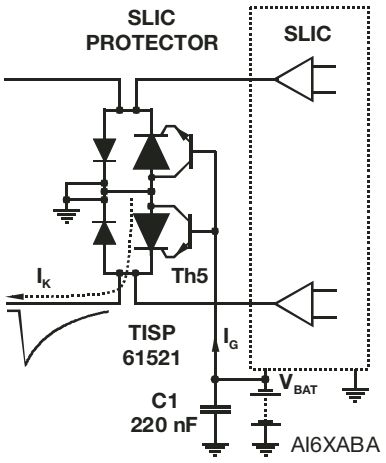


Figure 3. Negative Overvoltage Condition

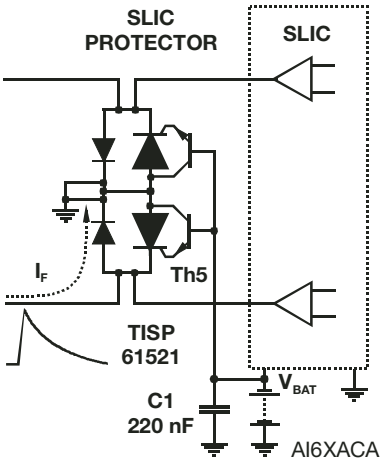


Figure 4. Positive Overvoltage Condition

Operation of Gated Protectors

Figure 3 and Figure 4 show how the TISP61521 limits negative and positive overvoltages. Positive overvoltages (Figure 4) are clipped by the antiparallel diode of Th5 and the resulting current is diverted to ground. Negative overvoltages (Figure 3) are initially clipped close to the SLIC negative supply rail value (V_{BATH}). If sufficient current is available from the overvoltage, then Th5 will switch into a low voltage on-state condition. As the overvoltage subsides, the high holding current of Th5 prevents d.c. latchup. The protection voltage will be the sum of the gate supply (V_{BATH}) and the peak gate-cathode voltage ($V_{GK(BO)}$). The protection voltage will be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse, the gate current (I_G) is the same as the cathode current (I_K). Rates of 70 A/μs can cause inductive voltages of 0.7 V in 2.5 cm of printed wiring track. To minimize this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimized. Inductive voltages in the protector cathode wiring will also increase the protection voltage. These voltages can be minimized by routing the SLIC connection through the protector as shown in Figure 6.

Figure 5, which has a 10 A/μs rate of impulse current rise, shows a positive gate charge (Q_{GS}) of about 0.1 μC. With the 0.1 μF gate decoupling capacitor used, the increase in gate supply is about 1 V (= Q_{GS}/C1). This change is just visible on the -72 V gate voltage, V_{BATH}. But the voltage increase does not directly add to the protection voltage, as the supply voltage change reaches a maximum at 0.4 μs, when the gate current reverses polarity, and the protection voltage peaks earlier at 0.3 μs. In Figure 5, the peak clamping voltage ($V_{(BO)}$) is -77.5 V, an increase of 5.5 V on the nominal gate supply voltage. This 5.5 V increase is the sum of the supply rail increase at that time, (0.5 V), and the protection circuit's cathode diode to supply rail breakover voltage (5 V). In practice, use of the recommended 220 nF gate decoupling capacitor would give a supply rail increase of about 0.3 V and a $V_{(BO)}$ value of about -77.3 V.

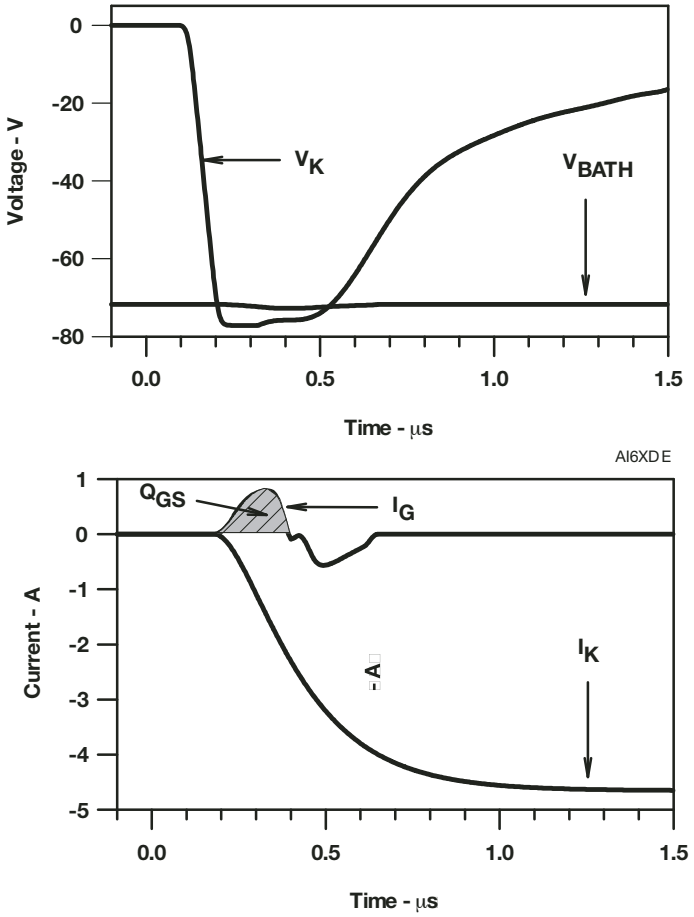


Figure 5. Protector Fast Impulse Clamping and Switching Waveforms

Application Circuit

Figure 6 shows a typical TISP61521 SLIC card protection circuit. The incoming line conductors, Ring (R) and Tip (T), connect to the relay matrix via the series overcurrent protection. Fusible resistors, fuses and positive temperature coefficient (PTC) resistors can be used for overcurrent protection. Resistors will reduce the prospective current from the surge generator for both the TISP61521 and the ring/test protector. The TISP7xxxF3 protector has the same protection voltage for any terminal pair. This protector is used when the ring generator configuration may be ground or battery-backed. For dedicated ground-backed ringing generators, the TISP3xxxF3 gives better protection as its inter-conductor protection voltage is twice the conductor to ground value.

Relay contacts 3a and 3b connect the line conductors to the SLIC via the TISP61521 protector. The protector gate reference voltage comes from the SLIC negative supply (V_{BATH}). A 220 nF gate capacitor sources the high gate current pulses caused by fast rising impulses.

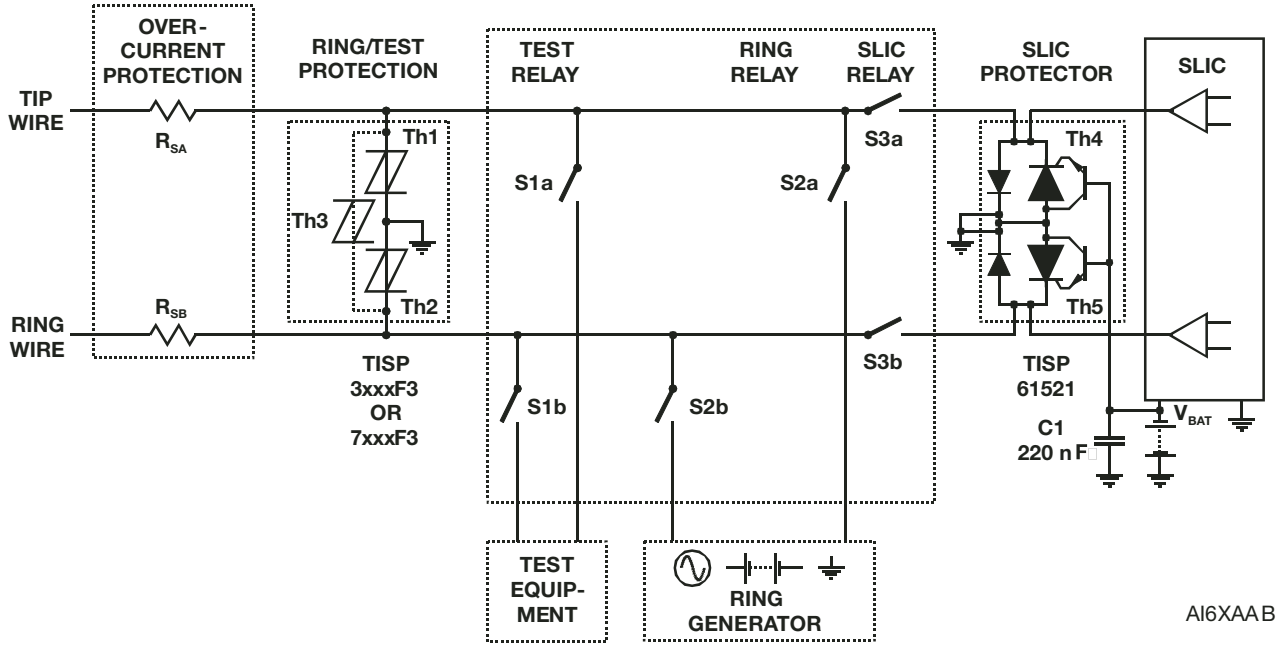


Figure 6. Typical Application Circuit

MECHANICAL DATA

Device Symbolization Code

Devices will be coded as follows:

Device	Symbolization Code
TISP61521DR-S	61521

APRIL 2001 REVISED JULY 2008