

**PERIPHERAL DRIVERS FOR
HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS**

performance

- Characterized for Use to 300 mA
- No Output Latch-Up at 15 V (After Conducting 150 mA)
- Very-High-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- P-N Junctions Protected by Silicon Nitride
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 75430

DEVICE	LOGIC OF	
	COMPLETE CIRCUIT	PACKAGES
SN75430	Positive-AND [†]	J, N
SN75431	Positive-AND	JG, P
SN75432	Positive-NAND	JG, P
SN75433	Positive-OR	JG, P
SN75434	Positive-NOR	JG, P

[†]With output transistor base connected externally to output of gate.

description

Series 75430 dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. Diode-clamped inputs simplify circuit design. They are mechanically interchangeable with the popular Series 75450B, Series 75460, and Series 75470 peripheral drivers. Typical applications include very-high-speed logic buffers, line drivers, MOS drivers, memory drivers, and power drivers. Series 75430 drivers are characterized for operation from 0°C to 70°C.

The SN75430 is a unique general-purpose device featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. This device offers the system designer the flexibility of tailoring the circuit to the application.

The SN75431, SN75432, SN75433, and SN75434 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

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SERIES 75430

DUAL PERIPHERAL DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN75430	SN75431 SN75432 SN75433 SN75434	UNIT	
Supply voltage, V_{CC} (see Note 1)	7	7	V	
Input voltage	5.5	5.5	V	
Interemitter voltage (see Note 2)	5.5	5.5	V	
V_{CC} -to-substrate voltage	15		V	
Collector-to-substrate voltage	15		V	
Collector-base voltage	15		V	
Collector-emitter voltage (see Note 3)	15		V	
Emitter-base voltage	5		V	
Off-state output voltage		15	V	
Continuous collector or output current (see Note 4)	400	400	mA	
Peak collector or output current ($t_W < 10$ ms, duty cycle $\leq 50\%$, see Note 4)	500	500	mA	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	J package	1025	mW	
	JG package	825		
	N package	1150		
	P package	1000		
Operating free-air temperature range	0 to 70	0 to 70	°C	
Storage temperature range	-65 to 150	-65 to 150	°C	
Lead temperature 1/16 inch from case for 60 seconds	J or JG package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	°C

- NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
 2. This is the voltage between two emitters of a multiple-emitter transistor.
 3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω .
 4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
 5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 11. In the J and JG packages, SN75430 through SN75434 chips are glass-mounted.

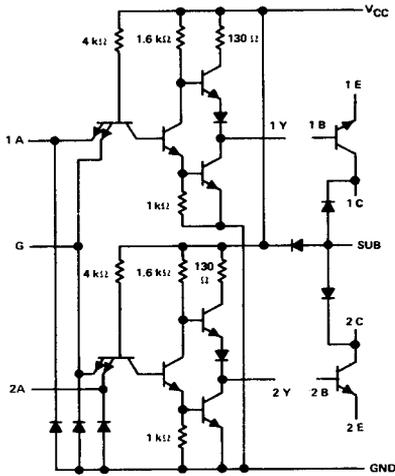
recommended operating conditions (see Note 6)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature, T_A	0		70	°C

NOTE 6: For the SN75430 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

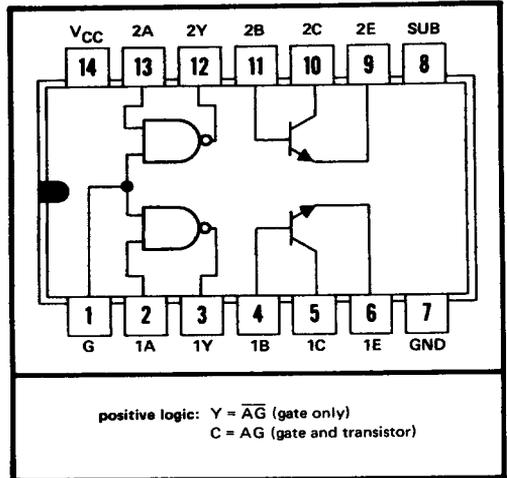
TYPE SN75430 DUAL PERIPHERAL POSITIVE-AND DRIVER

schematic



Resistor values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER		TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = 4.75\text{ V}$, $I_I = -12\text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$	2.4	3.3		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $I_{OL} = 16\text{ mA}$		0.22	0.4	V
I_I	Input current at maximum input voltage	input A			1	mA
		input G	$V_{CC} = 5.25\text{ V}$, $V_I = 5.5\text{ V}$		2	
I_{IH}	High-level input current	input A	$V_{CC} = 5.25\text{ V}$, $V_I = 2.4\text{ V}$		40	μA
		input G			80	
I_{IL}	Low-level input current	input A	$V_{CC} = 5.25\text{ V}$, $V_I = 0.4\text{ V}$		-1.6	mA
		input G			-3.2	
I_{OS}	Short-circuit output current [§]	$V_{CC} = 5.25\text{ V}$	-18		-55	mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.25\text{ V}$, $V_I = 0$		2	4	mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.25\text{ V}$, $V_I = 5\text{ V}$		6	11	mA

[‡]All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[§]Not more than one output should be shorted at a time.

TYPE SN75430

DUAL PERIPHERAL POSITIVE-AND DRIVER

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V(BR)CBO	Collector-Base Breakdown Voltage	I _C = 100 μA, I _E = 0		15			V
V(BR)CER	Collector-Emitter Breakdown Voltage	I _C = 100 μA, R _{BE} = 500 Ω		15			V
V(BR)EBO	Emitter-Base Breakdown Voltage	I _E = 100 μA, I _C = 0		5			V
h _{FE}	Static Forward Current Transfer Ratio	V _{CE} = 3 V, I _C = 100 mA, T _A = 25°C	See Note 7	25			
		V _{CE} = 3 V, I _C = 300 mA, T _A = 25°C		30			
		V _{CE} = 3 V, I _C = 100 mA, T _A = 0°C		20			
		V _{CE} = 3 V, I _C = 300 mA, T _A = 0°C		25			
V _{BE}	Base-Emitter Voltage	I _B = 10 mA, I _C = 100 mA	See Note 7	0.85		1	V
		I _B = 30 mA, I _C = 300 mA		1.05		1.2	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	I _B = 10 mA, I _C = 100 mA	See Note 7	0.25		0.4	V
		I _B = 30 mA, I _C = 300 mA		0.5		0.7	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	1	C _L = 15 pF, R _L = 400 Ω	9	20	ns	ns
t _{PHL}						

output transistors

PARAMETER	TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t _d	2	I _C = 100 mA, I _{B(1)} = 20 mA, I _{B(2)} = -40 mA, V _{BE(off)} = -1 V, C _L = 15 pF, R _L = 50 Ω	7	14	ns	
t _r			10	19	ns	
t _s			7	15	ns	
t _f			6	15	ns	

‡ Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

gates and transistors combined

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	3	I _C ≈ 100 mA, C _L = 15 pF, R _L = 50 Ω	15	26	ns	
t _{PHL}			15	26	ns	
t _{TLH}			7	12	ns	
t _{THL}			9	15	ns	
V _{OH}	4	V _S = 15 V, I _C ≈ 150 mA, R _{BE} = 500 Ω	V _S -10			mV