Feb. 1985

Features

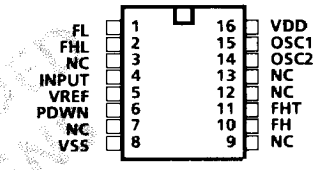
- Provides DTMF high and low group filtering
- Hard-limiting on filter outputs
- 6 pole bandpass high and low group filters
- 40 dB (typ) Intergroup attenuation
- Dial tone suppression
- +5 to +12V single supply operation
- Logical powerdown
- Uses inexpensive 3.58 MHz crystal
- Wide dynamic range 30dB

Applications

In DTMF Receivers For

- End-to-end signalling
- Control systems
- PABX
- Central Office
- Mobile Radio
- Key systems
- Tone to pulse converters

Pin Connections



Ordering Information -40°C to +85°C

MT8865XC	16 Pin Cerdip CIP
MT8865XE	16 Pin Plastic DIP

NOT RECOMMENDED FOR NEW DESIGN

Description

The Mitel MT8865 contains both the high group and low group filtering and comparator functions required to implement a Dual Tone Multi Frequency tone receiver using a Mitel DTMF Digital Detector (i.e., Mitel MT8860). Switched capacitor techniques are used to implement the filters and the device is fabricated using Mitel's double poly ISO²-CMOS high density technology. The filter clocks are derived from an on-chip oscillator requiring only a low cost TV crystal as external components. The MT8865 offers single supply operation over a wide supply voltage range and incorporates a logical power down facility.

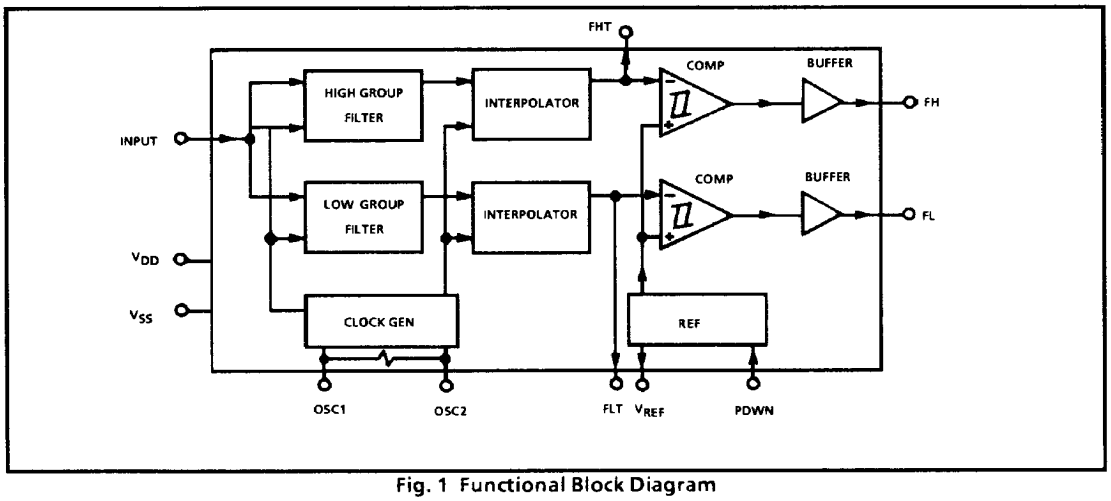


Fig. 1 Functional Block Diagram

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Absolute Maximum Ratings*

	Parameter		Symbol	Min	Max	Units
1	V_{DD} - V_{SS}				15	V
2	Voltage on any pin except OS1, OSC2			$V_{EE}-0.3$	$V_{DD}+0.3$	V
3	Max. Current at any pin		I_I		10	mA
4	Storage Temperature	C Package E Package	T_{STG} T_{STG}	−65 −65	+150 +125	°C °C
5	Power Dissipation	C Package① E Package②	P_D P_D		850 400	mW mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
①Derate above 75 °C at 16 mW / °C. All leads soldered to board.
②Derate above 25 °C at 6.3 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1		DC Power Supply Voltage	V_{DD}	4.75		13	V	
2		Operating Temperature	T_O	−40		+85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}), $T_A=25°C$, $f_c=3.579545$ MHz unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Operating Supply Voltage	V_{DD} V_{DD}	4.75		 13	V V	V_{DD} = 5V V_{DD} = 12V
2	SUPPLY	Operating Supply Current	I_{DD} I_{DD}		1.2 5	3 10	mA mA	V_{DD} = 5V, PDWN = V_{SS} V_{DD} = 12V, PDWN = V_{SS}
3	SUPPLY	Standby Supply Current	I_{DDS} I_{DDS}		70 300	100 500	µA µA	V_{DD} = 5V, PDWN = V_{DD} V_{DD} = 12V, PDWN = V_{DD}
4	SUPPLY	Operating Power Consumption Fig. 5(c)	P_O P_O		6 60		mW mW	V_{DD} = 5V, PDWN = V_{SS} V_{DD} = 12V, PDWN = V_{SS}
5	SUPPLY	Standby Power Consumption C = 15 pF	P_S P_S		0.5 1.5		mW mW	V_{DD} = 5V, PDWN = V_{DD} V_{DD} = 12V, PDWN = V_{DD}
6	INPUTS	Low Level Input Voltage PDWN & OSC1	V_{IL} V_{IL}			1.5 3.5	V V	V_{DD} = 5V V_{DD} = 12V
7	INPUTS	High Level Input Voltage PDWN & OSC1	V_{IH} V_{IH}	3.5 8.5			V V	V_{DD} = 5V V_{DD} = 12V
8	INPUTS	Pull Down Sink Current PDWN	I_{IH} I_{IH}		3 12	6 24	µA µA	V_{DD} = 5V V_{DD} = 12V
9	INPUTS	Input Current OSC1	I_I I_I		±2.5 ±6		µA µA	V_{DD} = 5V V_{DD} = 12V
10	OUTPUTS	Low Level Output Voltage FL, FH, OSC2	V_{OL} V_{OL}			0.1 0.1	V V	V_{DD} = 5V, No Load V_{DD} = 12V, No Load
11	OUTPUTS	High Level Output Voltage FL, FH, OSC2	V_{OH} V_{OH}	4.9 11.9			V V	V_{DD} = 5V, No Load V_{DD} = 12V, No Load
12	OUTPUTS	Ouput Drive Current, FL, FH N Channel Sink	I_{OL} I_{OL}	0.2 0.5			mA mA	V_{DD} = 5V, V_{OL} = 0.4V V_{DD} = 12V, V_{OL} = 1.2V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

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DC Electrical Characteristics (Cont'd) - Voltages are with respect to ground (V_{SS}), $T_A = 25°C$, $f_c = 3.579545$ MHz unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
13	OUTPUTS	Output Drive Current OSC2, N Channel Sink	I_{OL} I_{OL}	0.1 0.25			mA mA	$V_{DD} = 5V$, $V_{OL} = .4V$ $V_{DD} = 12V$, $V_{OL} = 1.2V$
14		Output Drive Current, FL, FH P Channel Source	I_{OH} I_{OH}	0.2 0.5			mA mA	$V_{DD} = 5V$, $V_{OH} = 4.6V$ $V_{DD} = 12V$, $V_{OH} = 10.8V$
15		Output Drive Current, OSC2, P Channel Source	I_{OH} I_{OH}	0.1 0.25			mA mA	$V_{DD} = 5V$, $V_{OH} = 4.6V$ $V_{DD} = 12V$, $V_{OH} = 10.8V$
16		Output Voltage, V_{Ref}	V_{Ref} V_{Ref}	2.3 5.4		2.6 6.2	V V	$V_{DD} = 5V$, No Load $V_{DD} = 12V$, No Load
17		Output Resistance, V_{Ref}	R_{OR} R_{OR}			16 8	kΩ kΩ	$V_{DD} = 5V$ $V_{DD} = 12V$

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Voltages are with respect to ground (V_{SS}), $T_A = 25°C$, $f_c = 3.579545$, $V_{DD} = 4.75$ - 13V.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	FILTER	Dynamic Range		30		36	dB	
2		Valid Input Signal Levels (Each tone of composite signal)		 27.9 67.0		$V_{DD}/2$ 883 2120	V_{pp} mVrms mVrms	 $V_{DD} = 5V$ $V_{DD} = 12V$
3		Input Impedance	Z_I	10			MΩ	
4		Passband Ripple	A_V		±0.3	±1.0	dB	See Note 1
5		Low Group Lower Limit 1dB Bandwidth Upper Limit	f_{LL} f_{LU}	 958	670 990	684	Hz Hz	
6		High Group Lower Limit 1dB Bandwidth Upper Limit	f_{HL} f_{HU}	 1660	1162 1740	1188	Hz Hz	
7		Intergroup Rejection Low Group with High Tone	IR_{L1209} IR_{L1477}	34 36	45 40		dB dB	1209Hz - w.r.t. 770Hz 1477Hz - w.r.t. 770Hz
8		Intergroup Rejection High Group with Low Tone	IR_{H941} IR_{H770}	38 36	50 40		dB dB	941Hz - w.r.t. 1336Hz 770Hz - w.r.t. 1336Hz
9		Dial Tone Rejection Low Group	DR_{L440} DR_{L350}	40 28	60 30		dB dB	440Hz - w.r.t. 770Hz 440Hz - w.r.t. 770Hz
10		Dial Tone Rejection High Group	DR_{H440} DR_{H350}	52 50	60 55		dB dB	440Hz - w.r.t. 1336Hz 350Hz - w.r.t. 1336Hz
11		FHT FLT Maximum Permissible Load	R_{LFT} C_{LFT}	250		 1000	kΩ pF	
12	LIM	Output Rise Time FL, FH Output Fall Time FL, FH	t_{TLHO} t_{THLO}		90 60	150 100	ns ns	10% to 90% V_{DD}
13	CLOCK	Crystal/Clock Freq. OSC1, OSC 2	f_c	3.5759	3.5795	3.5831	MHz	
14		Clock Rise Time Input Fall Time (OSC 1) Duty Cycle	t_{LHCI} t_{HLCI} DC_{CI}	 40	 50	110 110 60	ns ns %	 See Note 2
15		Clock Output OSC 2 Capacitive Load	C_{LOC}			30	pF	Unbalanced load see Fig. 5
16		Capacitance Any Input	C_I		5	7.5	pF	

Note 1. Passband ripple measured with respect to a passband gain of 0 dB ± 1dB.
Note 2. 10% to 90% V_{DD}. Externally Applied Clock.

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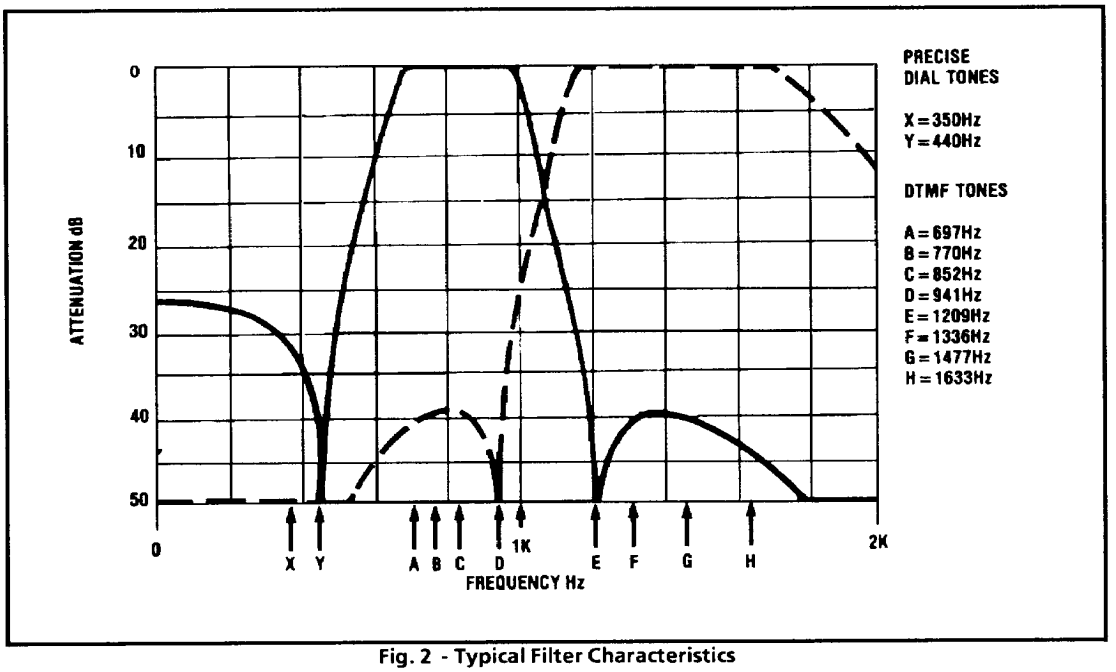

Fig. 2 - Typical Filter Characteristics

Pin Description

Pin #	Name	Description
1	FL	**Low Group Limiter Output.**
2	FLT	**Test Output.** Monitors low group filter output. Decouple to V_{SS} with 680pF capacitor.
3	NC	**Not Connected.**
4	INPUT	**Tone Signal Input (single ended).**
5	V_{Ref}	**Internal Reference.** Can be used to bias input via 2MΩ resistor.
6	PDWN	**Power Down Active High.** Internal pull down transistor. A high level signal powers down the device and inhibits the oscillator.
7	NC	**Not Connected.**
8	V_{SS}	**Negative (OV) Power Supply.**
9	NC	**Not Connected.**
10	FH	**High Group Limiter Output.**
11	FHT	**Test Output.** Monitors high group filter output. Decouple to V_{SS} with 680pF capacitor.
12	NC	**Not Connected.**
13	NC	**Not Connected.**
14	OSC2	**Clock Output.**
15	OSC1	**Clock Input.** 3.579545 MHz crystal connected between this pin and OS2 completes the internal oscillator circuit.
16	VDD	**Positive Power Supply.**

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Functional Description

The MT8865 separates the high group and low group components of the dual tone signal and limits the resulting pair of sine waves, to produce square waves having the same frequencies as the individual input tones. These limited low group and high group tones appear at the FL and FH outputs respectively. To implement a complete DTMF receiver the FL and FH outputs are connected to the FL and FH inputs of the DTMF Digital Decoder (MT8860). See Fig. 3.

Separation of the low group and high group tones is achieved by applying the dual tone signal simultaneously to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low group and high group tones. The frequency characteristic of each filter (see Fig. 2) also incorporates a notch at 440Hz to provide dial tone rejection. Each filter output is followed by a single order switched capacitor section which operates as an interpolator smoothing the signals prior to limiting. The limiting functions are performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals and noise. The comparator outputs are buffered to drive the FL and FH output pins and detector device inputs. The MT8865 has a single ended input allowing connection either to a PCM decoder, radio receiver (Fig. 3) or via a differential buffer to a telephone line (Fig. 4). The signal input (Pin 4) should be biased at $V_{DD}/2$. With the input

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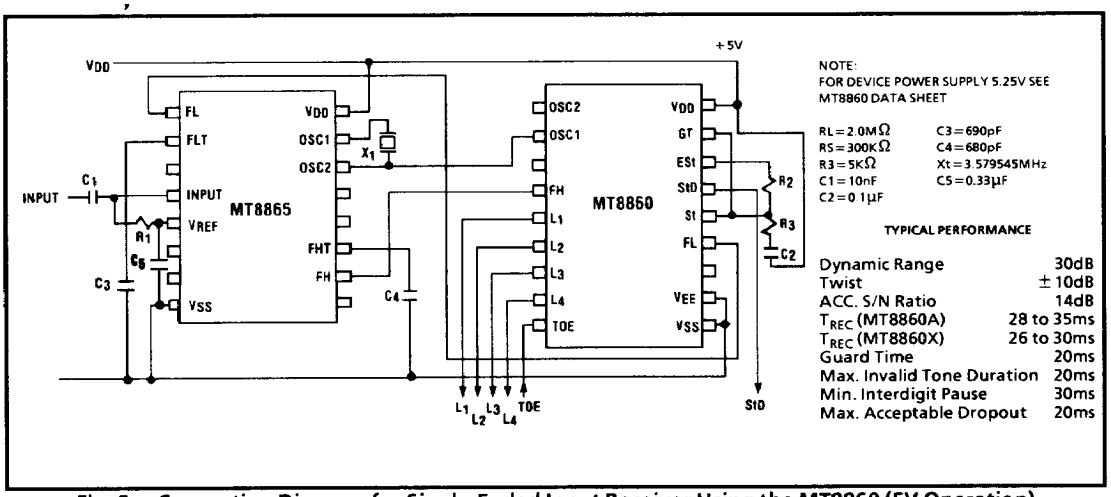

Fig. 3 - Connection Diagram for Single-Ended Input Receiver Using the MT8860 (5V Operation)

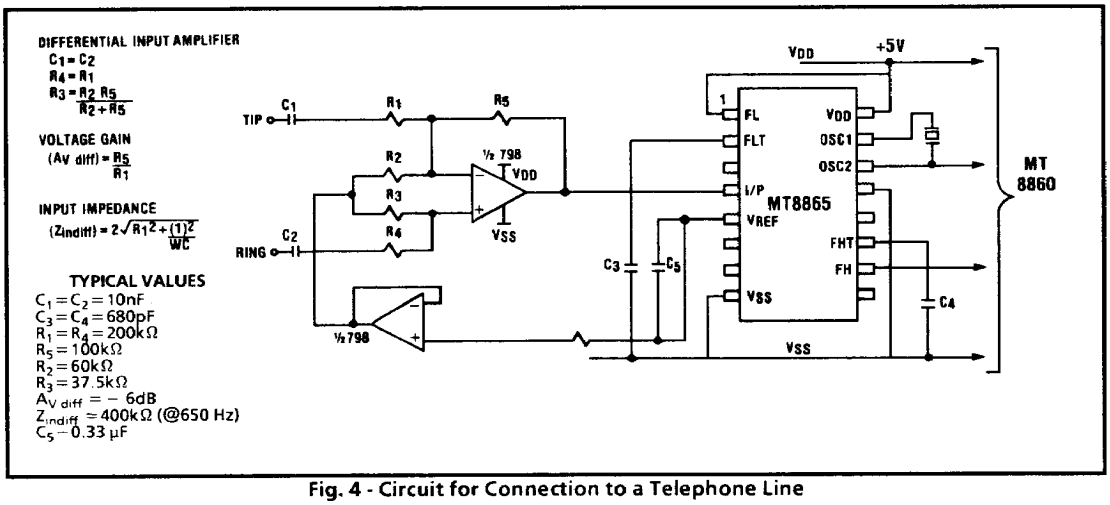

Fig. 4 - Circuit for Connection to a Telephone Line

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capacitively coupled, this is achieved by connecting the signal input to V_{Ref} (Pin 5) via a 2MΩ resistor.

FLT and FHT allow the filter outputs to be monitored prior to limiting, and should each be decoupled to V_{SS} by 680pF capacitors.

The MT8865 and its companion, the MT8860 DTMF decoder, can share a crystal by cascading the oscillator output (OSC2) to the adjacent device oscillator input (OSC1). The recommended circuit is shown in Figure 5.

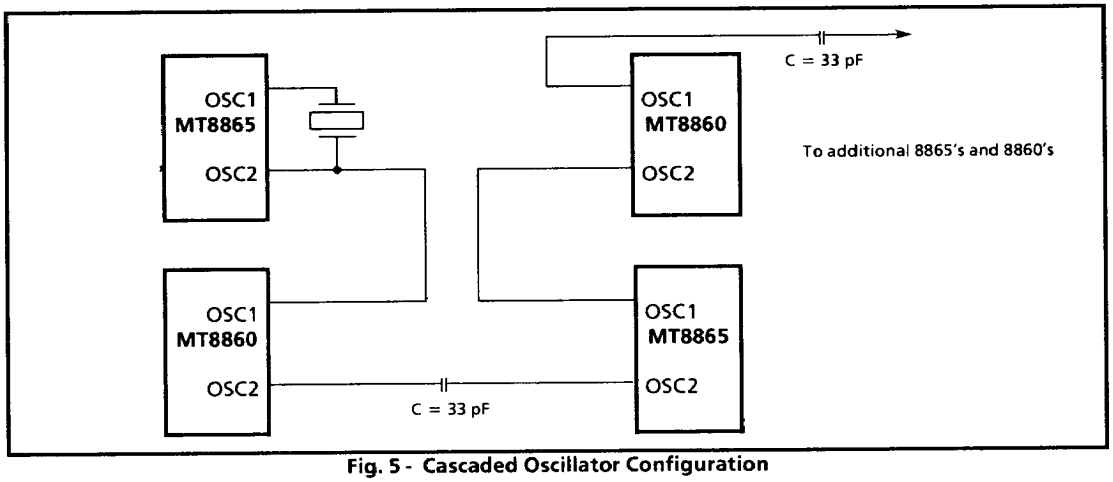

Fig. 5 - Cascaded Oscillator Configuration

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